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(54) Title: MEMORY STRUCTURE, METHOD FOR FABRICATING THEREOF, MEMORY ARRAY DEVICE AND METHOD FOR OPERATING THEREOF

(57) Abstract: According to various embodiments, there is provided a memory structure including a conductive core; and a switching material layer at least partially surrounding the conductive core, wherein the switching material layer includes a plurality of sections, each section of the plurality of sections arranged at least substantially parallel to a height of the conductive core; and wherein each section includes a plurality of cells, each cell of the plurality of cells arranged at a respective position along the height of the conductive core.
MEMORY STRUCTURE, METHOD FOR FABRICATING THEREOF, MEMORY ARRAY DEVICE AND METHOD FOR OPERATING THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Singapore Patent Application number 102014057.16R filed 15 September 2014, the entire contents of which are incorporated herein by reference for all purposes.

TECHNICAL FIELD

[0002] The present invention relates to memory structures, methods for fabricating memory structures, memory array devices and methods for operating memory array devices.

BACKGROUND

[0003] Since its introduction in 1988 by Toshiba, NAND flash non-volatile memory has undergone an unprecedented growth. New technologies, such as resistive random-access memory (RRAM) have emerged as competing alternatives to the NAND flash. To compete with the NAND flash, a new architecture to achieve high memory density may be required.

SUMMARY

[0004] According to various embodiments, there may be provided a memory structure including a conductive core; and a switching material layer at least partially surrounding the conductive core, wherein the switching material layer includes a plurality of sections, each section of the plurality of sections arranged at least substantially parallel to a height of the conductive core; and wherein each section includes a plurality of cells, each cell of the plurality of cells arranged at a respective position along the height of the conductive core.

[0005] According to various embodiments, there may be provided a method for fabricating a memory structure, the method including providing a conductive core; and surrounding the conductive core with a switching material layer so that the switching material layer at least partially surrounds the conductive core; wherein the switching material layer includes a plurality of sections, each section of the plurality of sections arranged at least substantially.
parallel to a height of the conductive core; and wherein each section includes a plurality of cells, each cell of the plurality of cells arranged at a respective position along the height of the conductive core.

[0006] According to various embodiments, there may be provided a method for operating a memory array device, the method including addressing a bit column from an array of bit columns, wherein each bit column of the array of bit columns includes a conductive core; a switching material layer at least partially surrounding the conductive core, wherein the switching material layer includes a plurality of sections, each section of the plurality of sections arranged at least substantially parallel to a height of the conductive core; wherein each section includes a plurality of cells, each cell of the plurality of cells arranged at a respective position along the height of the conductive core.

**BRIEF DESCRIPTION OF THE DRAWINGS**

[0007] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments are described with reference to the following drawings, in which:

[0008] FIG. 1 shows a conceptual diagram of a memory structure according to various embodiments.

[0009] FIG. 2 shows a conceptual diagram of a memory structure according to various embodiments.

[0010] FIG. 3 shows a conceptual diagram of a memory array device according to various embodiments.

[0011] FIG. 4 shows a conceptual diagram of a memory array device according to various embodiments.

[0012] FIG. 5 shows a flow diagram showing a method for fabricating a memory structure according to various embodiments.

[0013] FIG. 6 shows a flow diagram showing a method for operating a memory array device according to various embodiments.

[0014] FIG. 7 shows a cross-sectional view of part of a memory array device according to various embodiments.

[0015] FIG. 8A and 8B shows perspective views of a memory structure according to various embodiments.
FIG. 9 shows a top view of an access selector according to various embodiments.

FIG. 10 shows a perspective view of two adjacent access selectors according to various embodiments.

FIG. 11 shows a cross-sectional view of part of a memory array device according to various embodiments.

FIG. 12 shows a top view of a memory array device according to various embodiments.

FIG. 13 shows a table showing a relationship between layer number and cell size.

FIG. 14 shows a perspective view of a memory array device according to various embodiments.

DESCRIPTION

 embodiments described below in context of the devices are analogously valid for the respective methods, and vice versa. Furthermore, it will be understood that the embodiments described below may be combined, for example, a part of one embodiment may be combined with a part of another embodiment.

The term "coupled" (or "connected") herein may be understood as electrically coupled or as mechanically coupled, for example attached or fixed, or just in contact without any fixation, and it will be understood that both direct coupling or indirect coupling (in other words: coupling without direct contact) may be provided.

In the context of various embodiments, "resistive random access memory" may be but is not limited to being interchangeably referred to as "resistive memory" or "ReRAM" or "RRAM" or "resistive RAM".

In the context of various embodiments, "memory cell" may be but is not limited to being interchangeably referred to as a "cell".

It should be appreciated and understood that the term "substantially" may include "exactly" and "similar" which is to an extent that it may be perceived as being "exact". For illustration purposes only and not as a limiting example, the term "substantially" may be quantified as a variance of +1-5% from the exact or actual.

Since its introduction in 1988 by Toshiba, NAND flash non-volatile memory has undergone an unprecedented growth. New technologies, such as resistive random-access memory (RRAM) have emerged as competing alternatives to the NAND flash. To compete with the NAND flash, a new architecture to achieve high memory density may be required.
FIG. 1 shows a conceptual diagram of a memory structure 100 according to various embodiments. The memory structure 100 may include a conductive core 102 and a switching material layer 104. The switching material layer 104 may at least partially surround the conductive core 102. The switching material layer 104 may include a plurality of sections. Each section of the plurality of sections may be arranged at least substantially parallel to a height of the conductive core 102. Each section of the plurality of sections may include a plurality of cells and each cell of the plurality of cells may be arranged at a respective position along the height of the conductive core 102.

In other words, a memory structure 100 according to various embodiments, may include a conductive core 102 which is at least partially surrounded by a switching material layer 104. The switching layer 104 may fully surround the conductive core 102. The switching layer 104 may surround the conductive core 102 so as to cover an external surface of the conductive core 102. The switching material layer 104 may be configured to function as an array of memory cells, including a plurality of sections and a plurality of cells within each section of the plurality of sections. The plurality of sections may be portions of the switching material layer 104, divided along a longitudinal axis parallel to a height of the conductive core. Each section may be further divided into the plurality of cells, along a latitudinal axis perpendicular to the height of the conductive core 102. The plurality of cells may be non-volatile random access memory cells. The plurality of cells may include at least one of a resistive memory cell, such as a resistive random access memory (RRAM) or a phase-change random access memory (PCRAM) cell. The switching material layer 104 which may include a dielectric material or a phase-change material, may be coupled to electrodes for changing the resistance across the dielectric material. The RRAM cell may be operable by changing the resistance across the dielectric material.

FIG. 2 shows a conceptual diagram of a memory structure 200 according to various embodiments. The memory structure 200 may be similar to the memory structure 100 of FIG. 1, in that it may also include a conductive core 102 and a switching material layer 104. The switching material layer 104 may at least partially surround the conductive core 102. The switching material layer 104 may include a plurality of sections. Each section of the plurality of sections may be arranged at least substantially parallel to a height of the conductive core 102. Each section of the plurality of sections may include a plurality of cells and each cell of the plurality of cells may be arranged at a respective position along the height of the conductive core 102. The memory structure 200 may further include a plurality of access selectors 206. Each access selector 206 of the plurality of access selectors 206 may be
coupled to a respective cell of the plurality of cells of the plurality of sections. The access selector 206 may include a diode which may be a PN junction diode or a Schottky diode.

[0031] FIG. 3 shows a conceptual diagram of a memory array device 300 according to various embodiments. The memory array device 300 may include an array of bit columns, herein referred to as a bit column array 304. The bit column array 304 may include a plurality of bit columns 302. Each bit column 302 of the bit column array 304 may include the memory structure 100 of FIG. 1 or the memory structure 200 of FIG. 2. The plurality of bit columns 302 may be arranged in a plurality of rows and in a plurality of columns. Each bit column 302 may include a conductive core and a switching material layer at least partially surrounding the conductive core. The switching material layer may include a plurality of sections, each of which may be arranged at least substantially parallel to a height of the conductive core. Each section of the plurality of sections may include a plurality of cells and each cell of the plurality of cells may be arranged at a respective position along the height of the conductive core.

[0032] FIG. 4 shows a conceptual diagram of a memory array device 400 according to various embodiments. The memory array device 400 may include the bit column array 304 of FIG. 3. The memory device array 400 may further include a plurality of bitlines 440, a plurality of selector gate lines 442, a plurality of column selectors 444, a plurality of wordlines 446 and a layer decoder 448. The plurality of bitlines 440 may be configured to select a row from the plurality of rows of the bit column array 304. The plurality of selector gate lines 442 may be configured to select a column from the plurality of columns of the bit column array 304. Each selector gate line 442 of the plurality of selector gate lines 442 may be arranged perpendicular to each bitline 440 of the plurality of bitlines 440. Each selector gate line 442 of the plurality of selector gate lines 442 may be further arranged to be perpendicular to the conductive core of a respective bit column. Each bitline 440 of the plurality of bitlines 440 may also be arranged to be perpendicular to the conductive core of a respective bit column.

[0033] Each column selector 444 of the plurality of column selectors 444 may be coupled to a respective bitline 440 and may be further coupled to a respective selector gate line 442. The plurality of column selectors 444 may include at least one of a vertical transistor or a horizontal transistor. The column selector 444 may be a one of a field effect transistor (FET) or a bipolar junction transistor (BJT). The column selector 444 may be one from the group consisting of a metal-oxide-semiconductor field-effect transistor (MOSFET), a junction gate field-effect transistor (JFET), a dual-gate MOSFET, a fast-recovery epitaxial diode FET
(FREDFET), a heterostructure insulated gate transistor (HIGFET), a modulation-doped field-effect transistor (MODFET), a tunnel field-effect transistor (TFET), an insulated-gate bipolar transistor (IGBT), a high-electron-mobility transistor (HEMT), an ion-sensitive field-effect transistor (ISFET), a metal-semiconductor field-effect transistor (MESFET), a graphene nanoribbon field-effect transistor (GNRFET), a vertical-slit field-effect transistor (VeSFET), a carbon nanotube field-effect transistor (CNTFET) and a quantum field effect transistor (QFET).

[0034] Each wordline 446 of the plurality of wordlines 446 may be coupled to a respective access selector of the plurality of access selectors. The plurality of wordlines 446 may be formed as a comb-shaped electrode having a plurality of comb teeth and a connecting bar. The connecting bar may be at least substantially perpendicular to the plurality of comb teeth, and may be coupled to each comb tooth of the comb-shaped electrode. Each comb tooth of the plurality of comb teeth may be arranged at least substantially perpendicular to a respective conductive core. The plurality of wordlines 446 may include a first set of wordlines and a second set of wordlines. The first set of wordlines may be coupled to a first section of the plurality of sections of each switching material layer while the second set of wordlines may be coupled to a second section of the plurality of sections of each switching material layer. Each of the first set of wordlines and the second set of wordlines may be a comb-shaped electrode having a plurality of comb teeth arranged at least substantially perpendicular to a respective conductive core. The layer decoder 448 may be configured to select one of the first set of wordlines and the second set of wordlines. The comb teeth of the first set of wordlines may be arranged in between the comb teeth of the second comb-shaped electrode, in other words, the first of wordlines and the second set of wordlines may be positioned in an interdigitated manner such that the comb teeth of the first comb-shaped electrode may be interdigitated with the comb teeth of the second comb-shaped electrode.

[0035] FIG. 5 shows a flow diagram 500 showing a method for fabricating a memory structure according to various embodiments. The method for fabricating a memory structure may include processes 550 and 552. In 550, a conductive core may be provided. In 552, the conductive core may be surrounded with a switching material layer so that the switching material layer at least partially surrounds the conductive core. The switching material layer may include a plurality of sections. Each section of the plurality of sections may be arranged at least substantially parallel to a height of the conductive core. Each section of the plurality of sections may include a plurality of cells. Each cell of the plurality of cells may be arranged at a respective position along the height of the conductive core.
The method for fabricating a memory structure may further include providing a plurality of access selectors. Each access selector of the plurality of access selectors may be coupled to a respective cell of the plurality of cells of the plurality of sections. The process of providing the plurality of access selectors may include forming a plurality of access selector layers. The plurality of access selector layers may be formed by patterning a p-type material and patterning an n-type material. Providing the plurality of access selectors may further include depositing an insulator layer between every two access selector layers of the plurality of access selector layers. A row of access selectors may be formed on each access selector layer of the plurality of access selector layers. The row of access selectors on each access selector layer may include at least one access selector. The plurality of access selector layers may be etched as part of the process to provide the conductive core or to surround the conductive core with a switching material layer. The plurality of access selector layers may be etched between every two access selectors of each row of access selectors on each access selector layer. The process of providing the conductive core or the process of surrounding the conductive core with the switching material layer may include depositing a switching material into the gap, etching the switching material to form a hollow core in the switching material, and depositing a conductive material into the hollow core. The deposition of the switching material into the gap may also include atomic layer deposition or electroplating.

FIG. 6 shows a flow diagram 600 showing a method for operating a memory array device, according to various embodiments. The method for operating a memory array device may include a process 660. In 660, a bit column from an array of bit columns may be addressed. Each bit column of the array of bit columns may include a conductive core and a switching material layer at least partially surrounding the conductive core. The switching material layer may include a plurality of sections. Each section of the plurality of sections may be arranged at least substantially parallel to a height of the conductive core. Each section of the plurality of sections may include a plurality of cells. Each cell of the plurality of cells may be arranged at a respective position along the height of the conductive core. The array of bit columns may be arranged as a plurality of rows and a plurality of columns such that each bit column belongs to a respective row and a respective column. Addressing the bit column from the array of bit columns may include selecting the row of the array of bit columns and selecting the column of the array of bit columns. The memory array device may include a plurality of bitlines, wherein each bitline of the plurality of bitlines may be coupled to a respective row of bit columns. The memory array device may also include a plurality of selector gate lines, wherein each selector gate line may be coupled to a respective column of
bit columns. The row of the array of bit columns may be selected by applying a voltage to a respective bitline of the plurality of bitlines, while the column of the array of bit columns may be selected by applying a voltage to the respective selector gate line of the selector gate lines.

[0038] The method for operating a memory array device may further include accessing a cell of the plurality of cells of the plurality of sections. Accessing the cell may include operating an access selector coupled to the cell. The memory array device may include a plurality of wordlines, wherein each wordline of the plurality of wordlines may be coupled to a respective access selector. Operating the access selector coupled to the cell may include applying a voltage to a respective wordline coupled to the access selector to be operated.

[0039] A memory structure, according to various embodiments, relates to semiconductors and memory technology. More particularly, the memory structure may be part of a three-dimensional (3D) RRAM architecture. The 3D RRAM memory architecture may include a multi-layer stack with vertical memory cells, horizontal fin-like diode architecture and a 3D addressing scheme. The memory architecture may be a high density non-volatile memory array with a 3D one-diode, one-resistor (1D1R) architecture. The memory structure may be suitable for a 3D diode and memory integration scheme. A method for fabricating the memory structure may allow the fabrication of high quality diodes with low leakage current and high drive current. Therefore, the memory structure may be suited for building a large array. This architecture may enable a tunable drive current and may allow freedom in the selection of diode materials.

[0040] A memory array device, according to various embodiments, may include a hybrid 3D RRAM architecture. The memory array device may include access selectors which may be individually fabricated, with the flexibility to select a suitable material for fabricating the access selectors. The access selectors may be diodes, such as PN junction diodes or Schottky diodes. Other types of access selectors, for example, Ovonic Threshold Switch (OTS), Mott effect-based selector, Mixed-Ionic-Electronic-Conduction (MIEC) based selector or Field-Assisted-Superlinear-Threshold (FAST) selector, may also be used in place of the diodes. Furthermore, the ability to fabricate the access selectors separately may enable fabrication of high quality diodes which may enable the construction of a higher volume memory array. The high quality diodes may have advantages in terms of low leakage current, high on-current, and good uniformity. The memory array device may also have an easily tunable ratio of active diode size over active memory size. The ratio may be tuned easily by controlling the deposition thickness during the fabrication process. A large active diode size over active
memory size ratio or a large diode contact size may enable the memory array device to meet the high drive current requirements of memory cells such as a unipolar RRAM or PCRAM.

[0041] FIG. 7 shows a cross-sectional view 700 of part of a memory array device, according to various embodiments. The memory array device may have a 3D memory architecture. The memory array device may include a switching material 770, a conducting material 772, a first selector layer 774a, a second selector layer 774b, an interconnect material 776 and an insulator material 778. The switching material 770 may be a RRAM switching material. Each of the conducting material 772 and the interconnect material 776 may be a metal. The first selector layer 774a and the second selector layer 774b may form an access selector, such as a PN junction diode or a Schottky diode. The switching material 770 and the conducting material 772 may form a memory structure which may be at least substantially similar to or identical to the memory structure 100 of FIG. 1. The interconnect material 776 may be provided below the memory structure, for electrically coupling to an external device or circuit, for example a logical circuit. The insulator material 778 may be silicon dioxide or a material with a small dielectric constant, in other words, a low-k material. The insulator material may be an oxide material, including but not limited to fluorine-doped silicon dioxide, carbon-doped silicon dioxide and porous silicon dioxide.

[0042] A method for fabricating a memory structure according to various embodiments is described in this paragraph, with reference to FIG. 7. A layer of interconnect material 776 may be provided on a wafer and patterned. A layer of insulator material 778 may be deposited over the layer of interconnect material 776. The second selector layer 774b may be deposited over the insulator material 778, and patterned to form parallel lines. Next, the first selector layer 774a may be deposited over the second selector layer 774b and its underlying insulator material 778, and patterned perpendicularly relative to the patterning of the second selector layer 774b, to form a row of access selectors. For example, if the access selectors are PN junction diodes, the first selector layer may be an n-type material while the second selector type may be a p-type material. Following the formation of the row of access selectors, a further layer of insulator material 778 may be deposited over the row of access selectors. A further row of access selectors may be formed over the further layer of insulator material 778 by repeating the processes of depositing and patterning each of the first selector layer 774a and the second selector layer 774b, as described above.

[0043] The above-described processes of depositing insulator material 778 and forming rows of access selectors may be repeated for multiple stacks. Each stack may include a row of access selectors and a layer of insulator material 778. A chemical-mechanical planarization
process (CMP) may be carried out on the layers of insulator material 778, to maintain flatness of the wafer. CMP is a process of smoothing surfaces with the combination of chemical and mechanical forces, in other words, a hybrid of chemical etching and free abrasive polishing. The mask for patterning the first selector layer 774a and the mask for patterning the second selector layer 774b may be used repeatedly for the plurality of stacks. Therefore, two masks can be sufficient for creating a plurality of stacks. After creating the plurality of stacks, column patterning and etching may be performed. During etching, the layers of insulator material 778 and the plurality of first selector layers 774a may be repeatedly etched until the layer of interconnect material 776 is exposed, to create a gap. An etching stop layer may also be provided on top of the layer of interconnect material 776, to assist with achieving etching uniformity, as well as to provide an indication of an etching end point. The switching material 770 may be deposited into the gap created by the etching process. The switching material 770 may then be etched until the layer of interconnect material 776 is exposed. The etching of the switching material 770 may be performed using a maskless self-align technique. As a result of the etching of the switching material 770, a hollow column may be formed within the switching material 770, such that the switching material 770 forms a wall surrounding the hollow column, with the wall in contact with the first selector layer 774a of each stack of the multiple stack deposition. The conducting material 772 may be deposited into the hollow column to form a conductive core. The conductive core may be at least substantially similar to, or identical to the conductive core 102 of FIGS. 1 and 2. The deposition of the conductive material 772 may be followed by a CMP. The conductive core and the switching material 770 surrounding thereof, may be the memory structure 100 of FIG. 1. The conductive core, the switching material 770 surrounding thereof, and the access selectors coupled to the switching material 770, may be the memory structure 200 of FIG. 2. The memory structure may be at least substantially cylindrical in shape. As the memory structure may have a high aspect ratio, the deposition of the switching material 770 and the deposition of the conductive material 772 may be preferably deposited using at least one of atomic layer deposition (ALD) method or electroplating. If electroplating is used, a thin layer of ALD seed layers, such as Ta or TaN or a barrier layer, may be deposited before electroplating is carried out.

[0044] FIG. 8A shows a perspective view of a bit column 800 according to various embodiments. The bit column 800 may be identical or at least substantially similar to the memory structure 100 of FIG. 1 or the memory structure 200 of FIG. 2. The bit column 800 may include the memory structure 100 of FIG. 1 or the memory structure 200 of FIG. 2. The
bit column 800 includes a switching material layer 804 which is formed of the switching material 770 shown in FIG. 7; and a conductive core 802 formed of the conductive material 772 shown in FIG. 7. The switching material layer 804 may be identical or at least substantially similar to the switching material layer 104 of FIGS. 1 and 2. The conductive core 802 may be identical or at least substantially similar to the conductive core 102 of FIGS. 1 and 2. FIG. 8A shows the first two stacks of the memory array device of FIG. 7, cut off along line AB and line CD, and also excluding any adjacent memory structures not shown in FIG. 7. The perspective view shows electrodes 884a-884d, which couple the bit column 800 to respective access selectors. The switching material layer 804 forms a wall of the bit column and may function as an active area for RRAM switching. As the etching process to create the gap, as described in the previous paragraph, breaks the first selector layer in between two access selectors formed in the same stack, there will be two memory cells coupled to each bit column, wherein one memory cell is located on each side of two sides of the bit column. The two memory cells may be a first cell coupled to a first electrode 884a and a second cell coupled to a second electrode 884b. Each of the first electrode 884a and the second electrode 884b may be coupled to a respective access selector, or may be formed as part of the respective access selector. The first electrode 884a and the second electrode 884b may be formed as part of a same stack while the third electrode 884c and the fourth electrode 884d may be formed as part of a same further stack.

[0045] The dimension of the active area in a horizontal axis 880, in other words, a horizontal dimension, may be defined by lithography such that there is a minimum feature size. The minimum feature size may be denoted as F. The dimension of the active area in a vertical axis 882, in other words, a vertical dimension, may be defined by deposition thickness. Deposition thickness may be easily controlled by time duration of deposition or cycles of deposition. The vertical dimension may therefore, be smaller than F, for example, the vertical dimension can be 0.5F or even smaller. For example, an area of the active contact size, as illustrated in the perspective view of FIG. 8A, is 0.5F^2. The vertical dimension may be made smaller, so as to allow more stacks to be fabricated in a single memory structure. In other words, the smaller the vertical dimension, the more stacks that can be accommodated within the height of the memory structure.

[0046] FIG. 8B shows the bit column 800 of FIG. 8A, rotated 90° about a centre axis 888 parallel to the vertical axis 882. The switching material forms an external wall of the bit column, in other words, the switching material layer 804 at least partially surrounds the conductive core 802 formed of the conductive material. The switching material layer 804 is
shown as divided into 4 partitions, labeled as "A" 886A, "B" 886B, "C" 886C and "D" 886D. The switching material layer may function as plurality of cells. The switching material layer may include a plurality of sections, each section of the plurality of sections arranged at least substantially parallel to a height of the conductive core, in other words, each section may be arranged at least substantially parallel to the vertical axis 882. An example of the section is a first strip of the switching material layer 804 consisting of the partition "A" 886A and the partition "C" 886C. Another example of a section is a second strip of the switching material layer 804 including the partition "B" 886B and the partition "D" 886D. Each section may include a plurality of cells, each cell of the plurality of cells arranged at a respective position along the vertical axis 882. As shown in the perspective view 800B, the first strip includes the partition "A" 886A and the partition "C" 886C, wherein the partition "A" 886A is arranged above the partition "C" 886C along the vertical axis 882. Similarly, the second strip includes the partition "B" 886B and the partition "D" 886D, wherein partition "B" 886B is arranged above partition "D" 886D along the vertical axis 882. Each of the partitions 886A-886D may include a respective memory cell. Each of the partitions 886A-886D may be coupled to a respective electrode 884a-884d for coupling to a respective access selector. The respective memory cells may be a portion within the respective partition which is in contact with the respective access selector. For example, partition "A" 886A can include a memory cell, the memory cell being a portion of the switching material 770 within partition "A" 886A, which is in contact with an access selector through the electrode 884a. In order to operate partitions within a same stack individually, for example, to operate the partition "A" 886A separately from the partition "B" 886B, each section to which the partition belongs, need to be separately addressable.

[0047] FIG. 9 shows a top view of an access selector 900 according to various embodiments. The access selector 900 may be identical to or at least substantially similar to, the access selector 206 of FIG. 2. For example, the access selector 900 may be understood to be a first stack of the memory array device of FIG. 7, in between line EF and line GH. The access selector may include a first selector layer 774a and a second selector layer 774b. The first selector layer 774a and the second selector layer 774b may be patterned such that the length of the first selector layer 774a may be perpendicular to the length of the second selector layer 774b, wherein length refers to a longer dimension of the layer. In other words, the length of the first selector layer 774a is in the y-direction, i.e. parallel to the axis 990; while the length of the second selector layer 774b is in the x-direction, i.e. parallel to the axis 880. The access selector may be coupled to an electrode 884b on a first side and a further electrode 884b' on a
second side, wherein the second side opposes the first side. Both the electrode 884b and the
second electrode 884b' may include the same material as the first selector layer 774a. Both
the electrode 884b and the second electrode 884b' may be formed as part of the first selector
layer 774a and may be contiguous with the first selector layer 774a. Each of the first
electrode 884b and the second electrode 884b' may be coupled to a respective cell. The first
electrode 884b may be coupled to the cell that is partition "B" 886B of the memory structure
shown in FIG. 8B while the second electrode 884b' may be coupled to another cell that may
be part of a further memory structure. Each of 886B and 886B' may represent a different bit.

[0048] As the access selector 900 may be fabricated separately from the memory cell, the
range of materials for fabricating the access selector 900 need not be limited by the range of
materials suitable for fabricating the memory cell. Therefore, there may be a large flexibility
in the selection of materials for fabricating the access selectors 900 and as such, the range of
access selectors 900 that can be fabricated, is wide. For example, the access selector 900 may
be any one of, but not limited to a PN junction diode, a Schottky diode, a punch through
diode, an OTS switch or a MIEC switch. In addition, the ability to fabricate the access
selector 900 separately from the memory cell may provide freedom in the sizing of the access
selector 900. For example, the horizontal dimension of the access selectors 900 may be
defined by lithography freely, varying from F to 2F, or larger. For example, the dimension in
the x-direction may be 2F while the dimension in the y-direction may be F, while the vertical
dimension in the z-direction may be F. For such an access selector 900, which may be a
diode, the diode size is 6F². The memory contact size as shown in FIG. 8A, is 0.5F². Therefore,
the ratio of the diode size to the memory contact size may be 12, as shown in
equation (1). The high ratio of diode size over memory active size may be able to supply high
drive current to set/reset the memory, which may be an important feature for unipolar RRAM
or PCRAM.

\[
\frac{\text{Diode size}}{\text{memory contact size}} = \frac{6F^2}{0.5F^2} = 12 \quad \text{Equation (1)}
\]

[0049] Furthermore, the 3D access selector 900 may have a fin-like structure, or in other
words, a fin-like architecture, as shown in FIG. 9, the "fins" being extensions of the first
selector layer 774a. This 3D structure may increase the active interface of the access selector
900. With the large active interface, the access selector 900 may be able to handle a large
drive current during set/reset operations, as required by memory cell technologies such
unipolar RRAM and PCRAM.
[0050] By controlling the deposition thickness and pattern width of the second selector layer 774b as well as the pattern width of the first selector layer 774a, the contact area between the first selector layer 774a and the second selector layer 774b can be easily adjusted. The larger the contact area between the first selector layer 774a and the second selector layer 774b, in other words, the diode size in Equation (1), the higher the $I_{on}$ current of the access selector 900 and the larger the drive current on the memory cell 886b or 886b'. Besides, the access selector 900 may be separately fabricated, from the memory cells 886 and 886b'. The selection of materials for the access selector 900 may have nearly no effect on the formation of the memory cells 886 and 886b'. As such, the memory structure including the memory cells 886 and 886b' and the access selector 900 may provide a tunable drive current and may allow freedom in selection of materials for the access selector 900.

[0051] FIG. 10 shows a perspective view 1000 showing a first access selector 1010 and a second access selector 1012 within a same stack, according to various embodiments. Each access selector of the two access selectors may be at least substantially similar or identical to the access selector of FIG. 9. As the process of providing a bit column includes etching a gap in between two access selectors formed in the same stack, there will be two access selectors coupled to a single bit column of a memory structure. The bit column in between the first access selector 1010 and the second access selector 1012 is not shown in its entirety in the perspective view 1000, so that the access selectors may be more clearly visible. For example, the first access selector 1010 in FIG. 10 may be understood to be the access selector 900 of FIG. 9 while the second access selector 1012 may be an access selector in the same stack, separated from the first access selector 1010 by the bit column formed by the conductive material 772 as shown in FIG. 7. The switching material coupled to the electrode 884b may be part of the partition "B" 886B shown in FIG. 8B and FIG. 9. The switching material in the partition "B" 886B may function as a memory cell to hold Bit 1. Similarly, the switching material coupled to the electrode 884a may be part of the partition "A" 886A shown in FIG. 8B. The switching material in the partition "A" 886A may function as a memory cell to hold Bit 2.

[0052] FIG. 11 shows a cross-sectional view 1100 of part of a memory array device, according to various embodiments. The cross-sectional view 1100 is similar to the cross-sectional view 700 of FIG. 7, with added labels for the electrodes 884a-d; and the partitions 886A-D, each of which including a respective memory cells. The electrodes 884a-d are the same or at least substantially similar to the electrodes 884a-d shown in FIGS. 8A, 8B, 9
and 10. The partitions 886A-D are also the same or at least substantially similar to the partitions 886A-D shown in FIGS. 8B, 9 and 10.

[0053] FIG. 12 shows a top view 1200 of a memory array device according to various embodiments. The memory array device may include a plurality of bitlines 440 and a plurality of wordlines 446. The plurality of wordlines 446 may be arranged at least substantially perpendicular to the plurality of bitlines 440. The memory array device may further include a plurality of bit columns. Each bit column of the plurality bit columns may be arranged at an intersection between a bitline 440 and a wordline 446. Alternate wordlines 446, for example, a first wordline and a third word line may be coupled together while a second wordline and a fourth wordline may be coupled together. The memory array device may include a plurality of electrodes, wherein each bit column is coupled to at least one electrode. As an example, FIG. 12 shows each bit column coupled to two electrodes, the electrodes being formed of the first selector layer 774a of FIGS. 7 and 11.

[0054] As an example, with reference to FIG. 12, the width of a wordline 446, herein also referred to as a wordline width 1202 can be F. The width of a bitline 440, herein also referred to as a bitline width 1204 can be 2F. The width of an electrode, herein also referred to as the electrode width 1206, can be F. The distance between a bitline 440 and another bitline 444, herein also referred to as a bitline-to-bitline distance 1208 can also be F. The diameter of a bit column, herein also referred to as a contact diameter 1210, can be 2F. The distance between a wordline 446 and a bit column, herein also referred to as a contact-to-wordline distance 1214 can be F, where F denotes the minimum feature size. The dotted rectangle 1212 may represent a minimum repeated pattern in the memory array device and therefore, may be used to calculate a cell size. Based on the dimensions stated in the above example, the width of the dotted rectangle 1212 is the sum of the bitline width 1204 and the bitline-to-bitline distance 1208 and therefore, the width of the dotted rectangle 1212 is 2F + F = 3F; and the height of the dotted rectangle 1212 is the sum of the contact diameter 1210, the wordline width 1202 and twice of the contact-to-wordline distance 1214 and therefore, the height of the dotted rectangle is 2F + F + 2xF = SF. The area of the dotted rectangle 1212 is therefore 3FxF = 1SF². As there are two memory cells inside the dotted rectangle 1212, each memory cell of the two memory cells occupies an area of $\frac{1SF^2}{2} = 7.5F^2$ in a single stack. Hence, the equivalent cell size for L stacks or layers can be expressed as $\frac{7.5SF^2}{L}$, where L denotes a quantity of stacks or layers of the memory array device.
FIG. 13 shows a table 1300 showing a relationship between a number of layers and an equivalent cell size. The number of layers is also referred herein as a quantity of stacks or layers, indicated as L. As shown in the table 1300, the equivalent cell size decreases as the layer number increases.

FIG. 14 shows a memory array device 1400 according to various embodiments. The figure provides a perspective view of the memory array device 1400 for illustrating an example of memory array routing and addressing scheme of the memory array device 1400. The memory array device may include an array of bit columns wherein each bit column is identical or at least substantially similar to the memory structure of FIG. 1 and FIGS. 8A-8B. Each bit column includes a conductive core 102 and a switching material layer 104. The array of bit columns may be arranged in a plurality of rows and a plurality of columns. The memory array device may include a plurality of bitlines 440 and a plurality of selector gate lines 442, wherein the plurality of selector gate lines 442 may be arranged perpendicular to the plurality of bitlines. Each bitline 440 may be coupled to a row of bit columns while each selector gate line 442 may be coupled to a column of bit columns. Each bit column may be coupled to a column selector 444 through an interconnect layer at a bottom of the each bit column. Each column selector 444 may be coupled to a respective bitline 440 and a respective selector gate line 442. The column selectors 444 may be transistors, for example, FETs including a drain terminal 1400, a gate terminal 1402 and a source terminal 1404. The gate terminal 1402 may include a metal gate material covering a gate oxide and a silicon channel. The column selectors 444 may be configured to select the bit column from the array of bit columns. The column selectors 444 may be vertical transistors or conventional horizontal transistors. The process of fabricating horizontal transistors may be easier, given the mature level of technology in the industry. In order to avoid addressing two adjacent cells which are coupled to a common bit column, the wordlines in each stack may be divided into two sets, for example a first set of wordlines 446 and a second set of wordlines 446'. The layout of each set of wordlines in a stack may be designed like a comb, in other words, arranged as a comb-shaped electrode. The two sets of wordlines may be arranged in an interdigitated (IDT) pattern such that each wordline of the first set of wordlines 446 may be alternately arranged with each wordline of the second set of wordlines 446'. Each set of wordlines of the first set of wordlines 446 and the second set of wordlines 446' may be individually controlled by a layer decoder. The layer decoder may be identical to or at least substantially similar to the layer decoder 448 of FIG. 4.
[0057] The memory array device may be operated in the following manner. A column selector 444 may be operated to apply voltage to a bitline 440 and a selector gate line 442. In doing so, one bit column can be addressed. The desired wordline 446 may be selected through the layer decoder so as to operate only one memory cell of the addressed bit column.

[0058] A memory array device according to various embodiments may have various advantages. The memory array device may include high quality diodes as access selectors, as the fabrication process allows for the access selectors to be fabricated separately from the memory cells. As such, the access selectors may be fabricated with good uniformity and large $W/W$ ratios, thereby enabling a high density memory array. The memory active size may be tunable and using the example of FIGS. 9 and 10, the memory active size may be made to be smaller than $0.5F^2$, where $F$ is a minimum feature size as limited by lithography. In other words, the tunable memory active size is not limited by the lithography process and as such, the lithography requirement may be relaxed. A small effective cell size per bit may be achieved by having a large number of stacks. For example, in the example of FIG. 12, with eight stacks, the effective cell size per bit can be as low as $0.94F^2$.

[0059] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced. It will be appreciated that common numerals, used in the relevant drawings, refer to components that serve a similar or the same purpose.
Claims

1. A memory structure comprising:
   a conductive core; and
   a switching material layer at least partially surrounding the conductive core,
   wherein the switching material layer comprises a plurality of sections, each
   section of the plurality of sections arranged at least substantially parallel to a height of
   the conductive core; and
   wherein each section comprises a plurality of cells, each cell of the plurality of
   cells arranged at a respective position along the height of the conductive core.

2. The memory structure of claim 1, wherein the plurality of cells of the plurality of
   sections comprises at least one of a resistive memory cell or a phase-change memory cell.

3. The memory structure of claim 1, wherein the switching material layer comprises at
   least one of a dielectric material or a phase-change material.

4. The memory structure of claim 1, further comprising:
   a plurality of access selectors,
   wherein each access selector of the plurality of access selectors is coupled to a
   respective cell of the plurality of cells of the plurality of sections.

5. The memory structure of claim 4, wherein each access selector of the plurality of
   access selectors comprises a diode.

6. The memory structure of claim 4, wherein the each access selector of the plurality of
   access selectors comprises a fin-like architecture.

7. A memory array device comprising:
   an array of bit columns,
   wherein each bit column of the array of bit columns comprises the memory
   structure of claim 1.
8. The memory array device of claim 7, wherein the array of bit columns are arranged in a plurality of rows and a plurality of columns.

9. The memory array device of claim 8, further comprising:
   a plurality of bitlines configured to select a row from the plurality of rows; and
   a plurality of selector gate lines configured to select a column from the plurality of columns.

10. The memory array device of claim 9, wherein each selector gate line of the plurality of selector gate lines is arranged perpendicular to each bitline of the plurality of bitlines.

11. The memory array device of claim 9, wherein each selector gate line of the plurality of selector gate lines and each bitline of the plurality of bitlines are arranged perpendicular to the conductive core.

12. The memory array device of claim 9, further comprising:
    a plurality of column selectors, each column selector of the plurality of column selectors coupled to a respective bitline and further coupled to a respective selector gate line.

13. The memory array device of claim 12, wherein the plurality of column selectors comprises at least one of a vertical transistor or a horizontal transistor.

14. The memory array device of claim 7, further comprising:
    a plurality of wordlines, wherein each wordline of the plurality of wordlines is coupled to a respective access selector of the plurality of access selectors.

15. The memory array device of claim 14, wherein the plurality of wordlines comprises a first set of wordlines coupled to a first section of the plurality of sections of each switching material layer; and a second set of wordlines coupled to a second section of the plurality of sections of each switching material layer.

16. The memory array device of claim 15, further comprising:
a layer decoder configured to select one from the group consisting of the first set of wordlines and the second set of wordlines.

17. The memory array device of claim 15, wherein the first set of wordlines is a first comb-shaped electrode and the second set of wordlines is a second comb-shaped electrode.

18. The memory array device of claim 17, wherein each of the first comb-shaped electrode and the second comb-shaped electrode comprises a plurality of comb teeth, wherein the comb teeth of the first comb-shaped electrode is arranged in between the comb teeth of the second comb-shaped electrode.

19. A method for fabricating a memory structure, the method comprising:
   providing a conductive core; and
   surrounding the conductive core with a switching material layer so that the switching material layer at least partially surrounds the conductive core;
   wherein the switching material layer comprises a plurality of sections, each section of the plurality of sections arranged at least substantially parallel to a height of the conductive core; and
   wherein each section comprises a plurality of cells, each cell of the plurality of cells arranged at a respective position along the height of the conductive core.

20. A method for operating a memory array device, the method comprising:
   addressing a bit column from an array of bit columns,
   wherein each bit column of the array of bit columns comprises
   a conductive core;
   a switching material layer at least partially surrounding the conductive core,
   wherein the switching material layer comprises a plurality of sections, each section of the plurality of sections arranged at least substantially parallel to a height of the conductive core;
   wherein each section comprises a plurality of cells, each cell of the plurality of cells arranged at a respective position along the height of the conductive core.
FIG. 1

Conductive core

Switching material layer

100

102

104

FIG. 2

Conductive core

Switching material layer

Access selectors

200

206
Provide a conductive core.

Surround the conductive core with a switching material layer so that the switching material layer at least partially surrounds the conductive core.

FIG. 5

Address a bit column from an array of bit columns.

FIG. 6
FIG. 12

<table>
<thead>
<tr>
<th>Layer No. (L)</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
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<tr>
<td>Equivalent cell size (F2)</td>
<td>7.5</td>
<td>3.75</td>
<td>2.5</td>
<td>1.88</td>
<td>1.5</td>
<td>1.25</td>
<td>1.07</td>
<td>0.94</td>
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FIG. 13
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

H01L 45/00 (2006.01)  H01L 27/24 (2006.01)  G11C 13/00 (2006.01)

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01 L; G 11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPDOC; WPI

resistive memory, phase change memory, 3D architecture, array, cross-bar, cross-point, vertical core, plurality of sections and cells, individual access selector, 1D-1 R structure, diode, comb-shaped electrodes, interdigital and related search terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>US 201 1/0272663 A1 (AN, H; ET AL) 10 November 2011 figures 1, 2 and 4-15; paragraphs [0034];[0082]</td>
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Date of the actual completion of the international search
30/09/2015 (day/month/year)

Date of mailing of the international search report
16/01/2015 (day/month/year)

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