Abstract: It is related to an apparatus and a method for manufacturing a semiconductor package. A retainer (24) for retaining a wafer (20) is disclosed. The wafer (20) having a top surface for forming an integrated circuit (IC) thereon and a bottom surface opposite to the top surface. The retainer (24) comprises an opening, a base portion (240) around the opening, and a positioning portion (242) connecting with the base portion. The base portion (240) is configured to support the bottom surface of the wafer, the positioning portion (242) is configured to transversely position the wafer (20), and the opening is configured to expose the bottom surface corresponding the valid area of the wafer. The method involves applying a flattening element (22) on the positioning portion (242) above the wafer (20) to flatten the wafer in an alloy process.
BACKGROUND OF THE INVENTION

[0001] 1. Field

[0002] The present invention relates generally to an apparatus and method for manufacturing a semiconductor package.

[0003] 2. Related Art

[0004] To achieve a thin integrated circuit (IC) package, one way is to reduce the thickness of the wafer. However, the thinner the wafer is, the more easily warping occurs.

[0005] One solution to solve this technical problem is to improve the wafer grinding process. For example, the grinding process, different from an entirely conventional grinding, when grinding a wafer, leaves an edge, approximately 3 mm on the outermost circumference of the wafer and only grinds the inner circumference thin.

SUMMARY OF THE INVENTION

[0006] Generally, wafer warpage results from differential stress between the top surface and the bottom surface of the wafer due to the IC formation near the top surface of the wafer. The wafer warpage causes poor alloy formation for a twofold reason: one is non-uniform metal thickness because the deposition equipment is designed to deposit metal on flat wafers, and the other is non-uniform heating at the alloying step, because the equipment is designed to heat flat wafers. In addition, the wafer warpage causes increased wafer breakage because the process equipment is designed to handle flat wafers. The poor alloy formation and wafer breakage both reduce the output of quality IC packages, which incurs greater expense and does not meet customers' requirements.
A wafer thinning process makes the above problems more acute. Thus, the inventor endeavors to achieve a unique alloy in a thin wafer, and avoid the thin wafer being broken during transfer.

Embodiments of the present invention can solve the above technical problem. Instead of using a special grinding machine during the grinding process, the present invention stacks a flattening element above a warped wafer to flatten the warpage, and they are fixed together by a retainer having an opening. The bottom surface of the flattening element faces the upper surface of the warped wafer and the bottom surface corresponding to the valid area of the warped wafer is exposed to the opening, so that the exposed bottom surface of the warped wafer can be subsequently sputtered with metal and alloyed. The flattening element and the retainer are made of materials of excellent heat conductivity and high temperature endurance to ensure that the wafer is uniformly heated during the alloying process.

One embodiment of the present invention provides a retainer to retain a wafer, the wafer having a top surface for forming an integrated circuit (IC) thereon and a bottom surface opposite to the top surface. The retainer comprises an opening, a base portion around the opening, and a positioning portion connecting with the base portion. The base portion is configured to support the bottom surface of the wafer, the positioning portion is configured to transversely position the wafer, and the opening is configured to expose the bottom surface corresponding to the valid area of the wafer.

Another embodiment of the present invention provides a method for manufacturing a semiconductor package. The method comprises placing the wafer on a retainer, and stacking a flattening element above the wafer, so that the bottom surface of the flattening element nestles up to the top
surface of the wafer to flatten the wafer; wherein the wafer and the flattening element are transversely positioned by the retainer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a perspective view illustrating a wafer, a flattening element to flatten the wafer and a retainer to retain it, and the flattening element according to one embodiment of the present invention;

[0012] FIG. 2 is a top view of the retainer in FIG.1;

[0013] FIG. 3 is a sectional view of the retainer along line "AA" in FIG.2;

[0014] FIG. 4 is a top view of a flattening element according to an embodiment of the present invention; and

[0015] FIG. 5 is a top view of a flattening element according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Embodiments of the present invention are illustrated as follows:

[0017] According to one embodiment of the present invention, a method for manufacturing a semiconductor package includes: placing a wafer on a retainer and stacking a flattening element above the wafer, so that the bottom surface of the flattening element nestles up to the top surface of the wafer to flatten the wafer. The wafer and the flattening element are both transversely positioned by the retainer. In this specification, the top surface of the wafer is defined for forming an IC thereon. The flattening element and the
retainer will not be removed until the alloy formation on the wafer is completed.

[0018] Generally, the flattening element used in the method provided by the present invention has a size, including the horizontal size (such as the diameter) and the vertical size (such as the thickness), ensuring that the flattening element has a weight capable of flattening wafer warpage. Preferably, the flattening element has an outline similar to the wafer, i.e., is shaped as a circle of similar diameter so that the flattening element and wafer can be retained by the retainer for the best performance costwise. At the same time, the roughness of the flattening element is low enough to protect the wafer from being scratched.

[0019] The retainer used in the method provided by the present invention has an opening, a base portion around the opening, and a positioning portion connected with the base portion. The base portion is configured to support the bottom surface of the wafer, the positioning portion is configured to transversely position the wafer, and the opening is configured to expose the bottom surface corresponding to the valid area of the wafer so that the exposed valid area of the wafer will be subject to the subsequent metal formation and alloy formation thereon. The valid area of the wafer means the area where a die is to be formed in the top surface of the wafer. In an embodiment, the valid area is the main area of a wafer except the edge, approximately 3 mm on the outermost circumference of the wafer. Preferably, the bottom surface corresponding to the valid area of the wafer is entirely exposed to the opening of the retainer.

[0020] Furthermore, the flattening element and the retainer are heat conductive and endure high temperatures, for example to 500°C, so that they can satisfy qualified metal and alloy formation, which are known to persons skilled in the art. For
example, the retainer can be made of, but not limited to, metal (such as aluminum) or ceramic, and the flattening element can be, but not limited to, a dummy wafer, a quartz wafer, or a metal cap.

[0021] Figure 1 is a perspective view illustrating a wafer 20, a flattening element 22 for flattening the wafer 20 and a retainer 24 for retaining the wafer 20 and the flattening element 22 according to one embodiment of the present invention, wherein the flattening element 22 and the retainer 24 can be used in the method as illustrated above.

[0022] In this embodiment, the flattening element 22 shown in FIG. 1 is a dummy wafer. The diameter of the flattening element 22 is substantially equivalent to the wafer 20. For example, for an 8-inch 100um thin wafer 20, the flattening element 22 can select an 8-inch 140um dummy wafer. When the flattening element 22 is stacked on the top surface 200 of the wafer 20, the weight of the flattening element 22 flattens the wafer warpage. In other embodiments of the present invention, the dummy wafer can be replaced with a quartz wafer or a metal cap.

[0023] FIG. 2 is a top view of the retainer 24 in FIG. 1, and FIG. 3 is a sectional view of the retainer 24 along line "AA" in FIG. 2.

[0024] As shown in FIGS. 2 and 3, in this embodiment, the retainer 24 is an aluminum ring, including an inner ring defined by the base portion 240 and an outer ring defined by the positioning portion 242. The diameter "DDI" of the base portion 240, i.e., the diameter of the opening 244 around the base portion 240, is less than that of the wafer 20 so that the base portion 240 can support the wafer 20, but equal to or larger than the valid diameter that defines the valid area of the wafer 20 so as to entirely expose the bottom surface corresponding to the valid area of the wafer 20. The diameter
"DDO" of the positioning portion 242 is equal to the larger one of the wafer 20 and the flattening element 22. The height "HH" of the positioning portion 242 is at least larger than the thickness of the wafer 20. The wafer 20 and the flattening element 22 are retained within the positioning portion 242.

[0025] To achieve a desirable metal formation and alloy formation, the base portion 240 may alternatively define a plurality of protrusions 241 for further suspending the wafer 20, according to the process conditions.

[0026] FIGS. 4 and 5 are respectively a top view of a flattening element 22 according to another two embodiments of the present invention.

[0027] Different from the dummy wafer and quartz wafer, the roughness of some metal caps, such as an aluminum cap, is difficult to control in the desired manner. To protect the top surface of the wafer 20 from being scratched, the metal cap selected as the flattening element 22 in the present invention may be shaped as being central-symmetrically hollow, such as crosswise as shown in FIG. 4, or spokewise as shown in FIG. 5. Since the contact area between the flattening element 22 and the wafer 20 decreases, the risk of the wafer 20 being scratched by the flattening element 22 decreases.

[0028] To achieve a better flattening effect, a plurality of bulges 220 are alternatively formed on the outer edge of flattening element 22. Correspondingly, the retainer 24 defines a plurality of recesses 243 on the positioning portion 242 as shown in FIG. 2, so that the plurality of bulges 220 are respectively held in the plurality of recesses 243.
CLAIMS

1. A retainer for retaining a wafer, the wafer having a top surface for forming an integrated circuit (IC) thereon and a bottom surface opposite to the top surface, the retainer comprising:
   an opening;
   a base portion around the opening; and
   a positioning portion connecting with the base portion;
   wherein the base portion is configured to support the bottom surface of the wafer, the positioning portion is configured to transversely position the wafer, and the opening is configured to expose the bottom surface corresponding to the valid area of the wafer.

2. The retainer of claim 1, wherein the retainer is heat conductive, and high temperature endurable.

3. The retainer of claim 1, wherein the retainer is made of metal or ceramic.

4. The retainer of claim 1, wherein at least one of the base portion and the positioning portion has the shape of a circle.

5. The retainer of Claim 1, wherein the base portion defines a plurality of protrusions for further suspending the wafer.

6. The retainer of Claim 1, wherein the height of the positioning portion is larger than the thickness of the wafer.

7. The retainer of Claim 1, wherein the retainer is an aluminum ring, including an inner ring defined by the base portion and an outer ring defined by the positioning portion.
8. A method for manufacturing a semiconductor package, the semiconductor package including a wafer having a top surface for forming an integrated circuit (IC) thereon and a bottom surface opposite to the top surface; the method comprising:

   placing the wafer on a retainer; and
   stacking a flattening element above the wafer, so that the bottom surface of the flattening element nestles up to the top surface of the wafer to flatten the wafer;

   wherein the wafer and the flattening element are transversely positioned by the retainer.

9. The method of Claim 8, wherein the flattening element and the retainer are heat conductive, and high temperature endurable.

10. The method of Claim 8, wherein the flattening element is a dummy wafer, a quartz wafer, or a metal cap.

11. The method of Claim 10, wherein the roughness of the dummy wafer is less than 0.005um.

12. The method of Claim 10, wherein the metal cap is an intact or central-symmetrically hollow metal slice.

13. The method of Claim 12, wherein the central-symmetrically hollow metal slice is spokewise.

14. The method of Claim 12, wherein the metal cap is an aluminum cap.

15. The method of Claim 8, wherein the retainer is an
aluminum ring, including an inner ring supporting the wafer portion and an outer ring positioning the wafer and the flattening element.

16. The method of Claim 8, wherein the retainer further defines a plurality of recesses for positioning a plurality of bulges formed on the outer edge of the flattening element.

17. The method of claim 8, wherein the retainer is made of metal or ceramic.

18. The method of Claim 8, further including removing the flattening element and retainer after forming an alloy in the bottom surface of the wafer.

19. The method of Claim 8, wherein the retainer comprising:

   an opening;

   a base portion around the opening; and

   a positioning portion connecting with the base portion;

   wherein the base portion is configured to support the bottom surface of the wafer, the positioning portion is configured to position the wafer and the flattening element, and the opening is configured to expose the bottom surface corresponding to the valid area of the wafer.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
H01L 21/02 (2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI,CNPAT:EPDOC;CNKH:IEEE: substrate, lid, wafer, tilt+, support, base, flat+, plate, inner, opening, coat, warp+, dummy, position, heat, window, ring, retainer, stress, tray, cover, outer, annealing, alloy

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>US 2009250955 A1 (APPLIED MATERIALS INC.) 08 October 2009 (2009-10-08)</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:
A - document defining the general state of the art which is not considered to be of particular relevance
E - earlier application or patent but published on or after the international filing date
L - document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
O - document referring to an oral disclosure, use, exhibition or other means
P - document published prior to the international filing date but later than the priority date claimed

- later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- document member of the same patent family

Date of actual completion of the international search 01 September 2014
Date of mailing of the international search report 09 October 2014

Name and mailing address of the ISA/
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA(ISA/CN)
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ZHOU,Zhongtang

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Form PCT/ISA/210 (second sheet) (July 2009)
This International Searching Authority found multiple inventions in this international application, as follows:

[1] This Authority considers that there are two inventions covered by claims 1-19 indicated as follows:

[2] I: Claims 1-7 directed to a retainer for retaining a wafer;


[4] The common technical features between the above two inventions are as follows: a wafer with top and bottom surface, and forming an integrated circuit on the top surface, while, these features are well-known in the art.

Therefore, it follows that the above common technical features do not make a contribution over the prior art and can not be considered as special technical features within the meaning of Rule 13.2 PCT. The application, hence does not meet the requirement of unity of invention as defined in Rule 13.1 PCT.

1. □ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ □ ] As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. [ □ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ □ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

[ □ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

[ □ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

[ □ ] No protest accompanied the payment of additional search fees.
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