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(54) Title: METHODS AND APPARATUS FOR POWER FACTOR CORRECTION AND REDUCTION OF DISTORTION IN AND NOISE IN A POWER SUPPLY DELIVERY NETWORK

(57) Abstract: Methods and apparatus for reducing distortion in a power delivery system include a means for determining distortion in a power line, forming a corrective signal according to the distortion, digitally processing the distortion and selectively sinking and sourcing current to the power line according to the corrective signal. Furthermore, power for a solar power system is injected into a load via the same apparatus in a multi phase power system.
— with information concerning one or more priority claims considered void (Rule 26bis.2(d))
METHODS AND APPARATUS FOR POWER FACTOR CORRECTION AND
REDUCTION OF DISTORTION IN AND NOISE IN A POWER SUPPLY DELIVERY
NETWORK

Cross-Reference to Related Applications

docket RADA-00401, all of which are hereby incorporated by reference in its entirety for all purposes.

Field of the Invention

The present invention relates to the field of power electronics. More specifically, the
present invention relates to reducing distortion and noise of power delivered to or generated
by a load and improving power factor.

Background of the Invention

Power factor correction is an important component of increasing efficiency of modern
day power delivery systems. Due to reactive components in the loads that consume power
such as appliances that include a motor, a phase shift develops between a current and a
voltage component of a power signal. The power factor of an AC electric power system is
defined as the ratio of the real power flowing to the load to the apparent power and is a
number between 0 and 1 (frequently expressed as a percentage, e.g. 0.5 pf = 50% pf). Real
power (P) is the capacity of the circuit for performing work in a particular time. Apparent
power (S) is the product of the current and voltage of the circuit. The Reactive Power (Q) is
defined as the square root of the difference of the squares of S and P. Where reactive loads
are present, such as with capacitors or inductors, energy storage in the loads result in a time
difference between the current and voltage waveforms. During each cycle of the AC voltage,
extra energy, in addition to any energy consumed in the load, is temporarily stored in the load
in electric or magnetic fields, and then returned to the power grid a fraction of a second later
in the cycle. The "ebb and flow" of this nonproductive power increases the current in the
line. Thus, a circuit with a low power factor will use higher currents to transfer a given
quantity of real power than a circuit with a high power factor. A linear load does not change
the shape of the waveform of the current, but may change the relative timing (phase) between
voltage and current. Generally, methods and apparatus to correct power factor have involved
coupling a fixed corrective load having a known reactive value to a power line. The fixed
capacitive reactive load counteracts the reactive effect of inductive loads vice versa.
improving the power factor of the line. However, a fixed reactive load is only able to correct the power factor of a power line by a fixed amount to a certain extent because the power factor may be dynamic due to the changing nature of loads that are coupled and decoupled to the power line. To that end, later developments included several fixed reactive loads that may be selectively coupled to a power line in order to correct power factor. However, such systems require monitoring by an operator who must continually monitor the power factor in order to couple and decouple fixed reactive loads in order to counteract the ever changing power factor of the power line.

The changing landscape of electronics has introduced other inefficiencies in the delivery of power. The increased use of personal electrical appliances has caused an increase in the use of wall mounted AC-DC converters to supply power to devices and recharge the batteries of everyday items such as laptops, cellular telephones, cameras, and the like. The ubiquity of such items has caused users to have several of these converters, known as "wall warts" to be coupled into power systems. The two most common AC-DC converters are known as linear converters and switched mode converters. Linear converters utilize a step down transformer to step down the standard 120V power available in US residences to a desired AC voltage. A bridge rectifier rectifies that voltage. The bridge rectifier is generally coupled to a capacitor. Generally, this capacitor is of a high value. The capacitor forms a counter electromotive force. The capacitor forms a near DC voltage as it is charged and discharged. However, as it is charged, the capacitor draws current only a fraction of the cycle by the non linear bridge rectifier. As a result, the current waveform does not match the voltage and contains a heavy harmonic distortion component. Total harmonic distortion (THD) is the sum of the powers of all harmonic components to the power of the fundamental frequency. This harmonic distortion may be reflected back into the power network.

A switching power supply works on a different principle but also injects harmonics into a power delivery network. In general, a switched mode power supply operates by rectifying the 120V voltage available in US residences. The rectification against a counter electro motive force, such as a big reservoir capacitor, again adds harmonics and distortion. Also, the widespread adaptation of various types of linear or switch mode integrated circuits cause the system to create electrical noise. Furthermore, reactive components in the
alternating current network degrades power factor, and integrated circuits cause harmonics and noise to be reflected into the power line. These harmonics manifest as harmonic distortion in the current component of a power signal. Because the power network has a nonzero impedance, distortion along the current component may also translate to amplitude distortion. Amplitude distortion is distortion occurring in a system, subsystem, or device when the output amplitude is not a linear function of the input amplitude under specified conditions. Other undesirable effects are also formed, such as power factor distortion and overall reduction of energy transfer. Such effects decrease efficiency and reduce quality in the delivery of power. To that end, what is needed are methods and apparatus capable of not only correcting a power factor in a power delivery network, but also reducing or eliminating distortion in a power line, thereby allowing for maximum efficiency and quality in power delivery. As a result, overall energy consumption may be reduced.

Summary of the Invention:

The invention provided herein allows for increasing efficiency and quality of power delivery over a power network to a load. The person of ordinary skill having the benefit of this disclosure will appreciate that the methods and apparatus discussed herein may be applied to a great variety of loads having reactive and non linear components that cause a less than perfect power factor and cause distortion and noise and the like to be injected back into the power network. In some applications, the load is a family residence. The load is a parallel combination of all appliances drawing power within the residence. To the grid, through a power meter, the residence appears to be one dynamic load having changing reactive and non linear properties as users within the residence activate and deactivate appliances. Advantageously, the invention provided herein overcomes prior art solutions inherent drawbacks such as prohibitive cost, complicated installation at multiple locations, fixed PF compensation that may over or under compensate and reduce PF, and poor performance. The invention provided herein is able to correct a power factor to a load by dynamically measuring a reactive power component of the load, and coupling at least one corrective reactive load. As the reactive power changes, such as when a washing machine is activated, the invention is able to recognize that the characteristic of the load has changed,
and is able to couple or decouple other corrective reactive loads to the load causing the poor power factor. Furthermore, the invention provided herein is able to correct distortion, noise, and the like in the power delivered by a network to a load, thereby improving the quality of the power. The invention provides for comparing an electrical signal having distortion, noise, or the like to a reference signal. The electrical signal maybe the current component of the power delivered to a load through a network. The reference signal may be derived from a voltage component of the power delivered to a load, or be synthesized separately but synchronized with the voltage waveform. A corrective signal is derived by comparing, or subtracting, the reference signal from the signal having distortion. The corrective signal comprises the distortion. Current is sunk or sourced from the signal having distortion according to the corrective signal, resulting in reduced distortion. Advantageously, the invention is able to correct distortion caused by all non linear loads in a residence at one point. The invention is able to be coupled between a utility meter and the residence. As a result, the invention is agnostic to the number of appliances in the residence, their location, or any other parameter. Also, the invention is energy efficient since it improves distortion and PF as necessary without increasing PF or distortion and without the addition of any other electrical load within the property network.

In one aspect of the invention, a method of reducing distortion in an electrical signal having distortion comprises sensing a distortion in the electrical signal having distortion and combining a factor of the distortion with the electrical signal having distortion. In some embodiments, the sensing step comprises comparing the electrical signal having distortion to a reference signal to obtain a difference signal and scaling the difference signal to form the factor of the distortion. The combining step comprises subtracting the factor of the distortion from the electrical signal having distortion if the factor of the distortion is positive and adding the factor of the distortion to the electrical signal having distortion if the factor of the distortion is negative. In some embodiments, the subtracting step comprises applying the factor of the distortion to a first controlled current source coupled to the electrical signal having distortion and the adding step comprises applying the factor of the distortion to a second controlled current source coupled to the electrical signal having distortion. Applying the factor of the distortion to a first controlled current source further comprises applying a
power factor corrected positive power signal to the first controlled current source and applying the factor of the distortion to a second controlled current source further comprises applying a power factor corrected negative power signal to the second controlled current source.

In some embodiments, the combining step comprises modulating the factor of the distortion. The factor of the distortion is then added to the electrical signal having distortion if the factor of the distortion is negative and subtracting the factor of the distortion from the electrical signal having Distortion if the factor of the distortion is positive. The adding and subtracting step are able to be achieved by applying the factor of the distortion to a first switch coupled to the electrical signal having Distortion and applying the factor of the distortion to a second switch coupled to the electrical signal having Distortion. Modulating the factor of distortion can include pulse width modulation, delta-sigma modulation, pulse code modulation, pulse density modulation, or pulse position modulation. Applying the factor of the distortion to a first switch includes applying a power factor corrected positive power signal to the first switch and applying the factor of the distortion to a second switch includes applying a power factor corrected negative power signal to the second switch. Advantageously, the use of modulation techniques allows for highly efficient control of the switches. In some embodiments, analog or digital filters maybe included for filtering away the modulating signal.

In some applications, an impedance of the power network may be far lower than the impedance of the load that the power network is delivering power to. In such circumstances, it will be appreciated by persons having the benefit of this disclosure that the direction of sourcing or sinking current may need to be reversed. By way of example, a negative distortion is regularly corrected by injecting or sourcing current into the power line. However, if the impedance of the load is greater than the impedance of the network, the current will be injected into the network rather than the load. As a result, the opposite function may be done. This leads to adequate distortion correction of the total current waveform drawn from the grid.

In another aspect of the invention, a method for reducing distortion in a power line comprises correcting a power factor in the power line such that the power factor is
substantially one, comparing a current portion of the power line to a desired reference signal, thereby forming a corrective signal, and selectively sinking and sourcing current to the power line according to the corrective signal. Correcting a power factor comprises any known method of power factor correction or any method described herein. In some embodiments, selectively sinking or sourcing current comprises applying the corrective signal to at least one controlled current source, wherein the controlled current source couples a current supply with the power line according to the corrective signal. Alternatively, selectively sinking or sourcing current comprises modulating the corrective signal and applying the modulated corrective signal to at least one switch, wherein the switch couples a current supply with the power line and filtering modulation noise. Modulating the corrective signal comprises any among pulse width modulation, delta-sigma modulation, pulse code modulation, pulse density modulation, or pulse position modulation.

In some applications, an impedance of the power network may be far lower than the impedance of the load that the power network is delivering power to. In such circumstances, it will be appreciated by persons having the benefit of this disclosure that the direction of sourcing or sinking current may need to be reversed. Byway of example, a negative distortion is regularly corrected by injecting or sourcing current into the power line. However, if the impedance of the load is greater than the impedance of the network, the current will be injected into the network rather than the load. As a result, the opposite function may be done. This leads to adequate distortion correction of the total current waveform drawn from the grid.

In operation, distortion in electrical signals, such as the power being delivered to a residence, is reduced. The distortion maybe harmonic distortion, amplitude distortion, noise, elevated spectral noise, or the like. The power being delivered to a residence comprises a voltage and a current. Generally, the current component of the power delivered to a load will display distortion due to non linearities in the load. The distortion is able to be ascertained by comparing the current to a perfect sine wave, such as the voltage component of the power. This perfect sine wave is able to function as a reference signal. In cases where the voltage sinewave is less than perfect, such as when amplitude distortion has distorted the voltage sinewave, a near perfect sinewave is able to be created locally by synchronizing with the
voltage sinewave. For example, zero crossing transitions may be utilized as markers to form a near perfect sinewave. By subtracting the reference signal from the signal having distortion, a corrective signal is formed. The corrective signal comprises a factor of the distortion. A positive portion of the distortion is applied to a current sink coupled to the lines delivering power to the residence. The current sink sinks current out of the line according to the distortion. Similarly, a negative portion of the distortion is applied to a current source that is also coupled to the lines delivering power to the residence. When the distortion is negative, the current source sources current into the line according to the distortion. As a result, the distortion is removed from the current being drawn from the grid.

In some embodiments, the corrective signal may be modulated in order to enhance efficiency. Methods such as pulse width modulation, delta-sigma modulation, pulse code modulation, pulse density modulation, or pulse position modulation. The modulated corrective signal is applied to an active switch, such as a MOSFET, that conducts current into or away from the line providing power to the house according to the distortion.

In some embodiments, the method of reducing distortion further comprises correcting a power factor. A method of dynamic power factor correction comprises determining the reactive power of the first load, determining a power factor resulting from that reactive power, determining an optimum corrective reactive load to be coupled to the first load to bring the ratio to substantially one and coupling the optimum corrective reactive load to the first load.

In some embodiments, coupling the optimum reactive load to the first load includes selecting a quantization level for a desired accuracy, the quantization level having an MSB and an LSB, determining an MSB reactive load determining an LSB reactive load, and closing switches associated with any bit required to achieve the desired accuracy, wherein the switches electrically couple any among the MSB reactive load and LSB reactive load to the first load. Generally, the desired accuracy comprises determining an acceptable value for the ratio. The quantization level is able to further comprise at least one bit between the MSB and LSB. Determining a value for the LSB reactive load, MSB reactive load, and a bit reactive load of the at least one bit includes determining a maximum reactive component of the first load. The MSB reactive load, LSB reactive load, and bit reactive load of the at least one bit is
generally, a capacitor and may be coupled to the reactive load via any among a switch, an active switch, a MOSFET, an IGBT transistor, a pair of MOSFETs, a pair of IGBT transistors, a TRIAC, a relay, a thyristor, and a pair of thyristors. In some embodiments, the reactive power is continually monitored and a new optimum corrective reactive load to be coupled to the first load to bring the reactive power to substantially zero, and the power factor to substantially one, is dynamically determined.

In another aspect of the invention, a system for reducing distortion in an electrical signal having distortion comprises a power factor correcting module for bringing a power factor in the signal having distortion to substantially one, a substracter for comparing a current portion of the power line to a desired reference signal, thereby forming a corrective signal, and an electric circuit for selectively sinking and sourcing current to the power line according to the corrective signal. The power factor correcting module comprises a sensor for measuring the reactive power of a first load coupled to power line and a plurality of bit reactive loads for coupling with the first load to counteract a reactive component of the first load. In some embodiments, the electric circuit for selectively sinking or sourcing current is configured to apply the corrective signal to at least one controlled current source, wherein the controlled current source couples a current supply with the power line according to the corrective signal. Alternatively, the electric circuit for selectively sinking or sourcing current comprises a modulator for modulating the corrective signal and applying the modulated corrective signal to at least one switch, wherein the switch couples a current supply with the power line and a filter for filtering modulation noise. The modulator comprises any among a pulse width modulator, delta-sigma modulator, pulse code modulator, pulse density modulator, or pulse position modulator.

In operation, an electrical circuit for reducing distortion in a current signal having distortion comprises a first input for receiving the current signal having distortion, a second input for receiving a reference signal, a substracter coupled to the first input and second input for subtracting the current signal having distortion from the reference signal thereby forming a first corrective signal, and a circuit for selectively combining a positive portion of the first corrective signal and a negative portion of the first corrective signal with the current signal having distortion. The substracter is able to be an analog circuit, such as an operational
amplifier configured to subtract one input from another. Alternatively, the substracter may be
a digital system, such as a A/D converter capable of digitally subtracting one converted
bitstream input from another, and a D/A converter for converting the result to an analog
signal comprising the corrective signal.

In some embodiments, the circuit for selectively combining is able to be a positive
rectifier coupled to an output of the substracter for determining the positive portion of the
corrective signal and a first controlled current source, and a negative rectifier coupled to an
output of the substracter for determining the negative portion corrective signal and a second
controlled current source. Both controlled current sources are coupled to a positive power
supply and a negative power supply respectively in order to selectively sink or source current
to or from a main power line in order to correct distortion. In operation, when the distortion
is negative, current is sourced to a power supply line according to the negative distortion to
compensate. Likewise, when the distortion is positive, current is sunk away according to the
positive distortion, thereby compensating.

Alternatively, the circuit for selectively combining is able to be a positive trigger
comparator coupled to an output of the substracter for determining a positive portion of the
corrective signal, a negative trigger comparator coupled to the output of the substracter for
determining a negative portion of the corrective signal and a modulator. The modulator is
able to be any useful type of modulator, including a pulse width modulator, a delta-sigma
modulator, a pulse code modulator, a pulse density modulator, or a pulse position modulator.
The modulator is able to be coupled to an output of the positive trigger comparator and an
output of the negative trigger comparator for modulating any among the positive portion of
the corrective signal and the negative portion of the corrective signal. In some embodiments,
a first switch is coupled to positive trigger comparator. The first switch is able to selectively
couple current from a negative DC power supply according to the positive portion of the
corrective signal, thereby reducing distortion. Likewise, the second switch is able to
selectively couple current from a positive DC power supply according to the positive portion
of the corrective signal, thereby reducing distortion.

In some applications, an impedance of the power network may be far lower than the
impedance of the load that the power network is delivering power to. In such circumstances,
it will be appreciated by persons having the benefit of this disclosure that the direction of sourcing or sinking current may need to be reversed. By way of example, a negative distortion is regularly corrected by injecting or sourcing current into the power line. However, if the impedance of the load is greater than the impedance of the network, the current will be injected into the network rather than the load. As a result, the opposite function may be done. By sinking current from the power line, current is injected in the opposite direction.

In some embodiments, the electrical circuit for reducing distortion further comprises a power factor correction circuit for bringing the power factor between the current and the voltage being delivered to substantially unity. A system for power factor correction comprises means for determining the reactive power of a load, means for determining an optimum corrective reactive load to be coupled to the first load to bring the power factor to substantially one and the reactive power to substantially zero, and means for coupling the optimum reactive load to the first load. In some embodiments, the means for coupling the optimum reactive load to the first load comprises means for selecting a quantization level for a desired accuracy, the quantization level having an MSB and an LSB, means for determining an MSB reactive load, means for determining an LSB reactive load, and means for closing switches associated with any bit required to achieve the desired accuracy, wherein the switches electrically couple any among the MSB reactive load and LSB reactive load to the first load. The quantization level further comprises at least one bit between the MSB and LSB. More bits between the MSB and LSB will result in greater accuracy of power factor correction, or a power factor substantially closer to one. The bit reactive loads are generally a capacitor, and may be coupled to the reactive load via a switch, an active switch, MOSFET, an IGBT transistor, a pair of MOSFETs, a pair of IGBT transistors, a TRIAC, a relay, a thyristor, and a pair of thyristors.

In another embodiment of the invention, a system for reducing distortion in an electrical signal having distortion comprises an electric circuit for comparing at least a portion of the electrical signal having distortion in a power line to a desired reference signal, thereby forming a corrective signal; and an electric circuit for selectively sinking and sourcing current from one of a DC rectifier and a solar panel to the electrical signal having distortion.
according to the corrective signal to correct the distortion; and selectively injecting additive
current from the solar panel into at least one of a load or a power grid. Preferably, the system
further comprises a processor for determining when the solar power is generating current and
a processor for switching between the DC rectifier and the solar panel for sinking and
sourcing current, which may be the same processing unit. Also, the system comprises a
transformer, the transforming having a primary winding and a secondary winding, for
galvanically isolating the electric circuit for selectively sinking and sourcing from the power
line, wherein the secondary may be coupled in series or in parallel. Preferably, the electric
circuit for selectively sinking or sourcing current comprises a positive DC power supply
selectively coupled to one of the DC rectifier and the solar panel or providing a positive DC
current, a negative DC power supply selectively coupled to one of the DC rectifier and the
solar panel for providing a negative DC current, a processor for selectively sourcing current
into the power line from one of the positive DC power supply in response to a negative
distortion; or sinking current from the power line to the negative DC power supply in
response to a positive distortion, which again can the same processor mentioned above.

Similarly, a method of correcting a harmonic distortion in a power line comprises
generating a corrective signal as discussed above, generating positive DC current from one of
a rectifier and a solar power system, generating a negative DC current by inverting the
positive DC current, selectively sourcing the positive DC current into a load according to the
corrective signal to correct a negative distortion, selectively sourcing the negative DC current
into a load according to the corrective signal to correct a positive distortion, and injecting
additional available power into at least one of the load and the power line from the solar
power system, thereby increasing total current. Preferably, the method also comprises
galvanically isolating the load from the positive DC power supply and negative DC power
supply. In some embodiments, generating positive DC current from one of a rectifier and a
solar power system comprises determining whether the solar power system is generating
current, and sourcing current from the solar power system if the solar power system is
generating, or sourcing current from the rectifier if the solar power system is not generating
current. Advantageously, the method and apparatus mentioned allow for injection of current
from a solar power system without the use of a costly and inefficient inverter, as will be
explain in detail below.

In another aspect of the invention, a system for correcting harmonic distortion comprises means for determining the harmonic energy in a power line means for storing the harmonic energy, and means for selectively releasing the harmonic energy to counter harmonic energy of an opposite magnitude. Preferably, the means for determining the harmonic energy in a power line is as described above, including a sensor for measuring a current component in a power line, an oscillator for generating a reference signal, and a comparator for comparing the current component to the reference signal there by generating a corrective signal, wherein the corrective signal represents harmonic energy in the power line. The means for storing energy can be a capacitor or inductor. The energy is released by a switch, which selectively couples the means for storing harmonic energy between any among a positive power supply, a negative power supply, and a load. Preferably, the system further comprises a modulator to modulate the corrective signal to drive a transistor to selectively charge the means for storing energy.

Likewise, a method of correcting harmonic distortion in a signal having harmonic distortion comprises determining the harmonic energy in a power line, storing the harmonic energy, and selectively releasing the harmonic energy to counter harmonic energy of an opposite magnitude. The corrective signal is generated as described above, and the energy is stored and released as described above. As can be appreciated, using harmonic energy to correct future harmonic error saves from using an external power source to correct the energy, or drawing greater current from a power line.

In another embodiment, modulation of the power supplies is contemplated. Such an embodiment comprises means for comparing at least a portion of the electrical signal having distortion in a power line to a desired reference signal, thereby forming a corrective signal, means for selectively sinking and sourcing current to the electrical signal having distortion from a negative power supply and a positive power supply respectively, means for modulating the positive power supply according the corrective signal, and means for modulating the negative power supply according to the corrective signal. In analog electronics, such a power supply is referred to as a Class H amplifier. Class H amplifiers enjoy greater efficiency since the power supply closely tracks the current stage of an
amplifier. In this implementation, the power supply tracks the corrective signal. Preferably, the means for comparing comprises a sensor for sensing the signal having distortion, an oscillator for generating a reference signal, and a comparator for comparing the signal having distortion to the reference signal thereby generating a corrective signal. The means for selectively sinking and sourcing current comprise a first transistor coupled to the positive power supply for sourcing current to correct a negative harmonic according to the corrective signal, and a second transistor coupled to the negative power supply for sinking current to correct a positive harmonic according to the corrective signal. The means for modulating the power supplies comprises a first transistor for receiving the corrective signal and an LC-flywheel network for deriving a positive and a negative average of the corrective signals respectively.

In another aspect of the invention, a system for reducing distortion in a signal having distortion in a power delivery system comprises an input for receiving the signal having distortion, a first analog to digital converter for converting the signal having distortion into a digital signal having distortion, a frequency generator for generating a reference signal according to the signal having distortion, a second analog to digital converter for converting the reference signal into a digital reference signal, a processor for generating a corrective signal based upon the digital signal having distortion and the digital reference signal, and an electric circuit for selectively sinking and sourcing current to the signal having distortion according to the corrective signal to correct the distortion. The frequency generator generates a frequency, based upon an RMS value of the signal having distortion, a frequency of the signal having distortion, the frequency at which the power delivery system operates, or any combination of the above. In some embodiments, the processor comprises inputs for receiving the digital signal having distortion and the digital reference signal, a substracter for subtracting the digital reference signal from the digital signal having distortion, thereby forming a digital corrective signal and a digital to analog converter for converting the digital corrective signal to the corrective signal. Alternatively, the processor comprises a transform block for applying a transform function to the digital signal having distortion, thereby forming a transformed digital signal having distortion, a substracter for subtracting the digital reference signal from the transformed digital signal having distortion, thereby forming a
transformed corrective signal and an inverse transform block for applying an inverse of the transform function to the transformed digital corrective signal thereby forming the corrective signal.

In some embodiments, the signal having distortion is periodic. In such embodiments, the processor comprises a substracter for subtracting the digital reference signal from the digital signal having distortion, thereby forming a error signal, a memory bank having N rows and M columns, a sequencing means for writing the error signal line by line to a memory bank, an first array of logic gates for reading the memory bank column by column, thereby forming an M length portion of the digital corrective signal, a register for storing an M length string of the digital corrective signal, and a digital to analog converter for converting the M length string of the digital corrective signal to the corrective signal. N can be a number of samples taken in one period of the signal having distortion and M can be a number of periods of the signal having distortion sampled. Preferably, the processor further includes an array of N controllers, wherein each controller is configured to compare a sample of a first period to a corresponding sample in a second period. Each controller is configured to keep a value of a sample a difference between a sample of a first period and a corresponding sample in a second period is within an acceptable range.

Still alternatively, a processor can be configured to generate a corrective signal without the use of a reference signal. The processor can be configured to receive the transformed degraded signal and remove the fundamental frequency, leaving only the harmonics, then multiply the harmonics by a negative number, thereby forming a transformed corrective signal. An inverse transform block can be provided to form a corrective signal therefrom. Methods executed by the apparatus and systems described above are also contemplated. Greater detail regarding such embodiments is found in Figures 15D-15F and the supporting text in the detailed description of the drawings below.

Another aspect of the invention is directed toward power systems having multiple phases. In one embodiment, a multi phase power delivery system includes a phase line, a neutral line and a split phase line. Other phase lines are also contemplated. In such a power delivery system, a system for reducing distortion in an electrical signal having distortion comprises a first equivalent load coupled between the phase and neutral lines, a second
equivalent load coupled between the neutral and split phase lines and a third equivalent load coupled between the phase and split phase lines. The first, second and third loads represent different loads in a residence or commercial property coupled to the power network in a variety of ways. To correct distortion caused by those loads, a first processor for comparing at least a portion of a first electrical signal having distortion resulting from the first load to a reference signal, thereby forming a first corrective signal and a first circuit for selectively sinking and sourcing current to the first load according to the corrective signal to correct the distortion are provided. Specifically, to correct the distortion caused by the second load, a second processor for comparing at least a portion of a second electrical signal having distortion resulting from the second load to the reference signal, thereby forming a second corrective signal and a second circuit for selectively sinking and sourcing current to the second load according to the second corrective signal to correct the distortion. Similarly, a third processor for comparing at least a portion of a third electrical signal having distortion resulting from the third load to the reference signal, thereby forming a third corrective signal and a third circuit for selectively sinking and sourcing current to the third load according to the third corrective signal to correct the distortion can be included. Any among the first circuit, second circuit and third circuit selectively source and sink current from a DC power supply or a solar power assembly. To that end, a processor for determining when the solar power assembly is generating current and switching between a DC rectifier and the solar panel for sinking and sourcing current can be included. The several circuits can be galvanically isolated from the loads. Alternatively, each of the first circuit, second circuit and third circuit is galvanically isolated from the DC power supply. Preferably, any among the first circuit, second circuit and third circuit is coupled to at least one controlled current source, wherein the controlled current source couples one of the DC rectifier and the solar panel with the power line according to the first, second and third corrective signals respectively. Greater detail can be seen below in Figures 13D-13F and the supporting text.

The corresponding method for the above embodiment comprises forming a corrective signal as previously discussed, selectively sinking and sourcing current to the electrical signal having distortion from a negative power supply and a positive power supply respectively, and modulating the power supplies according to the corrective signal. Processors discussed
herein can be a monolithic commercially available DSP device, a plurality of standalone processors, FPGAs, or the like.

Advantageously, the embodiments summarized above are able to be implemented on the scale of a family residence. The systems and circuits summarized above are able to be produced inexpensively, allowing average homeowners access to such devices. Prior art solutions generally include devices that are either targeted for industrial applications, and therefore are configured to correct power factor in networks of far greater current carrying capacity. As a result, they are very large and cost many thousands of dollars and are not amenable to residential applications. Other solutions merely correct power factor and must be applied to individual devices within a home. Furthermore, they are generally fixed capacitor power factor correction units that do not adequately correct a power factor, and may in some instances degrade power factor. Still other solutions are systems wherein a central control unit drives power factor and harmonic correction units that must be coupled to individual appliances, wherein each coupling is an installation step. Such systems also attempt to correct current waveforms by drawing and dissipating current in a purely resistive load, such as an individual appliance. Conversely, the systems and circuits and methods implemented therein are generally to be coupled between a main utility meter and the home, allowing for simple, one step installation.

Brief Description of the Drawings:

FIG. 1 is a schematic block diagram of a power factor correction circuit per an embodiment of this invention.

FIG. 2 is a schematic block diagram of a power factor correction circuit per an embodiment of this invention.

FIG. 3A is a time vs. amplitude graph of a power factor corrected power signal having distortion.

FIG. 3B is a time vs. amplitude graph of a power factor corrected power signal having distortion.

FIG. 3C is a time vs. amplitude graph of a power factor corrected power signal having distortion.
FIG. 3D is a time vs. amplitude graph of a power signal having a poor power factor, distortion and methods of correction of distortion.

FIG. 4 is a schematic block diagram of a distortion reducing circuit per an embodiment of this invention.

FIG. 5 is a schematic block diagram of a distortion reducing circuit having modulation per an embodiment of this invention.

FIG. 6 is a schematic block diagram of a distortion reducing circuit having modulation per an embodiment of this invention.

FIG. 7 is a schematic block diagram of a distortion reducing circuit having modulation and enhanced filtering per an embodiment of this invention.

FIG. 8 is a schematic block diagram of a distortion reducing circuit having modulation and enhanced filtering per an embodiment of this invention.

FIG. 9 is an alternate schematic block diagram of a distortion reducing circuit having modulation and enhanced filtering per an embodiment of this invention.

FIG. 10 is a schematic block diagram of a distortion reducing circuit having modulation and enhanced filtering and galvanic isolation per an embodiment of this invention.

FIG. 11 is a schematic block diagram of a distortion reducing circuit having modulation and enhanced filtering and galvanic isolation coupled in series with a load, per an embodiment of this invention.

FIG. 12A is an example of a Class G power supply waveform.

FIG. 12B is an example of a Class H power supply waveform.

FIG. 12C is a schematic block diagram of a distortion reducing circuit having Class H power supplies.

FIG. 12D is an enhanced schematic block diagram of a distortion reducing circuit having Class H power supplies.

FIG. 13A is a schematic block diagram of a distortion reducing circuit having a solar power system.

FIG. 13B is a schematic block diagram of a prior art solar power system.

FIG. 13C is a graphical representation of current generated by a solar power system.
injected into a property load or AC power grid.

FIG. 13D is a schematic block diagram of a distortion reducing circuit for a multi phase power system having a solar power system.

FIG. 13E is an alternative schematic block diagram of a distortion reducing circuit for a multi phase power system having a solar power system.

FIG. 13F is yet another alternative schematic block diagram of a distortion reducing circuit for a multi phase power system having a solar power system.

FIG. 14A is a schematic block diagram of a distortion reducing circuit having the ability to recycle harmonic energy and use it to correct later harmonic distortion.

FIG. 14B is a graphical representation of energy in a distorted current signal that can be recycled for later use to correct harmonic distortion.

FIG. 14C is a schematic block diagram of a distortion reducing circuit having the ability to recycle harmonic energy and use it to correct later harmonic distortion.

FIG. 14D is a schematic block diagram of a distortion reducing circuit having the ability to recycle harmonic energy and use it to correct later harmonic distortion.

FIG. 15A is a schematic block diagram of a distortion reducing circuit having digital processing capability.

FIG. 15A′ is a schematic block diagram of a distortion reducing circuit having digital processing capability.

FIG. 15B is an exemplary periodic distorted electrical signal in graphical form.

FIG. 15C is an alternative schematic block diagram of a distortion reducing circuit having digital processing capability.

FIG. 15D is yet another an alternative schematic block diagram of a distortion reducing circuit having digital processing capability.

FIG. 15E is yet another an alternative schematic block diagram of a distortion reducing circuit having digital processing capability.

FIGS 15F- 15H are process diagrams for reducing distortion by digital processing.

Detailed Description of the Drawings

In the following description, numerous details and alternatives are set forth for the
purpose of explanation. However, one of ordinary skill in the art having the benefit of this disclosure will realize that the invention can be practiced without the use of these specific details. In other instances, well-known structures and devices are shown in block diagram form in order not to obscure the description of the invention with unnecessary detail.

Power Factor Correction Methods and Apparatus

Figure 1 is a block schematic diagram of a power factor correction circuit (PFC) 100 per an aspect of the present invention. Power factor (PF) is defined as the ratio of the real power flowing to the load to the apparent power, and is a number between zero and one. It may also be expressed as a percentage, i.e. a PF of .5 is 50%. Real power is the capacity of the circuit for performing work in a particular time. Apparent power is the product of the current and voltage of the circuit. A load with a PF substantially closer to zero draws more current than a load with a PF closer to one for the same amount of useful power transferred. It is generally understood that a PF closer to zero is considered to be a low PF and a PF closer to one is considered to be a high PF. It is highly desirable to optimize the PF and bring it close to one especially when and if the utility energy meter records only the apparent power consumed over time and not the active power. In general, utility companies prefer to have a good power factor in a grid network in order to optimize the infrastructure and maximize the active energy it can deliver to its customers. Bad power factor such as 0.9 and lower, will generate excessive apparent current loss in the lines and stress the grid due to higher currents.

In the example of Figure 1, the PFC 100 is configured to correct the power factor of power being delivered to a residence or a home, represented by a load 120. The PFC 100 is generally coupled to a 110VAC line 101A and a neutral line 101B. The PFC 100 is coupled between a standard power meter 101 and the load 120. Most homes have several electronic appliances that all represent a load that consumes power. Usually, each load has a reactive component. This reactive component is generally the result of inductive properties of the most common loads found in a household, such as the motor of a washing machine, dryer HVAC unit, or dishwasher, and the like. The combination of all these loads appears as a single load 120 to a utility power meter 101. However, as different appliances are activated and deactivated, the reactive and real components of the load 120 seen by the power meter 101 change dynamically. To that end, the dynamic PFC 100 is able to correct a PF of a load
120 dynamically. In some embodiments, a reactive power measuring module 105 is electrically coupled to a 110 VAC power line (also referred to as a phase line) 101A and a neutral line 101B by a first insulated set of conduits 102 and a second set of conduits 103. The example shown, the first set of conduits 102 are able to be wires coupled to the 110VAC power line 101A. The first set of contacts 102 measures a phase current component of the power being delivered to a load. A second set of contacts 103 is coupled across the 110VAC power line 101A and the neutral line 101B to measure the phase voltage. A step down transformer 103A maybe included to lower the amplitude of the voltage allowing for more simplicity in the PFC 100, as lower voltage electronics are more cost effective and allow for greater ease of design. The reactive power measuring module 105 is able to determine the reactive power of the load through conduits 102 and 103. Byway of example, the reactive power measuring module 105 is able to comprise a processor unit, such as the Analog Devices ADE 7878. The measuring module 105 is further able to communicate with an external processor 107.

In some embodiments, the controller 107 is able to selectively couple a number of reactive loads having differing values, for example capacitors 11OA-11OC in parallel with the load 120 in order to compensate for the reactive component of the load 120. A binary implementation is used to couple the loads 11OA-11OC with the load 120. In order to determine a value for the loads 11OA-11C, it is advantageous to first ascertain a minimum and maximum reactive power compensation range. In a binary implementation, it can be shown that the accuracy of the PFC 100 is able to be precise as half the value of the reactive power of the lowest value among the loads 11OA-11OC, where each load corresponds to a bit or quantization level. The lowest value among the loads 11OA-11OC is a lowest bit reactive load and smallest component of the desired quantization. The exemplary implementation of the PFC 100 shows a quantization level of 3. Stated differently, there are three bit reactive loads, the lowest being the LSB, or least significant bit reactive load and the highest being the MSB, or most significant bit reactive load. The accuracy of the PFC 100 may be represented as:

\[
\text{Err}_{\text{MAX}} = \frac{\text{LSB}}{2}
\]

where the LSB is chosen optimally by the equation:
\[
\text{LSB} = \frac{\text{VAR}_{\text{MAX}}}{(2^N - 0.5)}
\]

Where \(\text{VAR}_{\text{MAX}}\) is the maximum reactive value of the load 120 to be compensated and \(N\) is the level of quantization. It can be appreciated that the level of quantization is directly proportional to the accuracy of the compensation of the reactive portion of the load 120. A desired quantization level may be determined as a balancing of desired accuracy versus cost and complexity. Simulations of approximately 50 samples of minimum and maximum reactive power of the load 120 to be corrected are shown in Table 1:

<table>
<thead>
<tr>
<th>Table 1:</th>
<th>N=1</th>
<th>N=2</th>
<th>N=3</th>
<th>N=4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy vs. 1LSB</td>
<td>49.1%LSB</td>
<td>47.9%LSB</td>
<td>45.5%LSB</td>
<td>46.8%LSB</td>
</tr>
<tr>
<td>Inaccuracy vs. VAR_{\text{MAX}}</td>
<td>32.7%</td>
<td>13.7%</td>
<td>6.1%</td>
<td>3.0%</td>
</tr>
</tbody>
</table>

A corrective reactive power value \(Q_{\text{CORR}}\) is determined by the following algorithm:

\[
\text{IF} \ (\text{round}(Q/\text{LSB})) > (2^N - 1) \\
\text{Then} \ Q_{\text{CORR}} = \text{LSB} \times (2^N - 1)
\]

Else \(Q_{\text{CORR}} = \text{LSB} \times \text{Round}(Q/\text{LSB})\), all values in VAR where \(Q\) is the reactive value of the load 120 to be compensated. As mentioned above, the reactive value of the load 120 is changing dynamically as household appliances are being activated and deactivated and their individual reactive loads are being coupled into the load 120. To that end, it is advantageous for the reactive power measuring module 105 to be configured to measure a reactive power for the load 120 and communicate the reactive power to the controller 107. Alternatively, the controller 107 may be directly coupled to the load 120 in order to determine the reactive power instantaneously. If \(Q\) is zero or positive, the reactive portion of the load 120 is inductive. Less commonly, a negative \(Q\) indicates that the reactive portion of the load 120 is capacitive. Table 2 shows an example of the impact of quantization on the PFC 100 accuracy.

Table 2
By way of example, the active power consumed is assumed to be between 10 and 3000 watts and the reactive power of the load 120 is assumed to be between 8 and 2000 VAR in a single phase, 2 wire network configuration. In this example, the PF is fixed at .67 for illustrative purposes. As can be seen from Table 2, an implementation of two or three bits (i.e. N = 2 or N=3) generally optimizes a power factor to be substantially close to one while minimizing cost and complexity. For an instance in a 110V system such as in the US, and where N=3, and for the example set forth in Table 2, the reactances of the two reactive bits Q_{LSB} and Q_{MSB} and the middle bit Q are calculated as:

\[ Z_{Q_{LSB}} = U^7/Q_{LSB} = 110V7266.7VAR = 45.37 \text{ Ohm (Purely Capacitive)} \]
\[ Z_{Q} = U7Q = 110V7533 .3VAR = 22.68 \text{ Ohm (Purely Capacitive)} \]
\[ Z_{Q_{MSB}} = U7Q = 110V71 066.7VAR = 11.34 \text{ Ohm (Purely Capacitive)} \]

Referring back to Figure 1, Capacitors 110A-1 IOC, where 110A is the LSB bit reactive load and 110C is the MSB bit reactive load, the capacitor values are calculated as:

\[ C_{LSB} = 1/(2\pi F Z_{Q_{LSB}}) = 1/(2\pi * 60Hz * 45.37 \text{ Ohm}) = 58 \text{ uF} \]
\[ C = 1/(2\pi F Z_{Q}) = 1/(2\pi * 60Hz * 22.68 \text{ Ohm}) = 117 \text{ uF} \]
\[ C_{\text{MSB}} = \frac{1}{2 \pi Z Q_{\text{MSB}}} = \frac{1}{(2 \pi \times 60 \text{Hz} \times 11.34 \text{ Ohm})} = 234 \mu \text{F} \]

As a result, the LSB bit reactive load 110A is 58 \mu \text{F}, the bit reactive load 110B is 117 \mu \text{F}, and the MSB bit reactive load 110C is 234 \mu \text{F} in this example. Each bit reactive load 110A-110C is coupled to the load 120 in parallel via switches 109A-109C. Each switch is enabled by a switch driver 108A-108C. Each switch driver in turn is controlled by the controller 107. As mentioned above, the controller 107 either is able to measure the reactive power of the load 120 to be compensated or has that information communicated to it by the reactive power measuring module 105. The controller is able to be coupled to a memory 106. Alternatively, the memory 106 may be integral to the controller 107. The memory 106 is able to store the values of the maximum reactive power of load 120 to be compensated and the bit reactive values of the loads 110A-110C. Additionally, the memory 206 is able to store power factor correction records in order to give a user, such as a homeowner, useful data on the power consumption characteristics of the residence. Therefore, the controller 107 is able to selectively activate the switch drivers 108A-108C to enable or disable switches 109A-109C thereby selectively coupling the bit reactive loads 110A-110C to the load 120 in parallel, thereby dynamically compensating for the reactive power of the load 120.

In some embodiments, the controller 107 is coupled to a communications module 114. The communications module 114 is able to communicate with other PFC units 100. Also, the communications module 114 is able to communicate with a user apparatus such as a laptop or a cell phone in order to notify a user, such as the homeowner, of the status of the PFC 100 and the amount of correction that the PFC 100 is doing. The communications module 114 is able to communicate wirelessly through a wireless module 114A. The wireless module comprises an antenna 114B to make use of a local WiFi network such as IEEE 802.11. In some embodiments, the wireless module 114A is able to communicate with a cellular telephone network via standard technologies such as CDMA or GSM. A user, such as the owner of a residence, is able to track their home's dynamic power consumption in order to make informed decisions regarding energy use. Alternatively, the communications module 114 is able to communicate via wired networks through a port 115 able to connect via LAN, Serial, Parallel, IEEE 1394 Firewire, or any other known or application specific wired
communications standard. The PFC 100 further comprises a DC power supply 104 coupled
to the 110VAC power line 101A and the neutral line 101B via a step down transformer 104A.
The DC power supply is able to convert power from the power line 101A to a desired DC
voltage to provide power to the electronics such as the reactive power measuring module 105,
controller 106, and the rest of the modules within the PFC 100.

In some embodiments, the switches 109A-109C are able to be one or more transistors.
A transistor may include any combination of bipolar transistors, MOS transistors, IGBT
transistors, FET transistors, BJT transistors, JFET transistors, IGFET transistors, MOSFET
transistors, and any other type or subset of transistor. With respect to bipolar and IGBT
transistors, some considerations in the selection of bipolar or IGBT transistor are the weak
zero collector - emitter voltage of the transistor in ON state and driving requirements.
Furthermore, transistors are generally unidirectional, meaning that current generally flows
from a drain to a source or from a collector to an emitter. To that end, it may be
advantageous to arrange two transistors, one for each direction of current flow, each having
its own bit reactive load to be coupled to the 120. Another implementation consideration
when using transistors as switches 109A-109C is that transistors generally require an
additional protection diode against reverse voltage. For example, if the transistor is rated for
more than 110 or 220VAC, the maximum emitter to base voltage is approximately 5-10V.
As a result, it may be advantageous to implement a protection diode in series with the emitter
to protect the transistor during the reverse half sine wave voltage. Due to energy lost as heat
dissipation, transistors may require one or more heat sinks. The power dissipated by the
transistor in a conducting state for half the sine wave may be approximated as

\[ \text{Power} = \frac{U_{CE} \cdot I_{CE}}{2} = U_{CE} \cdot \frac{(U_{AC} - U_{CE})}{(2 \cdot Z)} \]

Assuming \( U_{CESAT} = 2 \) Volts at 10A, such as the ON Semiconductor 2N3773, \( U_{AC} = 110 \) Volts
for a common US residential power line, \( Z = 10.59 \) ohm, the power dissipated as heat per
transistor can be approximated as

\[ \text{Power} = 2V \cdot \frac{(110VAC - 2V)}{(2 \cdot 10.59)} = 10.2W \text{ per transistor} \]
A 2 bit reactive power correction system would require 4 transistors, 4 capacitors and 4 power diodes. The total power dissipated as heating the switches 109A-109C may be approximated as:

\[
\text{Power} = 2 \times 10.2\text{W (bit 2)} + 2 \times 5.1\text{W (bit 2 = LSB)} = 30.6\text{W}
\]

As a result, it may be advantageous to couple the switches 109A-109C to a heat sink, adding cost and complexity to the PFC 100.

MOS and MOSFET transistors are generally lower power dissipation devices. However, MOS and MOSFET devices are unidirectional as well and need protection against excess reverse $V_{GS}$ voltages. The power dissipated by a MOS or MOSFET switch in a conducting state for half the sine wave voltage maybe approximated as:

\[
\text{Power} = R_{DS,0N} \times I_{DS} / 2 = (R_{DS,0N} / 2) \times (U_{AC} / Z)^2
\]

Assuming $R_{DS,0N} = 0.13$ Ohm at 10A, such as a ST Microelectronics STF20N20, $U_{AC} = 110$ Volts for a common US residential power line, and $Z = 10.59$ ohm, the power dissipated as heat in the switch maybe approximated as:

\[
\text{Power} = 0.13\text{ohm/2} \times (110\text{VAC} / 10.59\text{ohm})^2 = 7.01\text{W}
\]

A 2 bit reactive power correction system would require 4 transistors, 4 capacitors and 4 power diodes. The total dissipated power in the switches can be approximated as:

\[
\text{Power} = 2 \times 7.0\text{W (bit 2)} + 2 \times 3.5\text{W (bit 2 = LSB)} = 2\text{LOW}
\]

Although the use of MOS or MOSFET devices in the switches 109A-109C reduce the power dissipated as heat by approximately one third, a heat sink may still be needed to dissipate the waste heat. Although MOS or MOSFET devices having a very low $R_{DS,0N}$ are commercially...
available, they generally carry a higher cost.

Figure 2 shows a PFC 200 per an embodiment of the present invention. Similar to the PFC 100 of Figure 1, the PFC 200 is configured to correct the power factor of power being delivered to a residence or a home, represented by a load 220. The PFC 200 is generally coupled to a 110VAC line 201A and a neutral line 201B. The PFC 200 is coupled between a standard power meter 201 and the load 220. In some embodiments, a reactive power measuring module 205 is electrically coupled to a 110 VAC power line 201A and a neutral line 201B by a first insulated set of contacts 202 and a second set of contacts 203. The example shown, the first set of contacts 202 are able to be wires coupled to the 110VAC power line 201A. The first set of contacts 202 measures a phase current component of the power being delivered to a load. A second set of contacts 203 is coupled across the 110VAC power line 201A and the neutral line 201B to measure the phase voltage. A step down transformer 103A maybe included to lower the amplitude of the voltage allowing for more simplicity in the PFC 200, as lower voltage electronics are more cost effective and allow for greater ease of design. By way of example, the reactive power measuring module 105 is able to comprise a processor unit, such as the Analog Devices ADE 7753. In some embodiments, the module 205 is able to communicate sags or over voltage conditions to a micro controller 207.

A controller 207 is coupled to the reactive power measuring module 205. The controller 207 is coupled to a plurality of TRIAC drivers 208A and 208B. The triac drivers 208A and 208B in turn are configured to selectively activate and deactivate a plurality of TRIACs 209A and 209B. In the example shown, 10mA is utilized to drive the TRIACs. However, other driving signals may be utilized to drive the TRIACs depending on its specifications. A TRIAC, or Triode for Alternating Current, is an electronic component approximately equivalent to two silicon-controlled rectifiers coupled in an inverse parallel configuration with their gates electrically coupled together. This results in an electronic switch that is able to conduct current bidirectionally and thus doesn't have any polarity. It can be activated by either a positive or a negative voltage being applied to a gate electrode. Once activated, the device continues to conduct until the current through it drops below a certain threshold value known as the holding current. As a result, the TRIAC is a very convenient
switch for AC circuits, allowing the control of very large power flows with milliampere-scale control currents. TRIACs are generally understood to belong to a greater category of components known as thyristors. Thyristors include but are not limited to: silicon controlled rectifiers (SCR), gate turn off thyristors (GTO), static induction thyristors (SIT), MOS controlled thyristor (MCT), distributed Buffer - gate turn-off thyristor (DB-GTO), integrated gate commutated thyristor (IGCT), MOS composite static induction thyristor (CSMT), reverse conducting thyristor (RCT), Asymmetrical SCR (ASCR), Light Activated SCR (LASCR), Light triggered thyristor (LTT), Breakover Diode (BOD), modified anode gate turn-off thyristor (MA-GTO), distributed buffer gate turn-off thyristor (DB-GTO), Base Resistance Controlled Thyristor (BRT), field controlled thyristor (FCTh), and light activated semiconducting switch (LASS). A person of ordinary skill having the benefit of this disclosure will be able to recognize that the embodiment of the PFC 200 of Figure 2 may be readily modified to use any known or application specific thyristor to realize particular design or application requirements to implement the PFC 200.

The controller 207 is able to implement an algorithm as described in Figure 1 above to enable or disable the TRIACs 209A and 209B through the TRIAC drivers 208A and 208B. Advantageously, TRIACs enjoy a lower logic threshold to enable them. As a result, smaller and more cost effective components are able to be used as drivers 208A and 208B. When enabled, the TRIACs 209A and 209B couple bit reactive loads 210A and 210B in parallel with the load 220 in order to compensate for poor power factors. Optionally, filters 212 and 213 may be implemented to reduce switching noise or hum introduced by the TRIACs.

In some embodiments, the controller 207 is coupled to a communications module 214. The communications module 214 is able to communicate with either PFC units 200. Also, the communications module 214 is able to communicate with a user apparatus such as a laptop or a cell phone in order to notify a user, such as the homeowner, of the status of the PFC 200 and the amount of correction that the PFC 200 is doing. The communications module 214 is able to communicate wirelessly through a wireless module 214A having an antenna 214B to make use of a local WiFi network such as IEEE 802.11. Also, the wireless module 214A is able to communicate with a cellular network, such as CDMA or GSM so that a user may use a cellular phone in order to track and make educated decisions regarding the
energy consumption of their home. Alternatively, the communications module 214 is able to communicate via wired networks through a port 215 able to connect via LAN, Serial, Parallel, IEEE 1394 Firewire, or any other known wired communications standard. A memory module 206 is coupled to the controller 207. The memory module 206 is able to store information such as the maximum expected reactive component that maybe expected from the load 120, the corrective action history of the PFC 200, or any other useful data collected by or used by the PFC 200. The PFC 200 further comprises a DC power supply 204 coupled to the 110VAC power line 201A and the neutral line 201B via a step down transformer 204A. The DC power supply is able to convert power from the power line 201A to a desired DC voltage to provide power to the electronics such as the reactive power measuring module 205, controller 207, and the rest of the modules within the PFC 200.

A person of ordinary skill having the benefit of this disclosure will be able to appreciate that the PFC 100 and PFC 200 in Figures 1 and 2 respectively show a 2 wire, 2 phase system. The implementation of the PFC 100 or PFC 200 for three phase 3-wire or 4-wire network configuration follows the implementation of Figures 1 and 2 except that the bit reactive loads 11OA-11OC and 210A-210B, switches 109A-109C, TRIACs 209A and 209B, filters 112, 113, 212, 213 and associated driver circuits are tripled and connected from phase 1 to 2, phase 2 to 3, and phase 3 to 1. If the neutral is available, a star connection may be implemented; i.e. connection from phase 1 to neutral, phase 2 to neutral, and phase 3 to neutral. The PFC 100 and PFC 200 will be able to compensate independently for any reactive loads up the total maximum correctible value. By way of example, a property with an air conditioning unit of 300-600VAR connected between the 3 phases, a washing machine of 100-400VAR connected between phase 2 and neutral and a dryer of 100-250VAR connected between phase 3 and neutral will all be fully corrected up to the maximum correctable reactive value.

Distortion Correction Methods and Apparatus

A power factor that is less than perfect is the most common weakness to be corrected in an electrical network. Another and more common weakness and source of problem is distortion in a power line due to non linear loads and the growing proliferation of electronics
devices with affordable but less than perfect power adapters. Generally, when no special
effort is provided in the design the power adapter, the AC power signal is generally first fully
rectified on both sine periods and then roughly filtered by a big capacitor, followed by
isolated DC-DC power supply electronics, such as integrated circuits. This affordable and
non-energy star solution generates current harmonics that are fed back onto the network. The
result is a current waveform is that close to a truncated parabolic shape rather than a sine
wave. Distortion is able to comprise harmonic distortion resulting from the various
characteristics of the loads that absorb and reflect power, noise, or any other form of
distortion.

Figure 3A shows a time versus amplitude graph 300 of a power factor corrected
power signal having distortion. The first axis 320 represents time in milliseconds and the
second axis 310 is a generic amplitude scale to show the amplitudes of both the current and
the voltage. The voltage U(t) 330 appears as a perfect 60Hz sine wave. However, the current
i_{TOT}(t) is heavily distorted to the point where it no longer resembles a corresponding sine
wave. Figure 3B shows a similar graph 400 having a time axis 420 and an amplitude axis
410. A voltage waveform 430 closely tracks a perfect sine wave. However, the current
waveform 440 is heavily distorted. In a residence, heavy use of ubiquitous and low quality
power adaptors along with standard resistive loads may cause a current waveform 440 to
display such distortion: some resemblance to a sine wave but still greatly distorted. Figure
3C shows a similar graph 500 having a time axis 520 and an amplitude axis 510. Here, the
current waveform 530 is even more greatly distorted versus the voltage waveform 540 due to
the introduction of one or more heavy reactive loads such as air conditioning and dryer units.
Finally, figure 3D is a graph 600 of a common current waveform 630 versus a voltage
waveform 640. Not only are heavy reactive loads, resistive loads, and AC-DC power
adaptors causing significant distortion in the current 630, there is also a phase shift 670
between the current 630 and voltage 640. In this example, the distortion is shown as a peak
660 in the distorted current signal 630. In this example, the phase shift is approximately 30
degrees, corresponding to a PF of .67. In order to correct the distortion, it is advantageous
that the PF first be corrected. PF correction may be achieved by the methods or apparatus
discussed above in Figure 1 and Figure 2 or any other convenient method. A corrective signal
650 is derived by comparing the distorted current waveform 630 to the near perfect sine wave approximation voltage waveform (not shown). The corrective signal 650 comprises a factor of the distortion within the current waveform 630. The factor may be one, but the factor may be any necessary multiplicand to achieve a desired amplitude ratio of the current waveform. By way of example, the multiplicand may be a factor to convert a voltage to a current or a current to a voltage. When the corrective signal 650 is selectively coupled to the current signal 630, the result is a corrected current signal 640 having greatly reduced or eliminated distortion.

Figure 4 shows a schematic block diagram of a circuit 800 for suppressing or eliminating distortion as described in Figure 3D. The circuit 800 is coupled between a utility power meter 801 and a load 840. The load 840 maybe any load, but in this application and example it is a residential dwelling. The load 840 comprises all electrical devices within the dwelling that together appear as one load 840 to a utility power meter 801. The characteristics of the load 840 change dynamically as appliances are activated and deactivated within the residence thereby coupling and decoupling their individual loads to the load 840. A PFC 875 is able to correct a power factor in a power line 833 to substantially one. A processor 810 is able to detect a current by sensing the power line 833. In this exemplary embodiment, the processor 810 is an analog device. However, a person of ordinary skill having the benefit of this disclosure will recognize that digital processing may be substituted. The processor 810 is also able to detect a voltage by sensing both the power line 833 and a neutral line 834. The power line 833 is also referred to as a phase line. In this exemplary implementation, the processor 810 comprises two differential inputs. Each input is coupled to a multiplier G1 812 and G2 813. The multipliers 812 and 813 are able to scale the current or the voltage by any factor desired or required by a particular application or implementation of the circuit 800. G1 is configured to receive the current from the power line 833. In this embodiment, the multiplier G2 is able to convert the voltage sensed into a current signal. Both the voltage and the current are scaled by their respective RMS values. The multipliers 812 and 813 are able to be standard analog operational amplifiers or any other useful circuit. The outputs of the multipliers 812 and 813 are coupled to a substracter 814. In some embodiments, the substracter 814 is configured to compare the scaled outputs of G1 812 and
G2 813, thereby deriving a corrective signal, such as the signal 650 of Figure 3D. Advantageously, converting both inputs to a current allow for the use of a simple substracter 814. However, both inputs may be converted into a voltage signal as well. In some embodiments, it may be desirable to include a block loop gain and loop filter 821 to control the process and optimize system control such as dynamic behavior, stability, gain margin, phase margin, and the like. It should be noted that the substracter 814 is able to be configured to compare the total current to a reference signal by subtracting the total current having distortion from the reference signal, or subtract the reference signal from the total current having distortion. The configuration may be made to suit particular implementation or application requirements. As a result, the corrective signal maybe directly or inversely proportional to the distortion in the total current.

The corrective signal is combined with the current to form a corrected current signal having greatly reduced or eliminated distortion, such as the signal 640 in Figure 3D. In the embodiment shown in Figure 4, the output of the loop filter 821 is coupled to a negative rectifier 815 and a positive rectifier 822. The negative rectifier 815 is in turn coupled to a first controlled current source 831 and the negative rectifier is coupled to a second controlled current source 832. In certain applications, such as the example of Figure 4, the impedance of the network downstream from the power meter 801 may have a very small impedance compared to the load 840. As a result, when current is injected to correct a negative distortion, the current will be sourced towards the grid rather than the load 840. As a result, distortion will be amplified. To that end, the embodiment of Figure 4 sinks current from the power line 833 in response to a negative distortion and sources current in response to a positive distortion. Due to the imbalance of the impedances of the grid and the load 840, the selectively sourced and sunk current will correct the distortion. When a corrective signal is negative, meaning that the distortion component is subtractive to the total current, the positive rectifier 822 enables the second controlled current source 832. The second controlled current source 822 is coupled to a negative DC power supply 852. When the second controlled current source 832 is enabled, current is sunk from the power line 833. In an embodiment wherein the grid impedance is lower than the impedance of the load 840, current will be sunk from the grid rather than the load, causing an additive effect to the load 840. When a
corrective signal is positive, meaning the distortion is additive to the total current, the negative rectifier 815 enables the first controlled current source 831. The first controlled current source 831 is coupled to a positive DC power supply 851. When the first controlled current source 831 is enabled, current is sourced from the positive DC power supply 851 to the power line 833. Again, in applications where the grid impedance is lower than the load 840, current will be sourced into grid rather than the load, causing a subtractive effect on the load 840. In operation, a corrective signal such as the signal 650 in is combined with a current signal having distortion such as the waveform 630 of Figure 3C by selectively sinking or sourcing current according to the corrective signal into the power line. One of a positive portion of the corrective signal and a negative portion of the corrective signal is selectively coupled to one of the controlled current sources 831 and 832. This is able to be done dynamically as the distortion component of the power line 833 changes with changes in the load 840 since the processor 810 continually compares the voltage to the current and continually derives a corrective signal. Alternatively, the processor 810 is able to generate its own reference signal to compare the distorted current signal to. For example, power in the United States is delivered at 60Hz. Therefore, a 60 Hz function generator within the processor 810 would be able to generate a perfect sine wave to compare the distorted current signal to and thereby derive a corrective signal. Alternatively, phase locked loops may be implemented to lock on zero crossing times of the voltage in order to derive a near perfect reference signal. As mentioned above, the substracter 814 may be configured to form a corrective signal that is directly or inversely proportional to the distortion in the total current. If the substracter 814 is configured to form a corrective signal that is directly proportional to the distortion, then a positive portion of the distortion should cause current to be sunk from the power line 833 accordingly. Likewise, a negative portion of the distortion should cause current to be sourced into the power line accordingly. The inverse is also true. In embodiments wherein the corrective signal is inversely proportional to the distortion in the total current, a negative portion of the corrective signal should cause current to be sunk away from the power line 833. Likewise, a positive portion of the corrective signal should cause current to be sourced into the power line 833.

While the embodiment shown in Figure 4 utilizes components that are widely
available and cost effective, it can be appreciated that the controlled current sources 831 and 832 are not very energy efficient. Assuming the positive DC power supply 851 is 250V, the instantaneous voltage in the power line 833 is 150V, and that the corrective current signal is 10A, the power dissipated and lost to waste heat maybe hundreds of watts.

To that end, Figure 5 shows a distortion reduction circuit 900 having a modulator 920. Similar to the circuit 800 of Figure 4, The circuit 900 is coupled between a utility power meter 901 and a load 940. The load 940 may be any load, but in this application and example it is a residential dwelling. The load 940 comprises all electrical devices within the dwelling that together appear as one load 940 to a utility power meter 901. A PFC 975 is able to bring a power factor of the power line 933 to substantially one. The PFC 975 maybe according Figures 1 or 2 or any other convenient PFC. As mentioned above, the characteristics of the load 940 change dynamically. A processor 910 is able to detect a current by sensing a power line 933. In this exemplary embodiment, the processor 910 is an analog device. However, a person of ordinary skill having the benefit of this disclosure will recognize that there are many off the shelf digital processors capable of executing the functions described below. The processor 910 is also able to detect a voltage by sensing both the power line 833 and a neutral line 934. In this exemplary implementation, the processor 910 comprises two differential inputs. Each input is coupled to a multiplier G1 912 and G2 913. G2 913 is able to convert a voltage to a current signal in a similar fashion to G2 813 of Figure 4 and is shown in a simplified manner. The multipliers 912 and 913 are able to be standard analog operational amplifiers or any other useful circuit. The outputs of the multipliers 912 and 913 are coupled to a substracter 914. In some embodiments, the substracter 914 is configured to subtract the output of G1 912 from the output of G2 913, thereby deriving a corrective signal, such as the signal 650 of Figure 3D. In some embodiments, it may be desirable to multiply this corrective signal by a scaling factor. By way of example, a loop gain filter is included to control the process in a similar fashion as shown in Figure 4 and in some embodiments combines the corrective signal by an RMS value of the current 811.

The output of the loop filter is coupled to a modulator 920. In this exemplary embodiment, the modulator 920 is a pulse width modulator (PWM). However, any method or scheme of modulation may be implemented as specific implementation and design
restrictions require, including but not limited to PWM, delta-sigma modulation, pulse code modulation, pulse density modulation, pulse position modulation, or any other known or application specific modulation scheme. The modulator 920 comprises a positive trigger comparator 822 and a negative trigger comparator 823 that signal a high logic level when the corrective signal emitted from the multiplier 915 is positive and a low logic level when the corrective signal is negative. In some embodiments, the low logic level is able to be a negative value. A pulse generator 921 generates a triangle wave that is combined with the positive portion of the corrective signal emitted from the negative trigger comparator 922 and the negative portion of the corrective signal emitted from the positive trigger comparator 923 by combinational logic 925. As a result, what is formed is a PWM corrective signal divided between positive and negative portions. The combinational logic 925 is configured to selectively couple a positive portion of the PWM corrective signal with a first controlled switch 932. The first controlled switch 932 is coupled to a negative DC power supply 952. The combinational logic 925 is also configured to selectively couple a negative portion of the PWM corrective signal with a second controlled switch 931. The second controlled switch is coupled to a positive DC power supply 952.

In operation, the switches 931 and 932 are selectively controlled by the PWM corrective signal depending on whether the PWM corrective signal is positive or negative. In some embodiments, a positive PWM corrective signal means that the distortion to be corrected in the power line 933 is negative, and vice versa. To correct a negative distortion in the power line 933, the second controlled switch 831 is enabled according to a negative portion of the PWM corrective signal. The second controlled switch, when enabled, couples sources from the positive DC power source 951 with the power line 933 according to the PWM corrective signal.

In the embodiment of Figure 5, an embodiment is shown wherein the impedance of the utility power meter 901 (and the grid that is downstream) has a lower impedance than the load 940. As a result, if a positive distortion is attempted to be corrected by a negative PWM corrective signal, the current sunk from the power line 933 will be sunk from the grid rather than the load 940. As a result, the distortion will be amplified. To that end, a positive PWM corrective signal is used to correct a positive distortion and a negative PWM corrective signal
is used to correct a negative distortion in applications where the impedance of the load 940 is greater than the impedance of the grid downstream from the power meter 901.

In some embodiments, it may be advantageous to filter the modulating signal. To that end, a filter 933 is included. Similarly, to correct a positive distortion in the power line 933, the first controlled switch 832 is enabled according to a negative portion of the PWM corrective signal. The first controlled switch, when enabled, sinks current to the negative DC power source 952 from the power line 933 according to the PWM corrective signal. As a result, distortion is substantially decreased from the current in the power line 933. Also, a second filter 934 may be advantageous to filter PWM noise from the power line 933. Each of the positive DC power source 951 and negative DC power source 952 comprise current limiting and sensing module 935 and 936 for communication any over current or under current conditions to the processor 910.

Figure 6 shows another embodiment of a distortion correction circuit 1000. Again, the circuit 1000 is coupled to a power line 1032 and a neutral 1034 in a two wire, one phase power system between a utility power meter 1001 and a load 1040. The load 1040 comprises all appliances and other electronic devices within a residence that appear as one load 1040 having reactive properties. In this embodiment, the current is measured by a processor unit 1200. A PFC 1275 is able to correct a power factor in the power line 1032 as described above. The processor unit 1200 comprises a current and voltage measurement module 1202. The module 1202 is also configured to do RMS and distortion computation. The module 1202 is able to be a digital processing module. In some embodiments, the module 1202 comprises one or more analog to digital converters for converting data, such as amplitude, phase, and distortion into digital bitstreams upon which mathematical operations may be done digitally. The processor 1200 is also able to have a memory module 1201. The memory module 1201 is able to store information relating to the dynamic harmonic correction, such as during what times of day correction is most active. The memory 1201 may be removed and inserted into a device such as a computer so that a user may make informed decisions regarding energy use. Alternatively, the processor 1200 comprises a communications module (not shown). The communications module may be connected to the internet through wires, such as by LAN cable, or wirelessly via a convenient standard such as IEEE 802.11 or
BlueTooth. Furthermore, the communications module may communicate through cellular standards such as GSM or CDMA. A protection module 1203 integral to the processor 1200 is able to power down the circuit 1000 in any defined fault condition, such as over voltage, over current, and over temperature. Such fault conditions are able to be stored in the memory 1201.

The processor 1200 is able to compute the total current having distortion within the power line 1032 and generate a reference signal. A digital to analog converter is able to convert digital bitstreams representing a total current and a reference signal into analog waveforms. Similar to the embodiments of Figures 4 and 5, the total current signal may be subtracted from the reference signal by a substracter. Alternatively, the processor 1200 is able to digitally subtract the total current from the reference signal, thereby forming a digital corrective signal. The processor 1200 is also able to modulate the digital corrective signal by any convenient known or application specific means of modulation. The modulated corrective signal may then be selectively coupled with a first transistor 1031 or a second transistor 1030 depending on whether current must be sunk or sourced into the line 1032 to correct distortion in the total current. The first and second transistors 1031 and 1030 operate as switches, that when enabled by the modulated corrective signal, source or sink current to or from the line 1032 from a positive DC source 1051 or a negative DC source 1052. In some embodiments, it maybe advantageous to include a first filter 1033 and a second filter 1034 to filter PWM noise from the first transistor 1031 and the second transistor 1030 respectively.

Figure 7 shows a further detailed embodiment of the invention of Figures 4, 5 and 6. The power factor and distortion correction module 1300 is coupled between a utility power meter 1302 and an equivalent property load 1340. The load 1340 is a representation of a dynamic load that changes as appliances within the residence as activated and deactivated. The positive DC power source 1351 comprises an optional low pass filter 1303 for filtering any noise and harmonics that may be present across the phase line 1333 and neutral 1334. AC power from the grid 1301 is rectified by a bridge rectifier 1304 and passed through a reservoir capacitor 1305. A PFC module 1306 is provided for correcting a less than ideal power factor. The PFC module 1306 is able to utilize any of the methods or apparatus described in Figured 1 and 2 and accompanying description. A first switching circuit 1331
comprises a first transistor 1308A coupled to the processing unit 1310. The processing unit 1310 drives the transistor 1308A by utilizing a modulated signal. The transistor 1308A couples current from the positive DC power source 1351 to the phase line 1333 in response to a corrective signal as described in the previous embodiments in Figures 5 and 6. An optional low pass filter 1309A is provided for filtering a modulating signal. A current limitation and sensor 1310A is able to communicate overcurrent conditions to the processor 1310. The sensor 1310A is represented by a resistor, but may be any useful sensing module for sensing an overcurrent condition. The positive DC power source is further coupled to a negative PFC module 1352 through an inverting power supply capacitor 1307. The inverting reservoir capacitor 1307 provides negative DC power proportional to the power supplied by the DC power source 1351. The negative PFC module 1352 is able to correct a power factor on the phase line 1333 according to the methods and apparatus described in Figures 1 and 2. The negative PFC module 1352 is coupled to a second switching circuit 1332. The second switching circuit 1332 comprises a second switching transistor 1308B also for receiving a modulated corrective signal from the processing unit 1310 as described in the embodiment of Figures 5 and 6. The processing unit 1310 comprises scaling multipliers G1 and G2. In this embodiment, G2 is coupled to a voltage to current converter. A substracter is able to compare one voltage signal to another to derive a corrective signal, as described in previous embodiments. A modulator is coupled to the output of the substracter for modulating the corrective signal. In this embodiment, PWM is shown. However, any known or application specific modulation scheme may be utilized. In some embodiments, a loop filter is coupled between the substracter and modulator for controlling the process and optimize system control such as dynamic behavior, stability, gain margin, phase margin, and the like. Furthermore, external processing may contribute to current measurement, voltage measurement, RMS and distortion computations and include memory such as RAM or ROM.

Figure 8 shows another embodiment wherein the source and sink current paths include an inductance 1360 and 1361 each to smooth and filter out the modulation that may generate spikes of voltages and currents. The first and second switching transistors 1308A and 1308B may charge the inductors 1360 and 1361 respectively in a quasi linear ramp up and when either the transistors 1308A and 1308B are disabled, and let the current charge
decrease to zero in a quasi linear fashion. A free wheel diode 1363 is needed to avoid for the current to shut off rapidly to avoid destructive high voltage spikes due to the inductance. A second freewheel diode 1364 is coupled in parallel to the second inductor 1362. The current waveform formed is similar to seesaw shape and allows for simpler filters 1309A and 1309B. In some embodiments, the inductors 1361 and 1362 are integrated into the filters 1309A and 1309B. Advantageously, losses in the paths sinking and sourcing current are diminished. In some embodiments, capacitors may be included in parallel to recycle any lost energy by the free wheel diodes 1363 and 1364. In the embodiment of Figure 8, the inductors 1361 and 1362 are coupled between the switching transistors 1308A and 1308B and the low pass filters 1309A and 1309B respectively.

In some applications, it maybe advantageous to couple the inductors 1361 and 1362 between the PFC modules 1351 and 1352 and the transistors 1308A and 1308B so that the inductance are not directly coupled with the load 1340, and the impedance measured from the grid 1301 is improved. Figure 9 shows such an implementation. Figure 9 shows a first current charging inductor 1363A coupled between the positive PFC module 1351 and the first transistor 1308A. Also, there is provided a second charging inductor 1363B coupled between a negative PFC module 1362 and the second transistor 1308B. Advantageously, when measured with from the grid equivalent impedance 1302, the first and second charging inductors 1363A and 1363B do not form additive inductance or reactance to the equivalent property load 1340, thereby easing any power factor correction requirements. Similarly to Figure 8, the first and second charging inductors 1363A and 1363B each have coupled in parallel thereto a freewheel diode 1364A and 1364B. As discussed above, a flywheel diode is a diode that protects a transistor, switch, relay contact etc. when switching DC powered inductive loads (relays, motors etc) is called a flywheel (or flyback) diode. A flywheel diode is often desirable because there are instances when the current through an inductive load is suddenly broken. In such instances, a back electro motive force (EMF) will build up as the magnetic field breaks down, and if there is no path for the current, a high voltage builds up. The high voltage can damage a transistor or cause arcing across the transistor. The flywheel diode is connected in reverse across the inductive load, and provides a path for the current so the magnetic field and current can safely decline.
Figure 10 shows yet another alternate embodiment of a circuit for distortion correction in a power line. It is desirable, and in some places required, to galvanically isolate electronics from a power supply line. Galvanic isolation is the principle of isolating functional sections of electrical systems preventing the direct conduction of electric current from one section to another. Energy and/or information can still be exchanged between the sections by other means, e.g. capacitance, induction, electromagnetic waves, optical, acoustic, or mechanical means. Galvanic isolation is used in situations where two or more electric circuits or two section of one system must communicate or transfer energy, but their grounds may be at different potentials, or one section is more susceptible to current spikes than another section, or any host of protection reasons. It is an effective method of breaking ground loops by preventing unwanted current from traveling between two units sharing a ground conductor. Galvanic isolation is also used for safety considerations, preventing accidental current from reaching the ground (the building floor) through a person's body.

Figure 10 shows a harmonic distortion correction system 1300 wherein the electronics are galvanically isolated on the output side from the equivalent property load 1340. In Figure 10, the output of the first switching transistor 1308A and second transistor 1308B are coupled to the first winding 1371 of a transformer 1370. Preferably, the transformer 1370 is a high frequency, high power transformer. The secondary 1372 of the transformer 1370 is coupled to the equivalent property load 1340 in parallel. Optionally, a low pass filter 1375 can be disposed between the secondary 1372 and the equivalent property load 1340 for filtering out any artifacts remaining from switching. When the circuit 1300 is correcting a negative harmonic, meaning that current is being sourced into the equivalent property load 1340, current is sourced from the center tap 1374 (coupled to ground) according to the switching signal provided by the processing unit 1310 to the transistor 1308A. Accordingly, the voltage generated across the primary 1371 is reflected to the secondary 1372 and a corresponding current is sourced into the equivalent property load 1340. Similarly, when a positive harmonic is to be corrected, meaning current is to be sunk from the equivalent property load 1340, a switching signal is provided the transistor 1308B from the processing unit 1310. A negative voltage is formed across the primary 1371 which reflects to the secondary 1372. Advantageously, none of the electronics such as the processing unit 1310, the current and
voltage measurement module and processor and memory 1305, PFC modules 1351 and 1352, are directly coupled with the equivalent property load 1340. Optionally, a full galvanic isolation for the system 1300 can be achieved by inserting an isolation transformer between the optional low pass filter 1303 and the rectifier 1304, and adding a transformer for the phase voltage measurement feeding the computation unit 1311. However, as can be appreciated, in sourced or sunk current will follow the path of least resistance. As a result, current sourced to the equivalent property load 1340 or sunk from the equivalent property load to correct a negative or positive harmonic respectively will not necessarily be applied to the equivalent property load. The nodes 1380A and 1380B form current dividers between the equivalent property load and the grid equivalent impedance 1302. Generally, the grid equivalent impedance can be quite low, on the order of the equivalent property load 1340 or even lower. It follows naturally that current sourced to the equivalent property load 1340 will instead be sourced to the grid equivalent impedance 1302, and back to the power grid in general. Similarly, current that was intended to be sunk from the equivalent property load 1340 will instead be drawn from the grid equivalent impedance 1302. What will result is incomplete correction of harmonic distortion in the power line.

To that end, Figure 11 shows a total harmonic distortion correction system 1500 wherein the current is selectively sunk or sourced to the equivalent property load 1540 in a series configuration, thereby eliminating the current divider that was formed at nodes 1380A and 1380B of Figure 10. As in Figure 10, the outputs of the transistors 1508A and 1508B are coupled to the primary of a transformer 1570 having a center tap 1574 to ground. However, in the configuration of Figure 11, the secondary 1573 is coupled in series with the equivalent property load 1540. Optional low pass filters 1572 and 1575 are coupled between the secondary 1573 and the grid equivalent resistance 1502, and the secondary and the equivalent property load 1540 respectively for filtering out any artifacts of switching or any other high frequency artifacts from the grid 1501. In this exemplary implementation, to correct a positive harmonic, the processing unit sends PWM signal to the transistor 1508B coupled to the negative PFC module 1535. When a corresponding voltage signal is formed across the primary 1571, it is reflected to the secondary 1573. Since the secondary 1573 is in series with the equivalent property load 1540, there is nowhere for the current to be sunk from than the
equivalent property load 1540 because there is no current divider to offer a path of less resistance. Similarly, when a negative harmonic is to be corrected, meaning current is to be sourced into the equivalent property load 1540, current has only one direction in which to flow. What results is a more complete harmonic correction.

In some applications, the EMI resulting from the switching outputs (such as the transistors 1508A and 1508B) is undesirable or not acceptable. To that end, the positive and negative power supplies that provide sinking and sourcing current can be modulated or otherwise more carefully manipulated to obviate a need for modulation. To that end, Class G and Class H power supplies can be incorporated into the systems described in Figures 6-11. Class G power supplies use "rail switching" to decrease power consumption and increase efficiency. There are a plurality of power rails available, and a different rail is used depending upon the instantaneous power consumption requirement. As a result, there is less area between the signal to be drive and the power rail. Thus, the amplifier increases efficiency by reducing the wasted power at the output transistors. Class G power supplies are more efficient than class AB but less efficient when compared to a switching solution, without the negative EMI effects of switching. Figure 12A shows an output graph 1200 with a voltage axis 1201 and a time axis 1202, representing a modulated signal 1203 and multiple voltage rails 1204A-1204F. From a time t=0 to t=1, the amplitude of the modulated signal 1203 is less than VI. As a result, a Class G power supply synchs to voltage rail VI 1204C. When the switching transistor is being turned on thus causing the rising slope seen starting near t=1, the driver (for example, current sources 831 and 832 of Figure 4) dissipates power as heat and thereby loses efficiency. Since the rail VI 1204C is of a low magnitude compared with the amplitude of the modulated signal 1203 at the time t=1, the overall inefficiency is greatly reduced. As the amplitude of the modulated signal 1203 increases between time t=1 and t=2, a greater magnitude voltage rail is required to drive the modulated signal. To that end, the rail V2 1204B is switched to. Similarly, V3 1204A is used after time t=3 since the amplitude of the modulated signal 1203 has increased again. Similarly, in a negative cycle, negative rails 1204D-1204F are switched to in sequence as the negative amplitude of the modulated signal 1203 increases from time t=4 to t=6.

Figure 12B shows the output 1250 of a Class H power supply. Class H amplifiers
modulate the power supply rail like in the case of a Class G power supply, but go one step further by continuously modulating a supply rail to form an infinitely variable supply rail. This is done by modulating the supply rails so that the rails are only relatively slightly larger in absolute magnitude than the output signal at any given time. As a result, the output stage operates at its maximum efficiency all the time. The graph 1250 has a voltage axis 1251 and a time axis 1252. For simplicity, the same modulated signal 1253 as shown in Figure 12A is used. In a Class H amplifier, the power supply rail voltage 1254 closely traces the modulated signal 1253. Therefore, the delta between the modulated signal 1253 and the rail voltage 1254 is continuously minimized. As a result, the driving devices (for example, current sources 831 and 832 of Figure 4) are efficiently driven.

Figure 12C shows an implementation of a Class H power supply in a harmonic distortion reduction system 1600. The Class H power supply comprises a rectifier 1610 that provides DC voltage to a positive switching power supply 1620 and a negative switching power supply 1630. The rectifier 1610 is electrically coupled to the phase 1603 and neutral 1604 lines and receives an AC power source therefrom. An optional low pass filter 1611 can filter out any unwanted noise or artifacts in the AC power. A rectifier 1612 rectifies the filtered AC power into DC power. Any known, convenient or application specific rectification circuit will suffice such as a bridge rectifier. In some embodiments, a PFC module 1615 is provided to bring the power factor of the power provided to substantially one. By way of example, a power factor correction circuit as described in Figures 1 and 2 and corresponding text can be used. The positive switching supply 1610 comprises a switching transistor 1611. The switching transistor 1611 receives a control signal from a processing unit 1650 that operates as described in Figures 6-11 to form a corrective signal by subtracting a sample of the phase line 1603 from a reference signal. According to the control signal, the switching transistor 1611 forms a PWM signal which passes through an LC-Flywheel network 1622 which takes a positive average of the PWM signal. Any artifacts or noise are filtered by an optional low pass filter 1623. An overcurrent sensor 1624 is provided for controlling or limiting current surge situations. Similarly, the negative switching supply 1630 comprises a switching transistor 1631. Again, the switching transistor 1631 receives a control signal from a processing unit 1650. In the case of the negative switching power
supply 1630 the processing unit 1650 only sends a control signal if there is a positive harmonic to be corrected, as explained in the several drawings and corresponding text above. According to the control signal, the switching transistor 1631 forms a PWM signal which passes through another LC-Flywheel network 1632 which takes a negative average of the PWM signal. Any artifacts or noise are filtered by an optional low pass filter 1633. An overcurrent sensor 1634 is provided for controlling or limiting current surge situations.

Figure 12D shows another embodiment of a harmonic distortion reduction system 1700 having a class H power supply. Similarly to the embodiment of Figure 16, the rectifier 1710 is electrically coupled to the phase 1703 and neutral 1704 lines and receives an AC power source therefrom. A low pass filter 1711 is provided to filter out any unwanted artifacts in the AC power. A bridge rectifier 1712 rectifies the filtered AC power into DC power. Although a bridge rectifier is mentioned, any known, convenient or application specific rectification circuit will suffice such as a bridge rectifier. In some embodiments, a PFC module 1715 is provided to bring the power factor of the power provided to substantially one. By way of example, a power factor correction circuit as described in Figures 1 and 2 and corresponding text can be used. The positive switching supply 1710 comprises a switching transistor 1721. The switching transistor 1721 receives a control signal from a processing unit 1750 that operates as described in Figures 6-11 to form a corrective signal by subtracting a sample of the phase line 1703 from a reference signal. According to the control signal, the switching transistor 1721 forms a PWM signal which passes through an LC-Flywheel network 1722 which takes a positive average of the PWM signal. Any artifacts or noise are filtered by an optional low pass filter 1723. An overcurrent sensor 1724 is provided for controlling or limiting current surge situations. The modulated positive power provided by the positive switching power supply 1710 feeds a second positive switching transistor 1725. The second positive switching transistor 1725 is also controlled by the processing unit 1750. Advantageously, the modulated power provided by the positive switching power supply 1710 closely tracks the PWM signal received by the second positive switching transistor 1725. As a result, very little headroom exists between the power supply and the power demand, as demonstrated in the output graph of Figure 12B. The negative switching transistor 1731 also receives a control signal from a processing unit 1750. The negative switching transistor 1731
is only activated by the processing unit 1750 when a positive harmonic is detected, meaning current must be sunk from the equivalent property load 1740. According to the control signal, the negative switching transistor 1731 forms a PWM signal which passes through an LC-Flywheel network 1732, thereby forming a negative average of the PWM signal. An optional low pass filter 1723 filters any artifacts or noise. An overcurrent sensor 1734 is provided for controlling or limiting current surge situations. The modulated positive power provided by the negative switching power supply 1730 feeds a second negative switching transistor 1735. The second negative switching transistor 1735 is also controlled by the processing unit 1750. Advantageously, the modulated power provided by the negative switching power supply 1720 closely tracks the PWM signal received by the second positive switching transistor 1725. As a result, very little headroom exists between the power supply and the power demand, as demonstrated in the output graph of Figure 12B.

Figure 13A shows another implementation of a harmonic distortion reduction system 1800 incorporating a solar power system (not shown) through a selector 1870. Before discussing the advantages and values of the system shown in Figure 13A, it is useful to understand a prior art solar power delivery system. Figure 13B shows a standard prior art solar power delivery system 1890. Solar panels 1891 are mounted such that they receive the greatest sunlight. The solar panels 1891 are electrically coupled to a regulator 1893 via diodes 1892 that protect the solar panels 1891 from reverse current. The regulator 1892 divides the available current from the solar panels 1891 while maintaining a 12VDC (or any other desired voltage) to batteries 1894 and an inverter 1895. The batteries 1894 act as a buffer to keep current flowing to the inverter 1895 if the solar panels 1891 were to quit generating current because of lack of sunlight. Because the solar panels 1891 generate only DC current, the inverter must also convert the DC current into AC current so the power is compatible with a residential equivalent load. The inverter is coupled to the Line (or Phase) and Neutral lines such as 1603 and 1604 of Figure 12C. The inverter 1895 is also protected by a fuse 1897 coupled between the inverter 1895 and regulator 1893. All of the regulator 1893, inverter 1895 and batteries 1894 are also coupled to ground through an earth spike 1896, which is generally a long metal rod which is inserted into the ground below the residence that the system 1890 is mounted on. However, DC-AC inverters are well known to
be inefficient. The most efficient designs reach approximately 85% efficiency, meaning that 15% of the energy generated by the solar panels 1891 is wasted to heat or mechanical vibration.

To that end, Figure 13A shows a harmonic distortion reduction system 1800 having the ability to inject solar power either into an equivalent property load 1850 or back into the power grid 1801 without the use of an inefficient and cumbersome inverter. The harmonic distortion reduction system 1800 comprises a DC power source 1810. The DC power source 1810 is coupled to the phase 1803 and neutral 1804 lines to receive AC power therefrom. An optional low pass filter 1811 filters out any harmonics or artifacts in the phase line 1803. Preferably, an isolation transformer 1812 is provided to galvanically isolate the phase and neutral lines 1803 and 1804 from the solar power system (described later). Then, a bridge rectifier 1813 converter rectifies the AC power to DC power. Although a bridge rectifier 1813 is shown, any rectification circuit or means can be used. Optionally, a PFC modules 1814 and 1815 can correct current distortion in the power supplies 1814 and 1815 and bring the current harmonic distortion to substantially zero. The DC power source 1810 is coupled to a switch 1870. The switch 1870 selectively couples either the DC power source 1810 or a solar power system (not shown) as an external DC power source. The switch 1870 is controlled by the measurement, processing and memory unit 1820. The unit 1820 can be programmed to automatically switch between the DC power source 1810 and the solar power system based upon the time of day and preprogrammed sunrise and sunset schedules. Alternatively, the unit 1820 can instruct a switch to either the DC power source 1810 or the solar power system depending upon the instantaneous current generation capability of the solar power system. If the solar power system is generating sufficient power to correct harmonic errors measured, then the solar power system can be switched into the system 1800. Any excess power provided by the solar power system can be used by the equivalent property load 1850. The switch 1870 is coupled to a positive switching circuit 1830 and a negative power supply 1815 which inverts the positive DC power supplied by the either the DC power source 1810 or the solar power system. A negative switching circuit 1840 modulates the negative DC power provided by the negative power supply 1815. The positive switching circuit 1830 and the negative switching circuit 1840 are controlled by the processing unit.
1825 as described in the several embodiments above; a positive PWM signal is generated to correct a negative harmonic error, and vice versa. Preferably, galvanic isolation is provided by a high frequency transformer 1880. The high frequency transformer isolates the equivalent property load 1850 and the grid 1801 from any potential spikes in current caused by the solar power system. In fact, such isolation can be required by regulation in solar power systems. An optional low pass filter 1881 is provided to filter out any artifacts or noise. Advantageously, the solar power system 1890 as shown in Figure 13B, leaving aside the inverter 1895, can be implemented with the harmonic distortion reduction system 1800 with extremely high efficiency. Furthermore, the secondary 1882 HF transformer 1880 is shown coupled in parallel with the equivalent property load 1850.

One advantage of the system described in Figure 13A is shown graphically in Figure 13C. Figure 13C shows a graph 1875 having a current axis I and atime axis t. A first output curve 1876 represents a current waveform that is heavily distorted. Through the means and methods described in the several drawings and corresponding text, it has been shown that the harmonic distortion 1872, represented by the single hatched area, can be corrected by selectively sinking and sourcing current to correct positive and negative harmonic errors respectively. What is formed is a corrected current waveform 1877. However, with the implementation of the system 1800 of Figure 13C, it becomes possible to inject additional energy from a solar power system. As a result, new current waveform 1878 is formed by the additional injected current 1873 represented by the double cross hatched area. As discussed above, PWM modulation is a highly efficient method of controlling the current sources, such as transistors 1308A and 1308B of Figure 8. In operation, DC current generated by the solar power system is converted into AC power used by an equivalent property load without losses due to an inverter found in prior art solar power systems.

Figure 13A is a preferred implementation for solar self generation and harmonic distortion correction for a 2-wire or 3-wire 1 phase power network configuration. In other embodiments, the solar self generation and harmonic correction distortion can be implemented for cases of 3-wire or 4-wire split phase power network configuration (phase, split phase, neutral and optionally earth). In such cases, the transformer 1890 is replaced by a transformer with same dual windings at the input and output. Input configuration is same as
The 2 output windings are connected at middle point to the neutral while each other access of the windings connected to the phase and resp. the split phase. Two optional low pass filters similar to 1891 can be used to filter out the PWM modulation on the wire attached to phase and to the one attached to split-phase.

To that end, a preferred configuration for solar self generation and harmonic correction distortion for a4-wire or 5-wire tri phase power network configuration (3 phases, neutral and optionally earth) is presented in various embodiments in Figures 13D-F. In these cases the transformer 1890 is replaced by a transformer with same dual windings at the primary but 3 windings at the secondary. Input configurations are similar to the configurations of Figure 13A. Configuration of the secondary windings can be delta or star configuration.

Figure 13D shows an implementation of a multi phase solar self generation and harmonic distortion correcting system 2000. The system 2000 forms a corrective signal similarly to the system 1800 of Figure 13A. The system 2000 of the multiphase configuration is able to inject self generated energy in a 3 or 4 wires split phase configuration. The load 1340 represents all the combined loads coupled between the phase 1333 line and neutral 1334 line. The load 1341 represents all combined loads coupled between then neutral 1334 line and the split phase line 1335. The load 1342 represents all loads coupled between the phases 1333 and split phase 1335 lines. The secondary 1892 of the HF transformer 1890 is center tapped. The center tap 1893 remains coupled to the neutral 1334 line. Optionally, a second low pass filter 1376 is included to remove transients. The secondary 1892 is coupled to the phase 1333 line at point 1380A and the split phase line at point 1380B. It follows naturally that distortion due to the load 1342 can be corrected. Distortion due to the loads 1340 and 1341 may not be completely corrected due to symmetric sink/source current injection from the negative switching circuit 1840 and positive switching circuit 1830 respectively. However when solar energy injection occurs, the current distortion reduces with the ratio of injected solar energy versus distortions generated by all loads in the property.

Figure 13E shows a system 2000' which alleviates the issue of the distortion due to the loads 1340 and 1341 not being completely corrected. The processing capability of the system 2000 can be doubled, including a second processing unit (not shown), which controls a
second positive switching circuit 1830' and second negative switching circuit 1840'. The first
processing unit 1310 of Figure 13A, first positive switching circuit 1830 and first negative
switching circuit 1840 can be configured to correct a distortion in load 1340 between the
phase 1333 and neutral 1334 lines by coupling the secondary 1892 of the HF transformer
across the phase 1333 and neutral 1334 lines. The processing unit 1310 can be configured to
derive a corrective signal for the distortion caused by the load 1340 specifically as described
above in detail (measuring the distorted current, comparing to a reference, etc.) A second
processing unit (not shown) can be configured to derive a corrective signal similarly for the
distortion caused by the load 1341 between the neutral 1334 and split phase 1335 lines. A
second positive switching circuit 1830' and second negative switching circuit 1840' are
coupled to the primary of a second HF transformer 1890'. The secondary of the second HF
transformer 1890' is coupled to the neutral 1334 and split phase 1335 lines. It follows
naturally that the distortion due to the load 1342 coupled between the phase 1333 and split
phase 1335 may not be completely corrected.

To that end, Figure 13F shows a system 2000'' with another layer of processing
capability included for correcting the distortion caused by the load 1342 between the phase
1333 and split phase 1335 lines. An additional processor (not shown) can be configured as
described above to derive a corrective signal for the distortion caused by the load 1342. A
third positive switching circuit 1830'' and a third negative switching circuit 1840'' are
coupled to the primary side of a third HF transformer 1890''. The secondary of the third HF
transformer 1890'' is coupled between the phase 1333 and split phase 1335 lines for
correcting the distortion caused by the load 1342. It is important to note that the
embodiments of Figure 13E and 13F are additive to the embodiment 2000 of Figure 13D.
The embodiments of Figure 13E and 13F are presented in block diagram form for the sake of
clarity. As can be appreciated, the HF transformers can add cost to the system 2000''. To
that end, an alternative embodiment replaces the HF transformers with low pass filters. Two
low pass filters or PWM filters per line will remove the modulating signals from the first,
second and third processing blocks. In such an embodiment, it is preferable to include
galvanic isolation in the DC power source 1810 of Figure 13D, most preferably after the
positive PFC power supply 1814 and the switch 1870.
Figure 14A shows another example of a harmonic distortion correction system 1900. In this embodiment, the harmonic distortion correction system 1900 is able to capture and use the energy in harmonic distortion to correct later distortion. Because distortion is not a dissipative process, i.e. the energy in distortion is not dissipated as heat, it is possible to reshape the current waveform with its own distortion energy when the power network has an average or DC value of substantially zero. Generally, the system 1900 stores distortion energy in a reactive component and releases it at a later time to correct distortion of similar or smaller energy value but of opposite magnitude. Reactive components maybe capacitors or inductors. Although capacitors are described herein, the person of ordinary skill having the benefit of this disclosure will readily appreciate that similar implementations replacing capacitors with inductors can be realized. It is helpful to first look at distorted current waveforms for a graphical representation of the energy that is to be harvested and recycled to correct distortion in later cycles. To that end, Figure 14B and shows a current versus time output graph 1980. The graph 1980 has a current amplitude axis 1981 and a time axis 1982. Three waveforms are represented: a current waveform having harmonic distortion 1986, a reference current 1987 and the difference signal 1988. Three areas under the curve of the difference signal 1988 are of particular interest as they represent distortion energy that can be harvested, stored and later used to correct same or lesser distortion of an opposite amplitude. The first area E1 1983 is negative sum distortion energy, the second area E2 1984 is a positive sum distortion energy, and the third area E3 1985 is again negative sum energy. As this portion of the waveforms represent half a corrective cycle T, identical and opposite harmonic energy appears in the second half of the corrective cycle T. As a result, E4 1983', E5 1984' and E6 1985' are equal and opposite magnitude errors to E1 1983, E2 1984 and E3 1985 respectively and can be corrected by injecting the stored energy of E1 1983, E2 1984 and E3 1985.

Referring back to Figure 14A, storage elements C1 1910, C2 1915 and C3 1920 are provided to store and release the harmonic energy. As in previous embodiments, the system 1900 is coupled between an equivalent property load 1940 and a utility power meter 1901. Processing unit 1920 controls whether the capacitors C1 1910, C2 1915 and C3 1920 are coupled into the system 1900 according to when positive or negative harmonic energy is to be
harvested. The processing unit 1920 comprises an averaging and subtracting portion 1921 which is substantially similar to the several embodiments discussed in detail above; i.e. the averaging and subtracting portion 1921 compares the current in the phase line 1902 with a reference signal and generates a corrective signal accordingly. Additional processing circuitry 1922 is provided to activate either C2 1915 or C3 1920 as they charge or discharge energy and simultaneously charge or discharge corresponding inverse energy from the next half cycle. Each capacitor is charged or discharged by switches 1912, 1917 and 1922. The switches 1912, 1917 and 1922 are controlled by the processing unit 1920 which generates PWM signals according to the error signal 1986 of Figure 14B. The capacitors C1 1910 and C2 1915 can be selectively coupled between a positive voltage line V+ 1907 that carries DC current generated by a positive DC power supply 1905 and the phase line 1902, or between the phase line 1902 and the neutral line 1903 by switches 1913 and 1918 respectively. The capacitor C2 remains coupled in parallel with the equivalent property load 1940. Table 3 shows an exemplary coupling scheme for charging and discharging the capacitors C1 1910, C2 1915 and C3 1920 with respect to the error 1986 of Figure 14B. Table 3 displays the event sequence, which capacitor is being charged or discharged, what the capacitor is coupled to, its status, the energy with which it is charged, and the result of the discharge. Furthermore one more principle must be kept in mind: A capacitor can be charged only by a difference of electrical potential, therefore to charge a capacitor during the half positive cycle it should be connected between a positive high DC voltage such as V+ 1907 for one electrode and the neutral N 1903, the phase P, or a high negative DC voltage V- for the other electrode. The same principle applies for charging it negatively: the capacitor should be connected to V- on one electrode and to N, P, or V+ on the other electrode. In the example of Figure 14A, a negative power supply is not shown for the sake of clarity. However, the person of ordinary skill having the benefit of this disclosure will appreciate that a negative DC voltage can be generated as described, for example, in Figures 4-12D and the corresponding text.

Table 3
<table>
<thead>
<tr>
<th>Sequence</th>
<th>Capacitor</th>
<th>Coupling</th>
<th>Status</th>
<th>Energy</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1</td>
<td>P and V-</td>
<td>charged by V-</td>
<td>E1</td>
<td>Cancel distortion E1 and store energy for canceling E4</td>
</tr>
<tr>
<td>2</td>
<td>C2</td>
<td>P and N</td>
<td>charged by P</td>
<td>E2</td>
<td>Cancel distortion E2 and store energy for canceling E5</td>
</tr>
<tr>
<td>3</td>
<td>C3</td>
<td>P and V-</td>
<td>charged by V-</td>
<td>E3</td>
<td>Cancel distortion E3 and store energy for canceling E6</td>
</tr>
<tr>
<td>4</td>
<td>C1</td>
<td>P and N or P and V+</td>
<td>discharged to N or discharged to P</td>
<td>E4</td>
<td>E1 energy cancels distortion E4 and capacitor depletes its energy to zero.</td>
</tr>
<tr>
<td>5</td>
<td>C2</td>
<td>P and N</td>
<td>discharged to N</td>
<td>E5</td>
<td>E2 energy cancels distortion E5 and capacitor depletes its energy to zero.</td>
</tr>
<tr>
<td>6</td>
<td>C3</td>
<td>P and N or P and V+</td>
<td>discharged to N or discharged to P</td>
<td>E6</td>
<td>E3 energy cancels distortion E6 and capacitor depletes its energy to zero.</td>
</tr>
</tbody>
</table>

The current flowing through C1 1910, C2 1915 and C3 1920 can flow in any direction. The respective PWM controlled switches 1912, 1917 and 1922 are preferably bi-directional switches, for example implemented with two transistors coupled in parallel and reverse (i.e. drain to source and vice versa). Any transistor can be used, including but not limited to bipolar, MOS, IGBT or JFET. Optionally, each capacitor C1 1910, C2 1915 and C3 1920 are respectively coupled to a PWM filter 1911, 1916 and 1921 to filter out the...
modulating signal generated by the processing unit 1920.

In some applications, it is desirable to have simpler topology while simultaneously having the ability to use harmonic energy to correct future harmonic content. To that end, Figure 14C shows a simplified harmonic distortion correction system 1990. The harmonic distortion correction system 1990 corrects a part of all distortion in a power line. In the embodiment shown, distortion correction is effective during the periods of time where the errors E2 1984 and E5 1984' are generated. Stated differently, when the current in the power line is greater than a reference current in absolute value. In some applications, where distortion is otherwise accounted for by, for example, the systems of Figures 4-13, a more simple embodiment such as the embodiment of Figure 14C will suffice. The system 1990 is again coupled between a utility power meter 1901 and an equivalent property load 1940 to a phase line 1902 and a neutral line 1903. One capacitor 1991 is selectively coupled in parallel with the equivalent property load 1940 by a switch 1992. The switch 1992 is controlled by a processing unit 1995. During the half positive period (for example when the error E2 1984 of Figure 14B is formed) when the current in the phase line 1902 is distorted and larger than a reference signal, the capacitor 1991 charges and stores the excess energy that is the distortion content. During the half negative period, the same happens but with the inverse current sign and the capacitor 1991 discharges and acts as a positive supply that counters the negative harmonic energy. Advantageously, the capacitor 1991 is coupled between the phase 1902 and neutral 1903 lines and no other current is flowing to any other potentials or nodes, thereby increasing efficiency. Although single capacitors are generally referred to in the embodiments of Figures 14A and 14C, it is understood that a bank of capacitors can be used.

Figure 14D shows another embodiment of a harmonic distortion reduction system 2000 having the capability of recycling harmonic energy to correct later harmonic distortion. The system 2000 is coupled between a utility power meter 2001 and an equivalent property load. The system 2000 comprises a negative DC power supply 2015 and a positive DC power supply 2010 which are each coupled to the phase 2002 and neutral 2003 lines. A first capacitor 2030 is selectively coupled to the positive DC power supply 2010, negative DC power supply 2015 or the neutral line 2003 by a three position switch 2032. The first capacitor 2030 is also coupled to the phase line 2002. The first capacitor's 2030 charging and
discharging is controlled by a switch 2033 which is in turn controlled by a PWM signal generated by the processing unit 2020. Optionally, a PWM filter 2031 filters the PWM modulating signal generated by the processing unit 2020. A second capacitor 2040 is selectively coupled in parallel with the equivalent property load 2040. Similarly, the second capacitor's 2040 charging and discharging is controlled by a switch 2043 which is in turn controlled by a PWM signal provided by the processing unit 2020. Although PWM control signals are described herein as they are well known and understood to be a highly efficient, any method or means of controlling the switches 2033 and 2043 can be used. A PWM filter 2041 filters out the PWM modulating signal provided by the processing unit 2020. Advantageously, the system 2000 provides a path from at least one energy storage element, in this example the first capacitor 2030, to neutral 2003 so that the element can discharge into the neutral line 2003, effectuating greater efficiency since the storage element is not coupled to the positive DC power supply 2010 or the negative DC power supply 2020 while discharging into the neutral line 2002. Additional embodiments and examples of harmonic distortion correction systems and circuits are listed in U.S. Provisional Patent Application No. 61/435,658, filed January 19, 2011, and incorporated in its entirety.

Alternate Methods of Processing

In the several embodiments above, analog processing to arrive at a corrective signal has generally been discussed. Stated differently, in all of the embodiments, analog components compare, subtract, and modulate to arrive at a corrective signal that controls switches for either selectively sinking or sourcing current or controlling the charge of capacitors for storing and using harmonic energy. However, processing can also be done in the digital domain with the use of Fourier Transforms. The analog signals such as current, voltage, active power, reactive power, phase (current to voltage), zero crossing event, active power THD, reactive power THD, voltage THD, current THD, I_RMS, U_RMS, power factor, or any other useful component of a signal, are digitized by one or more analog to digital converters (ADC). The person of ordinary skill having the benefit of this disclosure will readily appreciate that implementation of digital processing can be done with a DSP processor or ASIC or FPGA, and memory. Several off the shelf processors or arrays are available from Xilinx, Analog Devices, and other providers. Advantageously, such
processors are flexible and allow for partial digital and partial analog processing for greatest

efficiency. Then, the output analog signals are generated by one or more digital to analog

converters (DAC) or derived internally from digital or pseudo-digital signals such as PWM or

otherwise modulated analog signals. Such implementations could also comprise a protection
circuit against over-voltage, over-current, over-power, over temperature and other relevant

input/output parameter values. As is well known, analog signals can be digitized into digital

signals and be manipulated digitally.

In an exemplary method, total current in a phase line having PF and THD impairments

is measured for a number of cycles, quantifized and transformed in the frequency domain

with a FFT or other transform, such as a DFT. An FFT can be processed on a number of

points along the measured total current once per signal period (for instance l/60Hz), or

multiple times a fraction of the times in the period. Both real and imaginary vector results

can be derived. Windowing can be used to decrease the artifact generated in the FFT due to

non-periodic FFT sampling. Any known window such as Hann, Hamming, Blackman,

Cosine, Rectangle, etc. can be used. Preferably, the number of sample values inputted in the

FFT matches an integer time of the current signal period. Doing so decreases and suppresses

the artifacts created in the FFT and reduces the need for windowing, if any, that is desirable

for easier processing and higher FFT frequency or amplitude discrimination. Alternatively,

the number of sample values is equal to a number of periods of the current input signal, for

instance 2 to 50. An ideal current frequency response Iref(f) can be used and rescaled with

the RMS value of the input current. Both complex vectors of size n Iref(f) and Itot(f) are

compared for each index (j = 1,...,n) thereby generating a a complex error vector denoted by

Corr_l(f) = Real {Corr_l(f)} + Im {Corr_l(f)}. A gain, loop filter and other processing may

be applied thereafter. The error vector signal Corr_l(f) can then be converted back to the time

domain, and low pass filtered to avoid aliasing. The filtered error signal can be used as a

modulating signal to modulate the corrective signal. At the same time the positive values of

the error signal permits the modulated error signal to switch ON a sink/source power

transistor. Similarly the negative values of the error signal permits the modulated error signal
to switch ON a source/sink power transistor. The currents from the source and sink

transistors (opposite sign) are added to the summation network power node such as to cancel
the distortion in the power line and a less than ideal PF.

Another method based on digital processing uses the fact that the input signal, the total current, referred to as \( I_{tot}(t) \), is essentially periodic and sufficiently deterministic as to deal with it as a periodic, deterministic signal. We can distinguish three cases: First, when the power network status is quiescent, no appliance is changing status: Current (and voltage) may include phase delay due to reactive loads PF or THD. The current error signal is periodic. Second, when the power network status is slowly varying (speed of change is much slower than the AC power network frequency): one or more appliance may change their status slowly such as a motor establishing to the full rate in 5 seconds. In this case, the signal is periodic in terms of zero-crossing period and in term of almost constant waveform amplitude from period to period. Third, power network status is varying at mid or high speed of change (speed of change is comparable of faster than the AC power network frequency): In this case one or more appliance may change their status such as switching ON or OFF and the signal is periodic in terms of zero-crossing period but is not periodic in terms of waveform shape and amplitude for the duration of the transition.

It is desirable to correct any effect that falls under the first two categories. Effects resulting from the third category can be corrected to the extent of the feedback loop reaction time. By way of example, if the loop feedback reaction time is \( RT \) is 0.2 sec, any event shorter than \( RT \) seconds will fall into category 2 and be corrected. However if faster than \( RT \), the event cannot be corrected for the period of time lower than \( RT \). The current error signal is obtained from the comparison between an ideal current wave and the less than perfect measured current waveform that can be phased shifted and/or include various harmonic distortions. Indeed a standard proportional-integrator-derivative PID controller would not be able to control the loop if the input signal or error input signal varies with time all the time, being neither stationary nor convergent. To that end, a PLL or other zero-crossing detector is implemented to synchronize the process with the input current frequency/phase, for instance 60Hz and in phase. Also, the current signal is quantized into n bits. Then, an error signal is created that is the difference between the input current and a current reference signal. The current reference must be synchronized with the input current signal and normalized with its RMS value. The current reference signal (pure sinewave) can be generated from the voltage
input waveform and rescaled or created internally by a PLL locked with the input voltage waveform. The error input values are stored in a memory line by line such as to have one line being precisely equal to one cycle of the input current. A logic synchronization signal can be generated at each zero crossing event to reset the memory writing to column zero. The sync logic signal can be generated by a PLL or by a zero crossing detector. To capture a complete cycle, only negative to positive transitions may be used (or positive to negative).

Figure 15A shows an implementation of a digital or transform based signal processing block 1500. The block 1500 comprises inputs for signals i(t) and I_RMS. The signal i(t) is a distorted current signal as explained in detail above. The signal I_RMS is a calculated RMS value of the distorted current signal i(t). Both i(t) and I_RMS are optionally gained in programmable gain blocks 1501. The signal i(t) is digitized by a first ADC 1502 forming a digitized distorted signal i(i). The signal I_RMS is digitized by a second ADC 1503. The first ADC 1502 and second ADC 1503 can be in the range of 8 to 16 bits of resolution. ADCs 1502 and 1503 can be configured for a sampling frequency between 0.1 to 10OOKSample/sec. A sampling rate of 10.24KSamples/sec is preferred. That particular sampling rate provides a maximum bandwidth of 5KHz and provides a useful & realistic bandwidth of 4KHz. With 4KHz, feedback loop processing is able to see the input signal up to the 66th harmonic with a signal frequency i(t) of 60Hz and more with 50Hz.

The digitized distorted signal i(i) is then optionally filtered in by a digital filter 1504 forming a filtered digitized distorted signal i(i). The signal I_RMS multiplied by a multiplier block 1508 with a reference current iref(f) generated by a frequency generator 1507. In some embodiments, iref(f) is the fundamental frequency f(0) of i(t). Ire(f) is preferably formed in the frequency domain so there is no additional need for transform processing. Preferably, iref(f) is scaled to the RMS value of the distorted current signal i(i).

The filtered distorted digitized signal i(i) is transformed, for example by FFT, by a transform block 1506 thereby forming a transformed filtered distorted digitized signal i(f). A sampling frequency f(s) for the FFT is generated by a frequency generator 1505. Preferably, f(s) is chosen according to the phase/frequency of the power network voltage input, generally 60Hz for North America and 50 Hz in Europe. FFT can be simplified to a DFT in order to minimize complexity of implementation with 8 to 16 bits depth. An 11 bit FFT is preferred
(2048 input/output complex values). The FFT can be processed on 2 to 50 cycles of the input current waves for maximum frequency resolution. If the input fs generated by the frequency generator 1505 frequency is 60Hz, and the PWM (described below) oscillator frequency is 102.4KHz, 12 periods of 60Hz gives exactly 2048 samples when sampled at 1/10 of 102.4KSample/s, leading to a simplified FFT implementation i.e. a DFT of $2^{11} = 2048$ samples. With a size of 2048, at a rate of 10.24KS/sec, the FFT (DFT) frequency resolution would be 5Hz, providing sufficient granularity to discriminate harmonics from noise and other harmonics (including DC and fundamental frequencies) and provides amplitude value sufficiently accurate for error estimation.

A DFT can be implemented as 2048 inputs/outputs complex numbers of 16 to 128 bits resolution each. One exemplary solution for implementation is 32 bits fixed precision complex numbers. Two ways can be considered to feed the FFT (or DFT) processing block. A first way includes providing i(t) to the FFT at the rate of for instance 10.24KS/sec, so that the transform block 1506 provides updated FFT output results at the same rate of 10.24KS/sec. After filtering and taking into account the Nyquist theorem, the loop bandwidth may be half of the maximum of the sampling frequency f(s). With realistic filtering, a frequency loop bandwidth of 4KHz may be achievable. Therefore in this configuration, any transient, fluctuations, noise and other harmonics may be corrected up to 4KHz. A commercially available DSP processor can provide all processing and transform blocks.

A second way includes presenting the input current data to the FFT function block by block. As discussed previously each block would preferably be synced up with the input current signal frequency, such as 60Hz, in order to minimize FFT artifacts and lesser windowing requirements. With the preferred data above, each block would correspond to the duration of 12 cycles of 60Hz input current that is a duration of 0.2 sec (2048 Samples at a rate of 10.24KS/sec) and a length of 2048 complex values of 98usec each.

The signal I_REF is subtracted from the signal i(f) by a subtractor 1509, thereby forming an error signal e(f), which is a transformed corrective, or error signal. A corrective signal has been discussed in great detail above, and the person of ordinary skill having the benefit of this disclosure will readily appreciate that the guiding principles described herein do not change fundamentally when signal processing is done digitally or in transform. The
signal e(f) is passed through an optional loop filter and gain block 1510 to account for any losses during the subtracting process. Next, the signal e(f) is converted back into an analog corrective signal corr(t) by an inverse transform block 1511. A low pass filter 1512 is provided to remove aliases.

A PLL (phase lock loop) 1520 is provided and locks the phase of an internal clock to the phase/frequency of the power network. An optional VCO is provided for multiplying that locked frequency by any desired multiplier. The PLL 1520 is coupled to a modulator 1515. The modulator 1515 comprises a PWM 1518 that accepts the frequency generated by the PLL 1520, and comprises comparators 1516 and logic 1515, and operates similarly to the modulator 920 of Figure 5. Overvoltage and overcurrent protection can be included.

Alternatively, as shown in Figure 15A’, I RMS input, the second ADC 1503, Iref 1507, multiplier 1508 and substracter 1509 of Figure 15A are replaced with a processing block 1509 primera configured to replace the fundamental component, generally known as {eq}f(0)\), of the transformed digitized filtered degraded signal i(f) with zero. The processing block 1509 prima preferably comprises math blocks for performing mathematical operations on signals such as vector or matrix calculation, index searching, averaging, histogram, etc. Vector or matrix calculation preferably include subtraction and multiplication. The processing block 1509 prima can be integral to a larger processor, such as a DSP, or a discrete device. What remains after the fundamental frequency {eq}f(0)\) (e.g. 50Hz in Europe and 60 Hz in N. America) is removed are the harmonics that correspond to distortion in the time domain. In order to form a corrective signal corr(f), the negative of those harmonics should be derived. To that end, the processing block is configured to multiply the signal i(f) by a negative number, such as negative 1. As a result, the sign of every harmonic is changed. Every harmonic is also scaled if the negative number is not negative 1. What results is a transformed corrective signal e(f). The transformed corrective signal e(f) can be coupled to the inverse transform block 1511 thereby forming the corrective signal corr(t). Corr(t) can be filtered and modulated in the same way described above. Advantageously, this alternative embodiment does not require the use of a reference signal for comparing to the degraded signal. A sampling frequency 1505 can still be derived from the phase voltage u(t). The inverse of the degradation (including harmonics, noise, or anything else) is used as the corrective signal.
Generally, the distorted current signal discussed at length in this disclosure is a periodic signal. Transients or near-step functions are introduced into the current signal when appliances in a building are turned on or off, but otherwise the load current, or the current having distortion which the embodiments taught herein seek to alleviate, can be at least approximated to be periodic. Using this information, a simpler methodology can be implemented for the digitized calculation of a corrective signal.

Figure 15B shows a graph of an exemplary corrective signal corr(t). In some embodiments, corr(t) can be defined as err(t), where err(t) is -corr(t). As described previously, the signal corr(t) is derived from the subtracting of a reference signal and a degraded current signal, either in the time domain or done digitally. Corr(t) is sampled to form a digital error signal e(i). The error signal e(i) can be referred to as a digital corrective signal. The Y axis represents amplitude in milliamperes and the X axis represents time in seconds. While the embodiment of Figure 15A attempted to control aperiodic process with a collection of continuous contiguous samples e(1), e(2), e(3), ..., e(N), a collection of discontinuous streams can be formed and processed as will be described below. Each discontinuous stream is formed by a first sample of a first period, the first sample of a second period, and so on. For example, the waveform corr(t) in the graph 1530 shows a first period T1 and a second period T2. T1 has sampling points e(1), e(2)... e(N) and the second period T2 has sampling points e'(1), e'(2)... e'(N). A third period T3 (not shown) would similarly have the sampling points e''(1), e''(2)... e''(N). A first discontinuous stream comprises the first sample of each period. A second discontinuous stream comprises the second sample of each period, and so on. A first discontinuous stream has the sample points e(1), e'(1), e''(1) for a chosen number of periods, for example 10 periods. One exemplary method to process each of the discontinuous streams separately is to write in a table line by line and read back column by column. At that point each discontinuous stream of data e(i), e'(i), ..., e''(i) with i = 1,2,...,n can be processed separately with a standard loop controller such as a PID controller.

Figure 15C shows an embodiment of a processing block 1550. Similarly to the Block 1500 of Figure 15A, a distorted waveform i(t) is optionally gained by an amplifier 1551 and digitized by an ADC 1552, forming a digitized distorted waveform i(i) that is then optionally
filtered by a filter 1553, forming a filtered digitized distorted waveform \( i(t) \). A signal \( I_{RMS} \) corresponds to the RMS value of \( i(t) \) and is also digitized by an ADC 1552. The voltage of the power network is also accepted as a signal \( u(t) \), digitized by an ADC 1552 and optionally filtered by a filter 1553. A reference signal \( iref(t) \) is formed by a PLL/frequency generation block 1554 according to the phase sync PLLs 1556. The reference signal \( iref(t) \) is digitized to form \( iref(i) \) and is subtracted from the filtered digitized distorted waveform \( i(i) \) by a substracter 1555. The resulting digital corrective signal, alternatively known as a digital error signal \( e(i) \), is fed to a processing block 1560 which is described in further detail below. Alternatively, input processing can be done in analog, forming the analog signal \( corr(t) \) as shown in Figure 15B then digitized by an ADC to form the digital error signal \( e(i) \). The processing block 1560 is an MxN memory and processor capable of comparing and operating on stored data points. The processing block 1560 stores and operates on the incoming data column by column after the data is entered line by line. The output of the processing block 1560 is then converted to analog by a DAC 1571 and modulated by a modulator 1573.

Figure 15D shows a detailed block diagram of the processing block 1560. The processing block 1560 stores the digital signal error input values \( e(i) \) output by the substractor 1555 of Figure 15C in anM x M memory 1561 line by line. Preferably, each line is the discontinuous stream that represents one cycle of the input current. A logic synchronization signal can be generated at each zero crossing event to reset the memory writing to column zero. The sync logic signal can be generated by a PLL or by a zero crossing detector (not shown). To capture a complete cycle, only negative to positive transitions may be used (or positive to negative). A practical sampling rate is in the range of 10 to 50,000 times faster than the current input frequency so for a 60Hz cycle, a value between 0.6KSample/sec and 3MSample/sec. A preferred value is on that satisfies the following formula:

\[
N \times T_{err_i(t)} = T_{err_i(t)} \times f_s
\]

with \( N \) = number of samples in one period \( T_{err_i(t)} \), where \( f_s \) = sampling frequency, and \( T_{i(t)} \) = period of the input signal which is the degraded current signal \( err_i(t) \) as shown in Figure 15B, where \( err_i(t) \) is \( corr(t) \).

As an example, with \( T_{err_i(t)} = 1/60\text{Hz} \), and \( N = 100 \), sampling frequency becomes

-61-
fs = 6.0 Ksample/sec. The memory 1561 is read column by column by an array of controllers 1563. The columns of the memory 1561 can be held by an array of flip flops 1562 that enable once every N samples, with N corresponding to a cycle of the waveform of err_i(t). The array of flip flops 1562 can function as a sequencing means to process e(i) column by column. One controller 1563A per column can be used. The controller array 1563 can be a Proportional Integral Derivative (PUD) or any variation of it (P, I, D, PD, PI), linear control, Kalman filter, fuzzy logic, neuronal, genetic algorithm, adaptive control, AI, machine learning, optimal control, MPC, LQG, robust control, H-infinity loop shaping, stochastic control, or any known or application specific control implementation. Each controller, for example controller 1563A, analyzes for variance between the sampled periods. Controller 1563A analyzes the sample value e(l, j) for j = 1:M, where M is number of total periods sampled. What is achieved is that a variance, if any, between the periods is captured to ensure that the error signal e(i) is indeed periodic. An acceptable variance can be programmed into the controller array 1563 to account for minor and negligible variances from period to period. If there is a variance between the sample value from one period to another, the controller 1563A captures that variance and adjusts the coefficient, or value of the sample accordingly. The output values processed by the controller array 1563 are thereafter latched in a second array of flip flops 1564 and read line by line from a temporary register 1565. The lines, corresponding now to a corrective signal corr(M), are converted back to an analog signal corr(t) by a DAC 1571 of Figure 15D. An anti aliasing filter 1572 follows to remove aliases caused by digital to analog conversion. The modulator 1573 operates as described above in the similar embodiments.

Figure 15E shows another implementation of the processing block 1560 of Figure 15D. Figure 15E shows a processing block 1580 that is further simplified with respect to the processing block 1560. In this exemplary implementation, the controller array 1563 of Figure 15C is reduced to a single controller 1581. The controller 1581 communicates with a memory 1582 for which the status and coefficients of each sample e(i) would be retained in memory and used sequentially one after the other. The coefficients coeff(i) of the corresponding particular sample e(i) produces an output corrective signal point corr(i). In this implementation, one sample of e(i) per clock is needed at any time to generate a coeff(i). The
controller 1581 may be sampled at the same rate as e(i) in the embodiment of Figure 15C or may be sampled at a faster rate in order to increase the computation granularity and/or accuracy. This solution provides a faster feedback loop response and at the same time less feedback loop delay thereby improving the dynamic performance of the overall distortion and PF compensation system.

Figure 15F shows a process flow 2100 for digital correction of a signal having distortion. In one aspect, the process flow 2100 corresponds to the schematic block diagram of Figure 15A. In a first step 2110, a degraded current signal i(t) is measured. In a step 2111, a corresponding voltage u(t) is measured. I(t) and u(t) can be current and corresponding voltage of a power delivery system, for example to a residence. It is understood that complex loads in a power delivery system distort a current signal i(t) with harmonics and/or noise. I(t) and u(t) can be measured for a set number of periods or cycles. In a step 2112, an RMS value, referred to previously as I_RMS in some embodiments, of the degraded current signal i(t) is calculated, measured, or otherwise derived. In a step 2113, a transformed reference signal iref(f), which corresponds to the fundamental frequency f(0) of u(t) is derived from the measured u(t). In step 2020 i(t) is digitized to form i(i). In step 2021, f(0) and I_RMS are used to derive a transformed reference signal iref(f). In some embodiments, iref(f) is scaled to I_RMS. In a step 2022, i(i) is transformed from the time domain to the frequency domain by FFT, DFT, or any other useful transform function to form the transformed degraded current signal i(f). An FFT is processed on a number of sampled points in the digitized signal i(i) that can be any integer or non-integer multiplier of a reference frequency, such as f(0). Both real and imaginary vectors resulting from the transform are taken into account. A windowing function is generally needed to decrease the artifact generated in the FFT due to non-periodic FFT sampling. Windowing such as Hann, Hamming, Blackman, Cosine, Rectangle, etc. can be used. Preferably, a window length is the integer N, wherein N is the number of sample values in a period of i(t). Alternatively, N can be any integer number of periods. Such an implementation decreases/suppresses any artifacts resulting from the FFT and reduces the requirement on the windowing if any, resulting in easier processing and higher FFT frequency/amplitude discrimination.

In a step 2025, the transformed i(f) is subtracted from the reference signal iref(f),
thereby forming a transformed error signal $e(f)$. In some embodiments, both complex vectors of size $N$ $I_{\text{ref}}(i)$ and $I(i)$ are compared for each index $(j = 1, \ldots, n)$ thereby forming a complex error vector $e(i) = \text{Real}(e(i)) + \text{Im}(e(i))$.

In a step 2027, an inverse transform is applied to the transformed error signal $e(f)$ to form a time domain corrective signal $\text{corr}(t)$. Optionally, filtering and gain is applied in the frequency domain as well. In a next step 2028, the signal $\text{corr}(t)$ is modulated to correct distortion as explained in detail above.

Figure 15G is an alternate process 2130 for deriving a corrective signal $\text{corr}(t)$. In one aspect, the process 2130 corresponds to the circuit diagram shown in Figure 15C. In steps 2131 and 2132 the degraded signal $i(t)$ and voltage signal $u(t)$ are measured respectively. In a step 2133, an RMS value of $i(t)$ is derived or measured. In a step 2140, $i(t)$, $u(t)$ and $\text{irms}(t)$ are digitized to form $i(i)$, $u(i)$ and $\text{irms}(i)$. In a step 2141, a frequency of $u(i)$ is used to derive a reference signal $\text{iref}(i)$ as described in detail above, such as by phase locking onto the frequency of $u(i)$ and multiplying by an integer to generate a desired reference frequency $\text{iref}(i)$. In a step 2142, $\text{iref}(i)$ is multiplied by $\text{irms}(i)$ to form a scaled reference frequency.

In a step 2150, $i(i)$ and $\text{iref}(i)$ are used to derive a corrective signal $\text{corr}(i)$. In some embodiments, $i(i)$ is subtracted from $\text{iref}(i)$ to form the digital corrective signal $e(i)$. Then, $e(i)$ is stored line by line in an $N \times M$ memory bank, where $N$ is a number of samples in a period of $i(t)$ and $M$ is a total number of periods sampled. The $N \times M$ memory is read column by column, and each index of each sample is compared to a corresponding index by an array of processors. For example, an index corresponding to a first sample of a first period is compared to an index corresponding to a first sample of a second period. Any difference between the two are captured and analyzed to ensure that the signal $e(i)$ is periodic. An acceptable variance can be included to account for transients. The signal $e(i)$ is read column by column and stored in an $N$ length register. Alternatively, rather then processing column by column and using an array of processors or controllers, the status and coefficients of each sample $e(i)$ are be retained in memory and processed sequentially. The coefficients $\text{coeff}(i)$ of the corresponding particular sample $e(i)$ produces a digital corrective signal $\text{corr}(i)$. In a step 2160, the digital corrective signal, however formed, is converted to analog by a DAC, thereby
forming corr(t). In a step 2170, corr(t) is modulated and coupled to the power system as described in detail above for correcting a degraded current signal. The person of ordinary skill having the benefit of this invention will readily appreciate that the processes discussed in Figures 15F and 15G need not be the order presented. Calculations can be done in the time domain, frequency domain, digitized, or analog as applications require or cost, time, power consumption, or other factors are considered.

Figure 15H is a process flow 2200. In one aspect, the process flow 2200 corresponds to the schematic diagram of Figure 15A'. In a first step 2210, a degraded current signal i(t) is measured and digitized in a step 2220 forming the digitized degraded current signal i(i). In a next step 2230, the digitized degraded current signal i(i) is transformed, for example by FFT to form the transformed degraded signal i(f). A transform sampling rate should correspond to a fundamental frequency of the digitized degraded current signal i(t). To that end, in a step 2239, the fundamental frequency f(0) of i(t) is derived, either by analyzing i(t) or u(t). Any other transform can be used. In a step 2240, the fundamental frequency f(0), for example 60Hz in North America and 50 Hz in Europe, is removed, leaving only the harmonics. In a next step 2250, a negative of the transformed degraded signal i(f) is taken, for example by multiplying by negative 1 thereby forming a transformed corrective signal corr(f). If a scaling is desired, any other negative number can be used. In steps 2260 and 2270, filter gain, loop gain, and an inverse transform are applied thereby forming a corrective signal corr(t). In some embodiments, a low pass filtering step 2280 is applied to remove any aliasing. In a step 2290, the corrective signal is modulated as described above in detail.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be readily apparent to one skilled in the art that other various modifications are able to be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention as defined by the claims.
CLAIMS

What is claimed is:

1. In a power delivery system, a system for reducing distortion in a signal having distortion comprising:
   a. an input for receiving the signal having distortion,
   b. a first analog to digital converter for converting the signal having distortion into a digital signal having distortion,
   c. a frequency generator for generating a reference signal according to the signal having distortion;
   d. a processor for generating a corrective signal based upon the digital signal having distortion, and
   e. an electric circuit for selectively sinking and sourcing current to the signal having distortion according to the corrective signal to correct the distortion.

2. The power delivery system of Claim 1 wherein the processor comprises:
   a. a transform block for transforming the digital signal having distortion, thereby forming a transformed signal having distortion;
   b. a math block for removing a fundamental frequency of the transformed signal having distortion and multiplying the transformed signal having distortion with negative number thereby forming a transformed corrective signal; and
   c. inverse transform block for forming a corrective signal.

3. The power delivery system of Claim 2 wherein the transform block comprises an FFT block, a DFT block, or a discrete cosine transform block.

4. The power delivery system of Claim 1 further comprising one of a second analog to digital converter for converting the reference signal into a digital reference signal.

5. The power delivery system of Claim 1 wherein the reference signal comprises a
transformed reference signal.

6. The system of Claim 4 wherein the frequency generator is configured to generate a reference based upon an RMS value of the signal having distortion.

7. The system of Claim 4 wherein the frequency generator is configured to generate a reference based upon a frequency of the signal having distortion.

8. The system of Claim 4 wherein the frequency generator is configured to generate a reference based upon the frequency at which the power delivery system operates.

9. The system of Claim 5 wherein the processor comprises:
   a. a first input for receiving the digital signal having distortion;
   b. a second input for receiving the digital reference signal;
   c. a subtracter for subtracting the digital reference signal from the digital signal having distortion, thereby forming a digital corrective signal; and
   d. a digital to analog converter for converting the digital corrective signal to the corrective signal.

10. The system of Claim 4 wherein the processor comprises:
    a. a first input for receiving the digital signal having distortion;
    b. a transform block for applying a transform function to the digital signal having distortion, thereby forming a transformed digital signal having distortion,
    c. a second input for receiving a transformed digital reference signal;
    d. a subtracter for subtracting the transformed digital reference signal from the transformed digital signal having distortion, thereby forming a transformed corrective signal; and
    e. an inverse transform block for applying an inverse of the transform function to the transformed digital corrective signal thereby forming the corrective signal.
11. The system of Claim 4 wherein the signal having distortion is periodic, and the processor comprises:
   a. a first input for receiving the digital signal having distortion;
   b. a second input for receiving the digital reference signal;
   c. a subtracter for subtracting the digital reference signal from the digital signal having distortion, thereby forming a digital error signal,
   d. a processor processing the digital error signal, and
   e. a digital to analog converter for converting the digital corrective signal to the corrective signal.

12. The system of Claim 11 wherein the processor comprises:
   a. a memory bank having N rows and M columns, wherein N is a number of samples taken in one period of the signal having distortion and M is a number of periods of the signal having distortion sampled;
   b. a sequencing means for writing the error signal line by line into the memory bank; and
   c. a register for storing an M length string of the digital corrective signal.

13. The system of Claim 12 wherein the processor further comprises an array of N controllers, wherein each controller is configured to compare a sample of a first period to a corresponding sample in a second period, wherein each controller is configured to keep a value of a sample a difference between a sample of a first period and a corresponding sample in a second period is within an acceptable range.

14. The system of Claim 11 wherein the processor comprises:
   a. an input for receiving the digital error signal;
   b. an input for receiving coefficients of the digital error signal;
   c. a controller for sequentially analyzing the coefficients to ensure that the digital error signal is periodic; and
   d. an N length memory for storing the coefficients, where N is the number of
samples in one period of the digital error signal.

15. The system of Claim 14 wherein the controller is further configured to output the
digital corrective signal sequentially.
Utility Power Meter

Phase 110VAC Neutral

Measure Phase Current (e.g. Insulated)

3.3V Power Supply

Measure Phase Voltage (e.g. Insulated)

Power Supply Voltage (e.g. Insulated)

1-phase 2-wires Reactive Power Meter, Zero Crossing Detector, Sag detector, Over-voltage detector incl. communication

Micro-Controller Unit to Process data, reactive load algorithm and control, LED Display, interface with optional comm. module, etc.

Optional Communication to other modules (Wireless or Wired)

Optional Wireless Communication Port

Optional wired LAN, parallel or Serial Port

Fig. 2

Power Factor Correction System preferred impl. #1

Optional filter(s)

Phase 110VAC

TRIAC driver

TRIAC driver

209A

209B

208A

208B

210A

210B

213

212
Fig. 13C
Fig. 14A
Fig. 15D

**Array of Registers (memories)**

Enable once every N sample after controllers are done (store values in registers)

**Array of Controllers**

Enable once every N sample only

**Input signal** $e(i)$

$e(N,M)$ $e(N-1,M)$ $\cdots$ $e(3,M)$ $e(2,M)$ $e(1,M)$

$e(N,M-1)$ $e(N,M-2)$

$N \times M$

**Memory**

$\cdots$

$e(1,3)$ $e(1,2)$

$e(N,1)$ $e(N-1,1)$ $\cdots$ $e(3,1)$ $e(2,1)$ $e(1,1)$

**Single Digital Controller:**

Load coeffs(i). Computes Corr(i) & Updated coeffs(i) w/ coeffs(i) for each $e(i)$

Read coeffs(i) for each i, with $i = 1, \ldots, N$

When $i = N$, force $i+1 = 1$

**Output signal** Corr(i)

1 sample at a time

**Digital Controller may be PID or else.**

Memory, size $N$: coeffs(i)

Fig. 15E
INTERNATIONAL SEARCH REPORT

International application No. PCT/US2012/021915

A. CLASSIFICATION OF SUBJECT MATTER

G05F U66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F U66; H02J 1/02; H02M 7/00; H02M 7/02; H03F 1/00; H03K 7/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic database consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: power factor corrector, distortion, active harmonic filter, digital

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>US 05977660 A (JOHN N. MANDALAKAS et al.) 02 November 1999</td>
<td>1-15</td>
</tr>
<tr>
<td></td>
<td>See column 2, line 1 - column 5, line 15, and figures 1, 2, 5a-5c</td>
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<td>See page 2, line 2 - page 3, line 12, and figure 1</td>
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<td>See figure 7</td>
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</tbody>
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"A" document defining the general state of the art which is not considered to be of particular relevance
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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Further documents are listed in the continuation of Box C. × See patent family annex.

Date of the actual completion of the international search 04 MAY 2012 (04.05.2012)

Date of mailing of the international search report 07 MAY 2012 (07.05.2012)

Name and mailing address of the ISA/KR Korean Intellectual Property Office
Government Complex-Deajeon, 189 Cheongsa-ro, Seo-gu, Daejeon 305-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
Park Kee Yong
Telephone No. 82-42-481-8707

Form PCT/ISA/210 (second sheet) (My 2009)
<table>
<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
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<th>Publication date</th>
</tr>
</thead>
<tbody>
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<td>02.11.1999</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>KR 10-2006-0046389 A</td>
<td>17.05.2006</td>
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<td>07.06.2006</td>
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<td></td>
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<td>AU 2003-286569 A8</td>
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</tbody>
</table>