Title: CIRCUIT FOR THE PARALLEL SUPPLYING OF POWER DURING TESTING OF A PLURALITY OF ELECTRONIC DEVICES INTEGRATED ON A SEMICONDUCTOR WAFER

Abstract: The present invention relates to a circuit architecture for the parallel supplying of power during an electric or electromagnetic testing, such as EMWS or EWS or WLBI testing, of a plurality of electronic devices (2) each integrated on a same semiconductor wafer (1) wherein the electronic devices (2) are neatly provided on the semiconductor wafer (1) through integration techniques and have edges (5) bounded by separation scribe lines (7). Advantageously according to the invention, the circuit architecture comprises: - at least one conductive grid (4), interconnecting at least one group of the electronic devices (2) and having a portion being external (13) to the devices of the group; the external portion (14) of the conductive grid (4) being extended also along the separation scribe lines (7); the internal portion (13) being extended within at least a part of the devices of the group; interconnection pads (6) between the external portion (14) and the internal portion (13) of the conductive grid (4) being provided on at least a part of the devices of the group, the interconnection pads (6) forming, along with the internal and external portions, power supply lines which are common to different electronic devices (2) of the group.
DESCRIPTION

Field of application

The present invention relates to a circuit architecture and a method for solving the problem of the parallel supplying during the testing steps, in particular electromagnetic (EMWS) testing, of a plurality of electronic devices integrated on a semiconductor wafer and arranged in parallel on said wafer.

The invention further relates to creating connections between the various devices on the wafer, for then using them during the testing of the wafer itself to supply them, due to the non-negligible power required by the operation of the devices themselves.

The invention particularly, but not exclusively, relates to applications of a process of electric (EWS) and/or electromagnetic (EMWS) selection and/or wafer level burn-in (WLBI) intended for the quality control in the manufacturing of electronic devices integrated on semiconductor wafer.

Prior art

As it is well known in this specific technical field, to carry out an electric selection of electronic devices integrated on a semiconductor wafer (testing EWS) it is necessary to electrically connect a testing apparatus, i.e. a tester which carries out the measurements, to a wafer whereon components, devices or electronic circuits have been realised according to known processes of semiconductor monolithic integration.

To realise this connection between the testing apparatus and the wafer an interface is provided known as "probe card". This interface is substantially an electronic board essentially constituted by a PCB and by some hundreds (sometimes thousands) of probes which electrically connect the tester to ends known as pads of the integrated electronic devices to be tested.

A known type of electric testing on wafer is WLBI (Wafer Level Burn-In) and is used to check the reliability of a device by using test conditions at particularly high activation energies (in relation to the
specific device and to the technology used for realising it) to accelerate the failure mechanisms.

One of the several known solutions of WLBI testing has been developed in Motorola and is described in an article:


This article takes into consideration the creation of metallic connections on the wafer which connect to each other groups of electronic devices in a clusters architecture.

These metallic connections, that could be also considered as grids, are realised outside the various devices by overlapping, at the end of the manufacturing step, strips of sacrificial metal thereon. These strips are removed and completely eliminated by means of an acid etching at the end of the WLBI testing operations, to allow to carry out an electric testing on each single electronic device.

Some studies are currently ongoing to carry out a testing of the electromagnetic type (and at the most wireless), even during the step of manufacturing the devices so as to avoid, as much as possible (and at the most to completely avoid) the use of the probes of the testing apparatus. These studies are focused towards carrying out a parallel testing onto a plurality of devices or onto a whole wafer.

In fact, although advantageous under several aspects, and substantially meeting the aim, the probes which connect the tester to the wafer have some drawbacks; for example, they can lead to a damaging of the pads of the electronic devices selected for the testing. This damaging can cause problems in the assembly of the electronic devices that have passed the quality control at the end of the testing.

Moreover, for the electric or electromagnetic selection of said plurality of electronic devices, carried out in parallel, probe cards with a very high number of probes are used. This implies an increase of the contacting problems, and thus an increase of the electric continuity problems between the probe card and the wafer, or, better, between the probes and the pads of the electronic device, with subsequent problems of loss of electric performance.
Other problems are due to the mechanical limits of last generation state-of-the-art electronic devices, which have a high number of pads to be contacted, or have pads of reduced area, or even pads which are often very close to each other.

In case it is possible, in the future, to pass from completely electric testing mode to electromagnetic (completely or in part) testing mode, the introduction in each device of reception and transmission circuits is provided, so called transceivers or transponders. This will imply an increase of area of each electronic device, even if this need is to be considered unavoidable.

By using an electromagnetic testing the number of probes of the current testing apparatuses will be reduced or even eliminated.

However, the parallel electric or electromagnetic testing of a plurality of devices arranged on a single wafer, raises the problem of how to supply them enough to operate under testing conditions.

Obviously, when the testing parallelism increases, in consequence the power that the electromagnetic testing will have to use for the simultaneous supply of the various devices will increase.

In substance, the problem of supplying the various electronic devices which are tested in parallel is tied to the fact that these devices should operate simultaneously during the testing.

The technical problem underlying the present invention is that of providing a circuit architecture, and a corresponding method, to supply in parallel a plurality of electronically devices monolithically integrated on a single semiconductor wafer and intended to be tested in parallel, i.e. when all the devices operate simultaneously and the power they require can also be relatively high.

**Summary of the invention**

The solution idea of the present invention is that of realising electric connections between various electronic devices integrated on the wafer so as to create common power supply lines (and possibly also signal lines) which, if brought to a suitable biasing voltage, allow the devices to operate simultaneously.

The solution idea consists in realising electric connections between the various electronic devices on the wafer which can be used as
common power supply lines but avoiding to impact as much as possible on the project or on the design of the electronic devices. These common power supply lines can be realised by means of some conductive grids realised in the so called "scribe line" of the wafer, i.e. in the separation area which separates a device from the other.

The creation of these common power supply lines (and possibly signal lines) may add one or more diffusion masks with respect to those already provided in the manufacturing process of the electronic devices.

To supply the common power supply lines, one can exploit physical connections, between the power supply and the wafer itself.

All the electronic devices realised on a same wafer can have common connections, or be assembled with each other in groups with common connections only at the dice of the same group, or there can also be a mixed situation.

On the basis of the above solution idea, the technical problem is solved by a circuit architecture for the parallel supplying of power during an electric or electromagnetic testing of a plurality of electronic devices each integrated on a same semiconductor wafer wherein said electronic devices are neatly provided on said semiconductor wafer through integration techniques and have edges bounded by separation scribe lines characterised in that it comprises:

- at least one conductive grid, interconnecting at least one group of said electronic devices and having a portion being external to the devices of said group and a portion being internal to the devices of said group;
- the external portion of said conductive grid being extended also along said separation scribe lines;
- the internal portion being extended within at least a part of the devices of said group;
- interconnection pads between said external portion and said internal portion of said conductive grid being provided on at least a part of the devices of said group, said interconnection pads forming, along with said internal and external portions, power supply lines which are common to different electronic devices of said group.

Advantageously, each electronic device of said at least one group
thus comprises at least one additional power supply pad (and/or possibly signal pad) in correspondence with at least one edge of the electronic device for the connection with the external portion of said conductive grid.

Moreover, the use is provided of a plurality of additional power supply pads (and/or possibly signal pads), at least one at each edge of the electronic devices of said at least one group.

A noteworthy fact is that the above external portion is a bridging electric connection between at least one couple of pads of adjacent electronic devices; while the internal portion is an electric connection between at least two pads of a same electronic device.

In particular, according to an aspect of the invention, each electronic device of said at least one group comprises at least a power supply pad at the edge of the electronic device for the connection with the external portion of said conductive grid.

According to another aspect of the invention, a plurality of said power supply pads may be provided, at least one at each edge of the electronic devices of said at least one group.

Moreover, according to yet another aspect of the invention, said external portion may be an electronic bridging connection between at least one couple of power supply pads of adjacent electronic devices.

Also, according to another aspect of the invention, said internal portion may be an electric connection between two interconnection and power supply pads of a same electronic device.

According to an aspect of the invention, said internal portion may be formed by a Crossing technique.

Moreover, according to an aspect of the invention, said external portion may be formed by a Bridging technique.

According to another aspect of the invention, at least one part of said external portion may be realised in the scribe lines region separating an electronic device to another.

Moreover, according to an aspect of the invention, the circuit architecture, further comprising an insulating layer positioned on one of said scribe lines, is characterised in that said external portion comprised at least one metal layer deposited on said at least one
insulating layer which extends between two adjacent interconnection pads of two adjacent electronic devices.

According to another aspect of the invention, said part of said external portion in the scribe lines region comprises at least one metal layer deposited on a layer of filling insulating material extending within said scribe lines, at least partially filling said scribe lines.

Furthermore, according to yet another aspect of the invention, said interconnection pads may comprise power supply dummy pads and signal dummy pads.

According to another aspect of the invention, said external portion and said internal portion of said conductive grid may be orthogonal to each other.

Moreover, according to an aspect of the invention, at least one of said external portion and said internal portion of said conductive grid may be realised by a conductive line which is buried in at least one of said electronic devices or of said semiconductor wafer.

According to another aspect of the invention, said external portion and said internal portion of said conductive grid may be insulated from each other at crossover points.

In particular, at least one vias connection may be provided to contact said buried conductive line.

Advantageously according to another aspect of the invention, the circuit architecture further comprises at least one fuse link connected to at least one conductive grid.

Moreover, the circuit architecture may further comprise at least one fuse link included into said at least one conductive grid.

The above stated technical problem is also solved by a method comprising the steps of:

- forming scribe lines on a semiconductor wafer;
- forming a plurality of electronic devices integrated on said semiconductor wafer separated from each other by said scribe lines;
- forming a respective plurality of interconnection pads on each electronic device respectively;
- forming a conductive grid on said semiconductor wafer, said step of forming said conductive grid including the steps of:
forming an external portion of said conductive grid along said scribe lines;
forming an internal portion of said conductive grid within said electronic devices; and
connecting an interconnection pad of each electronic device to an interconnection pad of a respective adjacent electronic device and to said conductive grid to form power supply lines common to said electronic devices.

According to an aspect of the invention, said step of forming said internal portion may comprise electrically connecting two interconnection pads of a same electronic device.

Moreover, according to another aspect of the invention, the method further comprises a step of supplying a voltage to all of said electronic devices simultaneously through said conductive grid.

Finally, the method may comprise a step of simultaneously testing of said electronic devices.

for the parallel supplying of power during an electric or electromagnetic testing of a plurality of electronic devices being integrated on a semiconductor wafer wherein said electronic devices are neatly provided on the wafer through integration techniques, and have edges bounded by separation scribe lines, characterised in that it comprises:

- at least one conductive grid, interconnecting at least one group of said electronic devices and having a portion being external to the devices of said group and a portion being internal to the devices of said group;
- the external portion of said conductive grid being extended along said separation scribe lines;
- the internal portion being extended within at least a part of the devices of each group;
- interconnection pads between said external portion and said internal portion of said conductive grid being provided on at least a part of the devices of each group for forming, along with said external and internal portions, power supply lines which are common to the various electronic devices of a group.
The characteristics and the advantages of the circuit architecture and of the method according to the present invention will be apparent from the following description of an embodiment thereof given by way of indicative and non limiting example with reference to the annexed drawings.

**Brief description of the figures**

- figure 1 shows a schematic view of a semiconductor wafer portion incorporating a plurality of electronic devices realised according to the prior art;
- figure 2 shows a schematic view comparing a standard electronic device with an electronic device provided with a so called transponder circuit portion;
- figure 3 shows an enlarged scale schematic view of some electronic devices on the wafer of figure 1;
- figure 4 shows a schematic view of a group of electronic devices realised on a semiconductor wafer and provided with a circuit architecture according to the present invention;
- figure 5 shows a schematic view, similar to that of figure 1, of a semiconductor wafer whereon some electronic devices of figure 4 are realised and subjected to testing operations;
- figure 6 shows a schematic view of a single electronic device provided with a circuit architecture according to the present invention;
- figure 7 shows a more detailed schematic view of the connections between the device of figure 6 and other similar devices, according to the present invention;
- figure 8 shows a more detailed schematic view of some electric connection modes inside the electronic devices of figure 6 and being part of the circuit architecture of figure 7;
- figure 9 shows an enlarged vertical section schematic view of a portion of the circuit architecture according to one embodiment of the invention;
- figure 10 shows an enlarged vertical section schematic view of one embodiment of the circuit architecture portion of figure 9;
- figure 11 shows an enlarged vertical section schematic view of one embodiment of the circuit architecture of figure 9;
- figure 12 shows a schematic view of a group of electronic devices realised on a semiconductor wafer and provided with a circuit architecture according to one embodiment of the present invention;
- figure 13 shows an enlarged vertical section schematic view of a circuit architecture portion on the semiconductor wafer of figure 12;
- figure 14 shows a schematic view of a group of electronic devices realised on a semiconductor wafer and provided with a circuit architecture according to one embodiment of the present invention;
- figures 15 and 16 show an enlarged vertical section schematic view of a circuit architecture portion on the semiconductor wafer of figure 14;
- figure 17 shows a schematic view of a group of electronic devices realised on a semiconductor wafer and provided with a circuit architecture according to one embodiment of the present invention;
- figure 18 shows a schematic view of a group of electronic devices realised on a semiconductor wafer and provided with a circuit architecture according to one embodiment of the present invention;
- figure 19 shows an enlarged vertical section schematic view of a circuit architecture portion on the semiconductor wafer of figure 18;
- figure 20 shows a schematic view of a group of electronic devices realised on a semiconductor wafer and provided with a circuit architecture according to one embodiment of the present invention;
- figure 21 shows an enlarged vertical section schematic view of one embodiment of the circuit architecture of figure 9.

Detailed description

With reference to these figures, and in particular to the example of figure 1, a wafer of semiconductor material is globally and schematically indicated with 1, several semiconductor electronic devices 2 being neatly provided on a surface of the same according to known monolithic integration techniques.

The wafer 1 is housed on a support 12 which allows electrical connection of the lower or back surface of the wafer, on which the electronic devices 2 are realised, to a reference potential, for example a signal ground or a power supply.

The structure, nature and operation mode of the electronic devices
2 goes beyond the content of the present invention. The sole noteworthy-
peculiarity is that the electronic devices 2, the present invention is
intended for, are those shown in figure 2 and provided with a circuit
portion 11 of the transceiver or transponder type which can be used for
transmitting electric/electromagnetic signals from and towards the
electronic device 2 with or without a direct contact or in the so called
wireless mode.

One embodiment of the invention relates to a circuit architecture
for the parallel supplying of power during the electromagnetic (EMWS)
or electric (EWS) testing steps to a plurality of said electronic devices 2
integrated on the semiconductor wafer 1 and provided with at least one
transceiver or transponder 11.

Hereafter in the description and in the drawings the electronic
devices 2 will be also identified with the acronym DUT (Device Under
Test), as shown in figure 3.

According to one embodiment of the present invention, to supply a
sufficient electric power supply so as to make a plurality of devices 2
operative during the EMWS testing step, first the creation of some
conductive grids 4 on the wafer 1 is provided. The conductive grid 4 can
be realised with metallic material or semiconductor material or, in
general, with a conductive material.

Figure 4 shows an example of conductive grid 4 according to one
embodiment of the present invention, together with an embodiment of
the circuitual architecture always according to the invention.

Alternatively, a single conductive grid 4 could be provided
according to the physical structure of the electronic devices 2 and to
their modes of realisation and hauling onto the wafer 1.

The grids 4 comprise a portion 14, illustrate in figure 7, being
external to the various electronic devices 2 and a portion 13, illustrated
in figure 8, being internal to the same electronic devices 2. The external
portion 14 of the grids is realised in part inside a so called scribe line 7,
i.e. inside a separation line or lowered area which physically separates
each electronic device 2 from the other.

In substance, each electronic device 2 is delimited and surrounded
by scribe lines 7 which extend orthogonally to each other on the whole
A given conductive grid 4 interconnects a group of said electronic devices 2 by means of a portion or interconnection network 14 being external to the devices 2 of said group and a portion or interconnection network 13 being internal to the devices of said group.

For example, figure 7 shows a solution wherein the devices 2 are connected to each other by means of the external portion 14 of a conductive grid 4, which forms external connections, in particular bridging connections, which involve at least one pad 6 of a device 2 and at least another pad 6 of an adjacent device 2.

The external portion 14 of said conductive grid 4 is extended and crosses said separation scribe lines 7, while the internal portion 13 of the same conductive grid 4 is extended inside at least a part of the electronic devices 2 of each group.

Advantageously according to one embodiment of the invention, to connect an electronic device 2 to a corresponding grid 4 at least one additional or dummy power supply pad 8 is suitably provided at an edge 5 of the electronic device 2, as shown in figure 6. More in particular, one embodiment of the invention also provides of a plurality of power supply pads 8, at least one for each side 5 of the electronic device 2 so as to easily connect each pad 8 to the closest adjacent conductive grid.

The dummy pads 8 can be externally connected to pads 6 already on the electronic devices 2.

The pads 6 or 8 being on a given electronic device 2 and connected to a same grid 4 are also connected to each other, inside the electronic device, through the internal portion 13 of the grid 4, which forms internal connections of various type. For example, the internal electric connections between the pads 6 or 8 are suitably of the Crossing type, and extend inside each device 2 between at least two pads 6 or 8, or 6 and 8.

While the Crossing is realised inside each electronic device 2, the Bridging is created outside the various electronic devices 2 crossing, or better overlapping, also the separation scribe lines 7 between the various devices on the wafer.
It is conceptually possible to use some signal or power supply routings being already inside the electronic devices 2, but with respect to the known solutions the embodiments of the present invention however may provide the arrangement of some additional pads 6 in well defined positions which can serve to abut internal connections 13 or external connections 14.

By using a mixed solution of external connections 14 and internal connections 13, like the previously shown bridging connection 14 and crossing connections 13, it is possible to supply each device with also two or more different power supplies Vcc1 and/ or Vcc2 or ground GND voltage values, as well as with other electric signals such as for example the clock signal CK. Everything is well shown in figure 5.

In the case shown in figure 5, at least three distinct conductive connections will be necessary, one for the first supply Vcc1; one for the second supply Vcc2 and one for the clock signal CK.

The connection to a power supply ground can be ensured by the testing apparatus which provides an electric connection to ground for the lower surface of the wafer 1, or this ground connection can be created with a further grid 4.

Going back now to the structure of the external portion 14 of the conductive grids 4, with the help of figure 9 it can be understood how it is possible to realise the external connections 14 of the Bridging type by exploiting also the separation scribe line between a device 2 and the adjacent device 2.

Figure 9 clearly shows a peripheral additional pad 8 (power pad) of a device 2, indicated with DUT A, and a similar pad 8 of a second and adjacent device 2, indicated with DUT B, connected to each other by means of a bridging connection 14 formed above a passivation layer 15 which protects an underlying dielectric layer 16 (oxide).

The external connections 14 are realised in the final steps of the diffusion process, or with a dedicated post-processing step, and can then also be removed at the end of the testing step.

Since the bridging should cross the scribe lines 7, which are normally lowered with respect to the upper surface of the electronic devices, it may be desirable to fill in these scribe lines 7, completely or
in part, with electrically insulating, refractory filling material. In this way one contributes to reduce the faultiness in the scribe lines 7 themselves and makes the creation of the Bridging connections 14 easier.

In fact, in a further embodiment shown in figure 10, the bridging connection 14 is deposited above a layer 17 of filling insulating material, for example an oxide, expressly provided as partial filler of the lowered region of the scribe line 7.

If instead there is no difference of level between the surface of the scribe lines 7 and the surface of the various electronic devices 2, the realisation of the connections 14 can occur also without a precautionary deposition of filling insulating material 17.

In fact, in case the scribe line 7 is not lowered with respect to the at sight surface of the electronic devices 2 realised on the wafer 1, the external connection 14 can be flat and completely extended above the passivation layer 15, as shown in figure 11.

Going now back to the internal Crossing connections 13, we can consider them like the internal portion 13 of each device 2 of the conductive grid 4.

The technical expert in the field understands that it is possible to arrange the Crossing in different ways, according to the circumstances. For example, a possible configuration for the Crossing considers that inside the electronic device 2 the pads 6 or 8 of the same type, i.e. of signal or of power supply, are all connected to each other, so as to reduce the overall number of probes necessary for the supplying.

Advantageously, the various electronic devices 2 arranged on a same wafer 1 are, according to one embodiment of the invention, connected to each other outside the devices themselves, by exploiting the dummy pads 8 and the connections 14; while, the internal connections 13 between the same pads 8 will ensure the electrical continuity of a given conductive grid 4.

The Bridging connections 14 will have the possibility of being eliminated in any case after the testing step or after the cut of the wafer 1 for the physical separation of the electronic devices 2 so as to encapsulate each electronic device 2 inside a respective containment
and protection package.

To supply the various conductive grids 4 traditional probes can be exploited being used by the apparatuses arranged for the electric testing on wafer, and possibly, for a same power supply, a plurality of dummy probes can be used.

The presence of this plurality of dummy probes allows to supply all the power required by the operation of the various electronic devices 2, thus solving possible anomalous contact resistance problems due to the power flowing between the probes and the various grids 4.

Moreover, the dummy probes help to reduce the effect of the resistance of the conductive grids 4.

The ground pad of the various electronic devices 2 can also be in common, and can be provided by means of the probes or by means of the so called chuck of the prober.

As already seen, besides the supplying, the conductive grids 4 can also supply some signals to the various devices on the wafer.

The invention solves the technical problem and attains several advantages. For example, one embodiment of the present invention, makes the process of EMWS testing through electromagnetic (in part or completely) communication between tester and wafer possible, strong and reliable, and can be used also for the EWS electric testing or for the wafer level burn-in WLBI.

In consequence, thanks to the invention, it is possible to enormously increase the testing parallelism, with subsequent reduction of the costs and/or of the test times, until reaching a parallel testing even of all the electronic devices 2 of a same wafer 1.

Moreover, possible bonding problems during the assembly step are reduced, which can be caused by the damaging or possible abrasion of the pads 6 due to the contact with the probes necessary for the electric testing.

Now, with particular reference to the example of figures 12 to 19 some other embodiments of the circuit architecture according to the present invention are described.

In these other examples also some details and cooperating parts having the same structure and operation as the previous embodiments
will be described and for them the same reference numbers will be used.

To supply a plurality of devices 2 with at least one power supply and possibly at least one signal, alternative solutions can be used with respect to those of the previous examples.

In fact, inside the scribe lines 7 a grid can be provided comprising common connections, which can be conductive lines 23, orthogonal to each other, which connect more devices 2 to each other, as shown in figure 12.

At the crossing point between the orthogonal lines 23 an insulation oxide 20, as shown in figure 12, or an insulating material maybe provided, so as to prevent a short circuit.

The pads 6 and 8 of two adjacent devices 2 will be connected to each other externally by using Bridging connections 14, which, in turn, are electrically connected to the conductive lines 23, as shown in figure 13.

Inside the generic device 2 the pads 6 and 8 are connected to each other by means of Crossing connections 13.

Alternatively, at least one or even all the conductive lines 23 can be flooded or buried in an insulating layer 21 in the scribe line 7, as shown in figures 15 and 16.

In particular, the conductive lines 23 are insulated from each other as shown in figure 16.

It may be necessary to realise at least one electric connection 22 of the vias type between the generic buried conductive line 23 and the Bridging connection 14, thus creating a Bridging connection with vias 24, so as to create the conductive grids shown in figure 14.

Alternatively, if there is a non flooded conductive line 23 in the scribe line, the generic pad 6 or 8 can be connected by using some connections 9, so as to create the conductive grids as shown in figure 17.

Alternatively and different types of conductive lines 23 being present, flooded in an insulating layer 21 in the scribe line 7 or not, Bridging connections 14 and Bridging connections with vias 24 can be used simultaneously, so as to create conductive grids as shown in
In particular, as shown in figure 19, the generic Bridging connection 14 crosses the scribe line 7 in correspondence to the passivation 15 and is insulated from the conductive line 23 which is flooded in the insulator 21 of the scribe line 7.

The metallic connections and the power supply grids may be then eliminated in any case after the testing further to the wafer cut, to encapsulate the various devices in a suitable package.

Alternatively, it is also possible to simultaneously use Bridging connections 14 and Bridging connections with vias 24 ending in correspondence with the scribe lines 7, so as to create the conductive grids as shown in figure 20.

In particular, as shown in figure 19, the Bridging connection with vias 24 starts in correspondence with the scribe line 7 and reaches the pad 6 passing the passivation 15 and is insulated from the further conductive line 23 which is flooded in the insulator 21 of the scribe line 7.

It is also to be considered that possible protection circuits, for example for the short circuits, are comprised within the generic device 2, or possibly can be also outside the same by incorporating them in at least one grid 4, realising for example at least one fuse link connected to the grid 4 and/or incorporated therein.

In this sense, the generic conductive line can be designed so that the same incorporates at least one fuse link in at least one section of this line, so that if a certain current value is overcome, the overheating of the conductive line will lead to a local fusion of said line interrupting the line itself.

The present invention thus also relates to a method comprising the steps of:

- forming the scribe lines 7 on the semiconductor wafer 1;
- forming the plurality of electronic devices 2 integrated on the semiconductor wafer 1 separated from each other by the scribe lines 7;
- forming the plurality of interconnection pads 6 on each electronic device 2 respectively;
- forming the conductive grid 4 on the semiconductor wafer 1.
In particular, the step of forming the conductive grid 4 further includes the steps of:

- forming the external portion 14 of the conductive grid 4 along the scribe lines 7;
- forming the internal portion 13 of the conductive grid 4 within the electronic devices 2; and
- connecting an interconnection pad 6 of each electronic device 2 to an interconnection pad 6 of a respective adjacent electronic device 2 and to the conductive grid 4 to form power supply lines common to the electronic devices 2.

Advantageously according to one embodiment of the invention, the step of forming the internal portion 13 comprises electrically connecting two interconnection pads 6 of a same electronic device 2.

Moreover, the method further comprises a step of supplying a voltage to all of the electronic devices 2 simultaneously through the conductive grid 4.

In particular, the method may comprise a step of simultaneously testing of the electronic devices 2.

The invention makes it possible, strong and industrially applicable the EWS testing process through electromagnetic (in part or completely) communication between tester and wafer.

In consequence, the invention allows to enormously increase the testing parallelism, with subsequent reduction of the costs, testing times, etc. so as to attain a testing in parallel of all the devices on the wafer.

Moreover, the bonding problems at the assembly caused by the damaging of the pads, currently caused by the probes for the electric testing, are reduced.

These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.
CLAIMS

1. Circuit architecture for the parallel supplying of power during an electric or electromagnetic testing of a plurality of electronic devices (2) each integrated on a same semiconductor wafer (1) wherein said electronic devices (2) are neatly provided on said semiconductor wafer (1) through integration techniques and have edges (5) bounded by separation scribe lines (7) characterised in that it comprises:
   - at least one conductive grid (4), interconnecting at least one group of said electronic devices (2) and having a portion being external (14) to the devices of said group and a portion being internal (13) to the devices of said group;
   - the external portion (14) of said conductive grid (4) being extended also along said separation scribe lines (7);
   - the internal portion (13) being extended within at least a part of the devices of said group;
   - interconnection pads (6) between said external portion (14) and said internal portion (13) of said conductive grid (4) being provided on at least a part of the devices of said group, said interconnection pads (6) forming, along with said internal and external portions, power supply lines which are common to different electronic devices (2) of said group.

2. Circuit architecture according to claim 1, characterised in that each electronic device (2) of said at least one group comprises at least a power supply pad (8) at the edge (5) of the electronic device (2) for the connection with the external portion (14) of said conductive grid (4).

3. Circuit architecture according to claim 2, characterised in that a plurality of said power supply pads (8) is provided, at least one at each edge (5) of the electronic devices (2) of said at least one group.

4. Circuit architecture according to claim 1, characterised in that said external portion (14) is an electronic bridging connection between at least one couple of power supply pads (8) of adjacent electronic devices (2).

5. Circuit architecture according to claim 1, characterised in that said internal portion (13) is an electric connection between two interconnection and power supply pads (6, 8) of a same electronic device (2).
device (2).

6. Circuit architecture according to claim 5, characterised in that said internal portion (13) is formed by a Crossing technique.

7. Circuit architecture according to claim 4, characterised in that said external portion (14) is formed by a Bridging technique.

8. Circuit architecture according to claim 1, characterised in that at least one part of said external portion (14) is realised in the scribe lines (7) region separating an electronic device (2) to another.

9. Circuit architecture according to claim 7, further comprising an insulating layer (15 and/or 16) positioned on one of said scribe lines (7), characterised in that said external portion (14) comprised at least one metal layer deposited on said at least one insulating layer (15 and/or 16) which extends between two adjacent interconnection pads (6) of two adjacent electronic devices (2).

10. Circuit architecture according to claim 8, characterised in that said part of said external portion (14) in the scribe lines (7) region comprises at least one metal layer deposited on a layer of filling insulating material (17) extending within said scribe lines (7), at least partially filling said scribe lines (7).

11. Circuit architecture according to claim 1, characterised in that said interconnection pads (6) comprise power supply dummy pads (8) and signal dummy pads (8).

12. Circuit architecture according to claim 1, characterised in that said external portion (14) and said internal portion (13) of said conductive grid (4) are orthogonal to each other.

13. Circuit architecture according to claim 1, characterised in that at least one of said external portion (14) and said internal portion (13) of said conductive grid (4) is realised by a conductive line (23) which is buried in at least one of said electronic devices (2) or of said semiconductor wafer (1).

14. Circuit architecture according to claim 12, characterised in that said external portion (14) and said internal portion (13) of said conductive grid (4) are insulated from each other at crossover points.

15. Circuit architecture according to claim 14, characterised in that at least one vias connection (24) is provided to contact said buried
conductive line (23).

16. Circuit architecture according to claim 1, characterised in that it further comprises at least one fuse link connected to at least one conductive grid (4).

17. Circuit architecture according to claim 1, characterised in that it further comprises at least one fuse link included into said at least one conductive grid (4).

18. A method comprising the steps of:
   forming scribe lines (7) on a semiconductor wafer (1);
   forming a plurality of electronic devices (2) integrated on said semiconductor wafer (1) separated from each other by said scribe lines (7);
   forming a respective plurality of interconnection pads (6) on each electronic device (2) respectively;
   forming a conductive grid (4) on said semiconductor wafer (1), said step of forming said conductive grid (4) including the steps of:
   forming an external portion (14) of said conductive grid (4) along said scribe lines (7);
   forming an internal portion (13) of said conductive grid (4) within said electronic devices (2); and
   connecting an interconnection pad (6) of each electronic device (2) to an interconnection pad (6) of a respective adjacent electronic device (2) and to said conductive grid (4) to form power supply lines common to said electronic devices (2).

19. The method of claim 18 wherein said step of forming said internal portion (13) comprises electrically connecting two interconnection pads (6) of a same electronic device (2).

20. The method of claim 18 comprising a step of supplying a voltage to all of said electronic devices (2) simultaneously through said conductive grid (4).

21. The method of claim 20 comprising a step of simultaneously testing of said electronic devices (2).
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

**INV.** H01L23/58  
**ADD.** G01R31/28

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical search terms used)

**EPO-Internal**

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
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<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No</th>
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<tr>
<td>X</td>
<td>US 6 744 067 B1 (FARNWORTH ET AL.) 1 June 2004 (2004-06-01) column 5, line 30 - column 6, line 19; figures 3,4</td>
<td>1,4,7,8,13,18</td>
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<tr>
<td>Y</td>
<td>EP 0 413 542 A (TEXAS INSTRUMENTS) 20 February 1991 (1991-02-20) column 4, lines 6-22</td>
<td>16,17</td>
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<td>A</td>
<td>US 2007/275539 A1 (RASHID ET AL.) 29 November 2007 (2007-11-29) paragraphs [0017], [0019], [0020]; figures 2,3</td>
<td>1-4,8,9,18</td>
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* Special categories of cited documents

W: document defining the general state of the art which is not considered to be of particular relevance  
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L: document which may throw doubts on prior art or on the priority date claimed  
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Y: document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art  
A: member of the same patent family

**Date of the actual completion of the international search**

30 November 2009

**Date of mailing of the international search report**

08/12/2009

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## INTERNATIONAL SEARCH REPORT

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<tr>
<td>US 2007275539 A1</td>
<td>29-11-2007</td>
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