Various semiconductor die conductor structures and methods of fabricating the same are provided. In one aspect, a method of manufacturing is provided that includes forming a conductor structure (230) on a conductor pad (200) of a semiconductor die (170). The conductor layer has a surface. A polymeric layer (240) is formed on the surface of the conductor layer while a portion of the surface is left exposed. A solder structure (280) is formed on the exposed portion of the surface and a portion of the polymeric layer.

FIG. 12
Declaration under Rule 4.17:
— as to applicant’s entitlement to apply for and be granted a patent (Rule 4.17(H))

Published:
— with international search report
"before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments"
BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates generally to semiconductor processing, and more particularly to semiconductor die conductor structures and to methods of making the same.

2. Description of the Related Art

[0002] Conventional integrated circuits are frequently implemented on a semiconductor substrate or die that consists of a small rectangular piece of semiconductor material, typically silicon, fashioned with two opposing principal sides. The active circuitry for the die is concentrated near one of the two principal sides. The side housing the active circuitry is usually termed the "active circuitry side," while the side opposite the active circuitry side is often referred to as the "bulk silicon side." Depending on the thermal output of the die, it may be desirable to mount a heat transfer device, such as a heat sink, on the bulk silicon side of the die. This mounting may be directly on the bulk silicon side or on a lid that is positioned over the die.

[0003] A conventional die is usually mounted on some form of substrate, such as a package substrate or a printed circuit board. Electrical conductivity between the die and the underlying substrate or board is established through a variety of conventional mechanisms. In a so-called flip-chip configuration, the active circuitry side of the die is provided with a plurality of conductor balls or bumps that are designed to establish a metallurgical bond with a corresponding plurality of conductor pads positioned on the substrate or circuit board. The die is flipped over and seated on the underlying substrate with the active circuitry side facing downwards. A subsequent thermal process is performed to establish the requisite metallurgical bond between the bumps and the pads. One of the principal advantages of a flip-chip mounting strategy is the relatively short electrical pathways between the integrated circuit and the substrate. These relatively low inductance pathways yield a high speed performance for the electronic device.
The manner in which the solder balls are electrically connected to the bond pads of the semiconductor die may have a significant impact on the reliability of semiconductor die and the host electronic device to which it is mounted. In one conventional technique, a dielectric passivation layer is fabricated on the active circuitry side of the semiconductor die and lithographically patterned with a plurality of openings corresponding to the locations of the bond pads. Next, a polyimide layer is fabricated over the passivation layer and lithographically patterned with a plurality of openings that are generally concentrically positioned relative to the openings in the passivation layer. A so-called under bump metallization layer is next deposited over the polyimide layer so that metal extends down to and bonds with the underlying bond pads. Thus, the polyimide layer is positioned between the under bump metal layer and the passivation layer. The significance of this arrangement will be explained in further detail below. After the under bump metallization layer is formed, a film or stencil is patterned on the under bump metal layer with a plurality of openings that are positioned over the general locations of the bond pads and a solder material is deposited by a plating or stencil paste process. The stencil is removed and a thermal process is performed to reflow the solder structures. The solder structures solidify into ball-like structures.

Lead-based solders have been widely used in semiconductor device fabrication for decades. More recently, however, chip manufacturers have begun turning to lead-free solders. Lead-free solder materials tend to have relatively lower ductility than lead-based solders. This increased stiffness can lead to significant stresses in the solder balls, particularly where operating temperatures are high or where there is a significant mismatch between the coefficients of thermal expansion between the semiconductor die and the substrate upon which it is mounted. The difficulty with the conventional technique stems from the relative positions of the polyimide layer, the under bump metallization layer and the solder balls. Because the polyimide layer is essentially separated from the solder balls by the under bump metallization layer, the stress reducing abilities of the polyimide layer are not available to the solder balls. Accordingly, high mechanical stresses may be inflicted on the solder balls, particularly at the edges of the solder balls near the interfaces with the under bump metallization layer. The stresses can lead to cracks
in the solders balls. If the stresses are acute enough, mechanical failure of the solder balls can occur and produce electrical device failure.

[0006] The present invention is directed to overcoming or reducing the effects of one or more of the foregoing disadvantages.
SUMMARY OF THE INVENTION

[0007] In accordance with one aspect of the present invention, a method of manufacturing is provided that includes forming a conductor structure on a conductor pad of a semiconductor die. The conductor layer has a surface. A polymeric layer is formed on the surface of the conductor layer while a portion of the surface is left exposed. A solder structure is formed on the exposed portion of the surface and a portion of the polymeric layer.

[0008] In accordance with another aspect of the present invention, a method of manufacturing is provided that includes forming a conductor structure on a conductor pad of a semiconductor die. The conductor layer has a surface. A polymeric layer is formed on the surface of the conductor layer while a portion of the surface is left exposed. A solder structure is formed on the exposed portion of the surface and a portion of the polymeric layer. The semiconductor die is coupled to a first substrate.

[0009] In accordance with another aspect of the present invention, an apparatus is provided that includes a semiconductor die that has a conductor pad with a surface. A conductor structure is electrically coupled to the conductor pad. A polymeric layer is positioned on the surface of the conductor structure and has an opening to a portion of the surface of the conductor structure. A solder structure is coupled to the portion of the surface of the conductor structure.

[0010] In accordance with another aspect of the present invention, an apparatus is provided that includes a semiconductor die coupled to a first substrate. The semiconductor die includes a conductor pad that has a surface. A conductor structure is electrically coupled to the conductor pad. A polymeric layer is positioned on the surface of the conductor structure and has an opening to a portion of the surface of the conductor structure. A solder structure is coupled to the portion of the surface of the conductor structure.
BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

[0012] FIG. 1 is a sectional view of a conventional semiconductor die with a bond pad and passivation layer;

[0013] FIG. 2 is a sectional view of a conventional semiconductor die following polyimide and metal layer deposition;

[0014] FIG. 3 is a sectional view of a conventional semiconductor die following mask formation;

[0015] FIG. 4 is a sectional view of a conventional semiconductor die following solder deposition;

[0016] FIG. 5 is a sectional view of a conventional semiconductor die following solder reflow to establish a bump;

[0017] FIG. 6 is a sectional view of a conventional semiconductor die following flip-chip mounting;

[0018] FIG. 7 is a portion of the sectional view of FIG. 6 depicted at greater magnification;

[0019] FIG. 8 is a sectional view of an exemplary embodiment of a semiconductor die following passivation layer formation;

[0020] FIG. 9 is a sectional view of the exemplary embodiment of the semiconductor die depicting metal layer and insulating layer formation;

[0021] FIG. 10 is a sectional view of the exemplary embodiment of the semiconductor die depicting formation of a mask thereon;

[0022] FIG. 11 is a sectional view of the exemplary embodiment of the semiconductor die depicting formation of a conductor structure thereon;

[0023] FIG. 12 is a sectional view of the exemplary embodiment of the semiconductor die depicting a reflow of the conductor structure;

[0024] FIG. 13 is a sectional view of the exemplary embodiment of the semiconductor die depicting an exemplary mounting to a substrate;
FIG. 14 is a sectional view of an alternate exemplary embodiment of a semiconductor die depicting passivation, metal layer and mask formation thereon;

FIG. 15 is a sectional view of the alternate exemplary embodiment of the semiconductor die depicting removal of the mask and portions of the metal layer;

FIG. 16 is a sectional view of the alternate exemplary embodiment of the semiconductor die depicting formation of an insulating layer thereon;

FIG. 17 is a sectional view of the alternate exemplary embodiment of the semiconductor die depicting formation of a conductor structure thereon;

FIG. 18 is a sectional view of the alternate exemplary embodiment of the semiconductor die depicting a reflow of the conductor structure;

FIG. 19 is a pictorial view of another alternate exemplary embodiment of a semiconductor die provided with plural bump structures and a common metal layer; and

FIG. 20 is an exploded pictorial view of an exemplary semiconductor die depicting exemplary mounting configurations.
DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0032] In the drawings described below, reference numerals are generally repeated where identical elements appear in more than one figure. Before discussing the exemplary embodiments disclosed herein, it will be instructive to review briefly the structure and manufacture of a conventional solder bump metallization design. Turning now to the drawings, and in particular to FIGS. 1-5, therein is shown an exemplary conventional fabrication process for forming a conductive solder bump on the lower surface of a semiconductor chip 10. For simplicity of illustration, FIGS. 1-5 focus on a relatively small portion of a semiconductor device 10. Turning initially to FIG. 1, the semiconductor device 10 includes two opposing sides 20 and 30. The side 20 is often referred to as a backside and the opposite side 30 is sometimes referred to as a front side. Active chip circuitry (not visible) is typically positioned in one or more layers proximate the front side 30. A bond pad 40 is provided proximate the side 30 and designed to provide an electrical pathway from the circuitry of the device 10 through a later-formed solder bump to establish electrical conductivity with circuitry external to the device 10. There may be scores of such bond pads 40 depending on the complexity of the device 10. A passivation layer 50 of silicon nitride is formed on the side 30 and patterned so that an opening 60 extends to the bond pad 40. The passivation layer 50 is designed to prevent the diffusion of metallic materials down into the semiconductor device 10.

[0033] Referring now to FIG. 2, a polyimide layer 70 is formed on the stack consisting of the passivation layer 50, the bond pad 40 and the semiconductor device 10. The polyimide layer 70 is formed with an opening 80 that is concentrically positioned with the opening 60 in the passivation layer 50. Polyimide is chosen for its ability to provide both advantageous structural flexibility and electrical insulation. Following the application of the polyimide layer 70, a metallization layer 90 is formed on the polyimide layer 70 and down through the opening 80 therein to establish ohmic contact with the bond pad 40. The metallization layer 90 is sometimes referred to as an under bump metallization layer or UBM layer. The UBM layer 90 is sometimes deposited as a sequential stack of different metallic materials, such as titanium copper and nickel.
[0034] As shown in FIG. 3, an insulating film 100 is formed on the stack consisting of the metallization layer 90, the polyimide layer 70, the passivation layer 50, the bond pad 40 and the device 10. An opening 110 is patterned in the film 100 that exposes a portion of the metallization layer 90. The film 100 is designed to serve as a mask, or a stencil if a stencil process is used, to enable the subsequent deposition of a conductor material in the opening 110 that will ultimately be fashioned into a solder bump. The opening 110 is typically formed by a lithographic patterning process.

[0035] Referring now to FIG. 4, the semiconductor device 10 undergoes a plating process so that a conductor material 120 is deposited in the opening 110 of the film 100 and on the exposed portion of the metallization layer 90. The conductor material is typically a solder that establishes ohmic contact with the metallization layer 90. A conventional solder consists of a tin-lead mixture. A more recent innovation involves the use of a lead-free solder, such as a tin-copper solder. The polyimide layer 70 and the passivation layer inhibit diffusion of material from the conductor 120 and the metallization layer 90 into the device 10. The bond pad 40 is unaffected by the plating.

[0036] The film 100 depicted in FIG. 4 is removed and a thermal reflow process is performed on the semiconductor device 10 as depicted in FIG. 5 to reflow the conductor material 120 into a rounded bump. Following the solder reflow process, portions of the metallization layer 90 lateral to the solder bump 120 are etched away by wet etching. At this point, an ohmic pathway exists between the solder bump 120, the metallization layer 90 and the underlying bump pad 40. The passivation layer 50 and the polyimide layer 70 remain in place.

[0037] As noted in the Background section hereof, the placement of the polyimide layer 70 beneath the metallization layer 90 has an important ramification that is evident when the semiconductor device 10 is flip-chip mounted on another device. In this regard, FIG. 6 depicts a sectional view of the semiconductor device 10 flip-chip mounted on another substrate 130 such that the side 30 faces downward. An underfill material 140 is disposed between the polyimide layer 70 and the substrate 130 to lessen the stresses due to differences in the coefficients of thermal expansion of the electrical device 130 and the semiconductor device 10. The solder
bump of the semiconductor device 10 is positioned on a corresponding bond pad 150 of the
device 130. In this way, an electrical pathway is established between the bond pad 40 of the
device 10 and the bond pad 150 of the device 130 via the metallization layer 90 and the solder
bump 120. A small portion of the solder bump 120, the underfill layer 140 and the metallization
layer 90 is circumscribed by a small oval 160. The portion circumscribed by the oval 160 is
shown at greater magnification in FIG. 7.

[0038] FIG. 7 illustrates a drawback to the placement of the polyimide layer 70 shown in FIG.
6 between the metallization layer 90 and the solder bump 120. A crack 160 is shown in the
solder bump 120 that extends from the border 165 with the underfill material 140 toward the
central portion of the solder bump 120. The crack 160 is the result of thermal stresses that are
not adequately compensated for by virtue of the relative stiffness of the lead-free solder bump
120 and the relative distance of the polyimide layer 70 from the area where the crack 160 forms.
The crack 160 may propagate across the entire width of the solder bump 120 and produce an
open circuit.

[0039] An exemplary novel fabrication process that overcomes the pitfalls of the above-
described conventional process may be understood by referring now to FIGS. 8-12, which depict
successive sectional views of an integrated circuit or semiconductor device 170 undergoing
various process steps leading to the formation of a solder bump. It should be understood that
FIGS. 8-12 depict just a small portion of the device 170. The semiconductor device 170 may be
any of a myriad of different types of circuit devices used in electronics, such as, for example,
microprocessors, graphics processors, application specific integrated circuits, memory devices or
the like, and may be single or multi-core.

[0040] Structurally speaking, the device 170 has opposing sides 180 and 190. Device circuitry,
represented schematically by the dashed box 195, may be located proximate the side 190. To
connect the circuitry 195 electrically to external devices, the semiconductor device 170 may be
provided with multiple conductor or bond pads, one of which is shown and labeled 200, that are
positioned proximate the side 190. Depending on the complexity and size of the semiconductor
device 170, there may be scores of the pads 200. The bond pad 200 may be composed of a
variety of conductor materials, such as aluminum, copper, silver, gold, titanium, refractory metals, refractory metal compounds, alloys of these or the like. The bond pad 200 may be formed by plating, physical vapor deposition or other material deposition techniques.

[0041] A passivation layer 210 is formed on the side 190 with an opening 220. The passivation layer 210 is designed to inhibit the diffusion of metallic or other materials down into the semiconductor device 170. The layer 210 may be composed of a variety of insulating materials, such as, for example, silicon nitride, silicon dioxide, various silicate glasses or the like. The opening 220 may be formed by well-known lithographic patterning and etching techniques.

[0042] For simplicity of illustration, the remaining figures do not include the circuitry 195. Attention is now turned to FIG. 9. A conductor or metal layer 230 is formed on the passivation layer 210 and in the opening 220 thereof so that ohmic contact is established with the bond pad 200. The metallization layer 230 is designed to provide a conducting interface between the bond pad 200 and a subsequently formed solder structure (not shown). The metallization layer 230 may be composed of a variety of conductor materials, such as aluminum, copper, silver, gold, titanium, refractory metals, refractory metal compounds, alloys of these or the like. In lieu of a unitary structure, the layer 230 may consist of a laminate of plural metal layers, such as a titanium layer followed by a nickel-vanadium layer followed by a copper layer. In another embodiment, a titanium layer may be covered with a copper layer followed by a top coating of nickel. However, the skilled artisan will appreciate that a great variety of conducting materials may be used for the metallization layer 230. Various well-known techniques for applying metallic materials may be used, such as physical vapor deposition, chemical vapor deposition, plating or the like. It should be understood that additional conductor structures could be interposed between the metal layer 230 and the conductor pad 200.

[0043] An insulating film 240 is deposited on the stack consisting of the metallization layer 230, the passivation layer 210, the pad 200 and the semiconductor device 170. The insulating film 240 is positioned on a surface 255 of the metal layer 230. The layer 240 is intended to provide passivation and cushion against differences in thermal expansion of the semiconductor
device 170, the metallization layer 230 and the subsequently formed solder bump (not shown).

Exemplary materials for the insulating layer 240 include, for example, polymeric materials such as polyimide and benzocyclobutene or the like, or other insulating materials such as silicon nitride or the like. Spin coating, chemical vapor deposition or other deposition processes may be used. The insulating layer 240 is patterned lithographically with an opening 250 that exposes a portion of the metallization layer 230. Note that the insulating layer 240 is positioned above the metallization layer 230 as opposed to below the metallization layer 90 in the conventional technique depicted in FIGS. 1-5. This placement provides a structural advantage as described in more detail below.

Attention is now turned to FIG. 10. A mask film 260 is deposited on the stack consisting of the insulating layer 240, the metallization layer 230, the passivation layer 210, the pad 200 and the semiconductor device 170. The mask film 260 is patterned lithographically with an opening 270 that is concentric with the opening 250 in the insulating layer 240. Together, the openings 250 and 270 leave a portion 275 of the surface 255 of the metal layer 230 exposed. In a subsequent process, a conductor material is positioned in the combined openings 250 and 270 to establish ohmic contact with the metallization layer 230 and the underlying bond pad 200 of the device 170. The film 260 may be made from, for example, a rubberized epoxy resin with phenol resin, fused silica and synthetic rubber. Optionally, other materials suitable for a metal application mask may be used.

As shown in FIG. 11, the semiconductor device 170 is subjected to a plating process to deposit a conductor material 280 in the openings 250 and 270 and on the exposed portion 275 of the surface 255 of the metallization layer 230. The film 260 serves as a mask against this deposition process. The conductor 280 may be a lead-based solder or lead free as desired. Exemplary materials include, for example, tin-copper, tin-silver, or other solder materials. The conductor material 280 borders the insulating layer 240. At this point, a conductive pathway between the bond pad 200, the metallization layer 230 and the conductor material 280 exists. The passivation layer 210 is unaffected. Of course, another conductor(s) (not shown) may be
positioned between the conductor 280 and the bond pad 200 and still provide the desired ohmic pathway.

[0046] As shown in FIG. 12, the film 260 depicted in FIG. 11 is removed and a reflow process is performed to reflow the conductor 280 into a ball or bump-like structure. In an exemplary embodiment, the semiconductor device 170 may be heated to about 170 to 190°C for about 10 to 120 seconds. The appropriate parameters for the reflow will depend on the composition of conductor material 280. Unwanted portions of the metallization layer 230 are removed by a chemical etch process. Thus, portions of the passivation layer 210 lateral to the conductor 280 are exposed. A conductive pathway exists between the conductor 280 and the bump bond pad 200 by way of the metallization layer 230. Note that the conductor 280 is positioned on a portion 285 of the insulating layer 240. The portion 285 provides a stress reducing interface with a peripheral corner 287 of the conductor 280.

[0047] The advantages of the new positioning of the insulating layer 240 are evident when the device 170 is mounted to another substrate. Attention is now turned to FIG. 13, which depicts the semiconductor device 170 mounted on another electrical device 290. The electrical device 290 may be a printed circuit board, or other electrical device as desire. FIG. 13 depicts a flip-chip mounting arrangement in which the device 170 is flipped over and mounted on the electrical device 290 so that the solder structure 280 is seated on a bond pad 300 of the electrical device 290. It should be understood that the device 290 may include scores of such pads 300 to receive corresponding bumps 280 of the device 170. If desired, the pads 300 may be fitted with small solder bumps (not shown) designed to meld with solder structure(s) 280 during a subsequent reflow. An underfill material 310 is dispersed between the device 170 and the electrical device 290 to reduce the effects of differences in the coefficients of thermal expansion of the device 170 and the device 290. The underfill 310 may be, for example, an epoxy resin mixed with silica fillers and phenol resins. Because the insulating layer 240 is positioned between the metallization layer 230 and the solder structure 280, an additional compliant cushioning effect is provided for the corner 320 of the solder bump 280 against the types of thermal stresses and
cracking associated with the conventional structure depicted in FIGS. 6 and 7. Note that the corner 320 extends around the entire periphery of the solder structure 280.

[0048] In the foregoing illustrative embodiment, a plating process may be used to form the solder structures 280. In an alternate exemplary process depicted in FIGS. 14-18, a stencil process may be used to establish a solder structure. Turning initially to FIG. 14, the semiconductor device 170 may be processed as described elsewhere herein to provide the bond pad 200, the passivation layer 210 and the metallization layer 230. At this stage, an etch mask 330 of resist or other mask material is formed on the metallization layer 230, and an etch is performed on the metallization layer 230 to trim portions thereof lateral to the bond pad 200 and expose portions of the passivation layer 210 as shown in FIG. 15. The etch mask 330 may be removed by ashing, solvent stripping or the like. When viewed from above, the metallization layer 230 may be circular or another shape as desired. The bond pad 200 is unaffected by the etch or mask strip.

[0049] As shown in FIG. 16, the insulating layer 240 is formed on the stack consisting of the metallization layer 230, the passivation layer 210, the bond pad 200 and the semiconductor device 170 as generally described elsewhere herein. The insulating layer 240 has the aforementioned opening 250 leading to the metallization layer 230 and leaving the surface thereof 255 with an exposed portion 275.

[0050] Referring now to FIG. 17, a stencil 340 is formed on the stack consisting of the insulating layer 240, the metallization layer 230, the passivation layer 210, the bond pad 200 and the semiconductor device 170. The stencil 340 includes an opening 350 over the metallization layer 230 and portions of the insulating layer 240. The stencil 340 may be fabricated from, for example, a rubberized epoxy resin with phenol resin, fused silica and synthetic rubber. Optionally, other materials suitable for metal application stencils may be used. A conductor paste 360 is pressed into the opening 350 of the stencil 340. The conductor paste 360 is positioned on the exposed portion 275 of the surface 255 of the metal layer 230 and a portion 365 of the insulating layer 240. The paste 360 may be composed of the same materials used for the solder bump 280 described elsewhere herein. Of course, another conductor(s) (not shown)
may be positioned between the conductor 360 and the bond pad 200 and still provide the desired ohmic pathway.

[0051] To complete the process, the stencil 340 is removed and a thermal reflow process is performed to reshape the conductor paste 360 into a bump that metallurgically bonds to the pad 200 as shown in FIG. 18. In an exemplary embodiment, the semiconductor device 170 may be heated to about 170 to 190°C for about 10 to 120 seconds. The appropriate parameters for the reflow will depend on the composition of conductor paste 360. The passivation layer 210 is unaffected. The conductor 360 is positioned on a portion 365 of the insulating layer 240. As in the above-described embodiment, the insulating layer 240 provides enhanced structural protection for a peripheral corner 370 of the solder bump 360.

[0052] In addition to providing improved structural protection for the solder bumps 280, 360 etc., the positioning of the insulating layer 240 as disclosed herein enables the under bump metallization layer 230 to serve as an electrical routing structure. An exemplary embodiment may be understood by referring now to FIG. 19, which is a pictorial view of a portion of the semiconductor device 170 positioned with the insulating layer 240 and several bumps facing upwardly. One of the bumps is labeled 280 as in FIGS. 8-12. Two other bumps are separately labeled 380 and 390. A group of six bumps are collectively labeled 400. The bumps 280, 380 and 390 may be formed and provided with discrete under bump conductor structures or metal layers 410, 420 and 430 that are structurally isolated using the techniques disclosed herein. The metal layers 410, 420 and 430 are covered by the insulating layer 240 and thus shown in phantom. However, the group of bumps 400 may be formed using the techniques disclosed herein, but with a common under bump conductor structure or metal layer 440 that is covered by the insulating layer 240 and thus also shown in phantom. The insulating layer 240 is thus formed with plural openings to expose plural portions of the metal layer 440 prior to formation of the bumps 400. In this way, the metal layer 440 can serve as a routing structure for the group of bumps 400. This may be advantageous where several bumps are dedicated temporarily or permanently to one type of input/output, such as power or ground. Because the insulating layer 240 is positioned between the group 400 of bumps and the metallization layer 440, selected...
bumps can be tied together without risk that solder will seep laterally and make unwanted shorts during reflow. Of course, the number and groupings of bumps and shaping of the common under bump metallization layer(s) 440 are subject to great variation.

[0053] The skilled artisan will appreciate that the exemplary processes disclosed herein may be performed concurrently on multiple dice that are arranged in a wafer. Thereafter, singulation may be performed. Optionally, an individual die may be processed after singulation.

[0054] The semiconductor device 170 may be mounted in a variety of ways. FIG. 20 depicts an exploded pictorial view of a few exemplary mounting possibilities. The semiconductor device 170 is depicted with the solder bumps 280 facing upwards. The device 170 may be flipped over as indicated by the arrow 450 and flip-chip mounted on a substrate 460. The substrate 460 may be a package substrate, a printed circuit board or other type of substrate. If configured as a package substrate, the substrate 460 may be a pin grid array, a ball grid array, a land grid array, a surface mount or other type configuration. The substrate 460 may be mounted to another substrate 470. The substrate 470 may be a printed circuit board or other type of substrate. For example, the substrate 470 may be a motherboard for a computer system. The semiconductor device 170 may be included in a larger system, such as a computing device represented by the dashed box 480. The computing device 480 may be include, for example, a digital television, a handheld mobile device, a personal computer, a server, a memory device, an add-in board such as a graphics card, or any other computing device employing semiconductors.

[0055] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.
CLAIMS

What is claimed is:

1. A method of manufacturing, comprising:
   forming a conductor structure on a conductor pad of a semiconductor die, the conductor
   structure having a surface;
   forming a polymeric layer on the surface of the conductor structure while leaving a
   portion of the surface exposed; and
   forming a solder structure on the exposed portion of the surface and a portion of the
   polymeric layer.

2. The method of claim 1, wherein the forming the polymeric layer comprises forming a
   polyimide layer.

3. The method of claim 1, wherein the forming the solder structure comprises plating a
   solder material.

4. The method of claim 3, wherein the plating the solder material comprises plating a lead-
   free solder.

5. The method of claim 1, wherein the forming the solder structure comprises stencil
   forming a solder material.

6. The method of claim 1, wherein the forming the solder structure comprises a thermal
   reflow.

7. The method of claim 1, wherein the forming the conductor structure comprises depositing
   metal and etching the metal to remove unwanted portions thereof.
8. The method of claim 1, wherein the forming of the polymeric layer comprises leaving portions of the surface exposed and wherein the forming a solder structure on the exposed portion and a portion of the polymeric layer comprises forming solder structures on the exposed portions of the surface, portions of the solder structures being positioned on the polymeric layer.

9. A method of manufacturing, comprising:
   forming a conductor structure on a conductor pad of a semiconductor die, the conductor layer having a surface;
   forming a polymeric layer on the surface of the conductor layer while leaving a portion of the surface exposed;
   forming a solder structure on the exposed portion of the surface and a portion of the polymeric layer; and
   coupling the semiconductor die to a first substrate.

10. The method of claim 9, wherein the coupling the semiconductor die comprises flip-chip mounting.

11. The method of claim 9, comprising coupling the first substrate to a second substrate.

12. The method of claim 9, wherein the forming the polymeric layer comprises forming a polyimide layer.

13. The method of claim 9, wherein the forming the solder structure comprises plating a solder material.

14. The method of claim 13, wherein the plating the solder material comprises plating a lead-free solder.
15. The method of claim 9, wherein the forming the solder structure comprises stencil forming a solder material.

16. An apparatus, comprising:
   a semiconductor die including a conductor pad having a surface;
   a conductor structure electrically coupled to the conductor pad;
   a polymeric layer positioned on the surface of the conductor structure and having an opening to a portion of the surface of the conductor structure; and
   a solder structure coupled to the portion of the surface of the conductor structure.

17. The apparatus of claim 16, wherein the polymeric layer comprises a polyimide layer.

18. The apparatus of claim 16, wherein the solder structure comprises a lead-free solder.

19. The apparatus of claim 16, wherein the conductor structure comprises a laminate of plural metal layers.

20. The apparatus of claim 16, wherein the polymeric layer includes another opening to another portion of the surface of the conductor structure and another solder structure is coupled to the another portion of the surface of the conductor structure.

21. An apparatus, comprising:
   a semiconductor die coupled to a first substrate and including a conductor pad having a surface;
   a conductor structure electrically coupled to the conductor pad;
   a polymeric layer positioned on the surface of the conductor structure and having an opening to a portion of the surface of the conductor structure; and
a solder structure coupled to the portion of the surface of the conductor structure.

22. The apparatus of claim 21, wherein the first substrate comprises a package substrate.

23. The apparatus of claim 21, wherein the first substrate is coupled to second substrate.

24. The apparatus of claim 21, wherein the polymeric layer comprises a polyimide layer.

25. The apparatus of claim 21, wherein the solder structure comprises a lead-free solder.

26. The apparatus of claim 21, wherein the conductor structure comprises a laminate of plural metal layers.

27. The apparatus of claim 21, wherein the polymeric layer includes another opening to another portion of the surface of the conductor structure and another solder structure is coupled to the another portion of the surface of the conductor structure.
FIG. 6
(PRIOR ART)

FIG. 7
(PRIOR ART)
**INTERNATIONAL SEARCH REPORT**

**International application No.**
PCT/IB2008/002024

**A. CLASSIFICATION OF SUBJECT MATTER**

INV. H01L23/485 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC.

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

HOIL

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and where practical, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
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<tr>
<th>Category</th>
<th>Citation of document with indication, where appropriate of the relevant passages</th>
<th>Relevant to claim No</th>
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Further documents are listed in the continuation of Box C. See patent family annex.

- Special categories of cited documents
  - "A" document defining the general state of the art which is not considered to be of particular relevance
  - "E" earlier document but published on or after the international filing date
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  - "O1" document referring to an oral disclosure, use exhibition or other means
  - "P" document published prior to the international filing date but later than the priority date claimed

**Date of the actual completion of the international search**

2 December 2008

**Date of mailing of the international search report**

11/12/2008

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Form FCT/ISA/210 (second sheet) (April 2005)
**DOCUMENTS CONSIDERED TO BE RELEVANT**

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