The present invention provides an electronic assembly (400) and a method for its manufacture (800, 900, 1000, 1200, 1400, 1500, 1700). The assembly (400) uses no solder. Components (406), or component packages (402, 802, 804, 806) with I/O leads (412) are placed 800 onto a planar substrate (808). The assembly is encapsulated (900) with electrically insulating material 908 with vias (420, 1002) formed or drilled (1000) through the substrate (808) to the components' leads (412). Then the assembly is plated (1200) and the encapsulation and drilling process (1500) repeated to build up desired layers (422, 1502, 1702).
CROSS REFERENCE TO RELATED APPLICATIONS

The present application is based on and priority is claimed to provisional applications

entitled "ELECTRONIC ASSEMBLY WITHOUT SOLDER," U.S. Application No. 60/928,467, filed on May 8, 2007; "ELECTRONIC ASSEMBLY WITHOUT SOLDER AND METHODS FOR THEIR MANUFACTURE," U.S. Application No. 60/932,200, filed on May 29, 2007; "SOLDERLESS FLEXIBLE ELECTRONIC ASSEMBLIES AND METHODS FOR THEIR MANUFACTURE," U.S. Application No. 60/958,385, filed on July 5, 2007; "ELECTRONIC ASSEMBLIES WITHOUT SOLDER AND METHODS FOR THEIR MANUFACTURE," U.S. Application No. 60/959,148, filed on July 10, 2007; "MASS ASSEMBLY OF ENCAPSULATED ELECTRONIC COMPONENTS TO A PRINTED CIRCUIT BOARD BY MEANS OF AN ADHESIVE LAYER HAVING EMBEDDED CONDUCTIVE JOINING MATERIALS," U.S. Application No. 60/962,626, filed on July 31, 2007; "SYSTEM FOR THE MANUFACTURE OF ELECTRONIC ASSEMBLIES WITHOUT SOLDER," U.S. Application No. 60/963,822, filed on August 6, 2007; "ELECTRONIC ASSEMBLIES WITHOUT SOLDER AND METHODS FOR THEIR MANUFACTURE," U.S. Application No. 60/966,643, filed on August 28, 2007; "MONOLITHIC MOLDED SOLDERLESS FLEXIBLE ELECTRONIC ASSEMBLIES AND METHODS FOR THEIR MANUFACTURE," U.S. Application No. 61/038,564, filed on March 21, 2008; and "THE OCCAM PROCESS SOLDERLESS ASSEMBLY AND INTERCONNECTION OF ELECTRONIC PACKAGES," U.S. Application No. 61/039,059, filed on March 24, 2008, the benefits of the filing dates which are claimed under 35 U.S.C. § 119(e).
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FIELD OF THE INVENTION

The present invention relates generally to the field of electronic assembly and more specifically, but not exclusively, to the manufacture and assembly of electronic products without the use of solder.

BACKGROUND

The assembly of electronic products and more specifically the permanent assembly of electronic components to printed circuit boards has involved the use of some form of relatively low-temperature solder alloy (e.g., tin/lead or Sn63/Pb37) since the earliest days of the electronics industry. The reasons are manifold but the most important one has been the ease of mass joining of thousand of electronics interconnections between printed circuit and the leads of many electronic components.

Lead is a highly toxic substance, exposure to which can produce a wide range of well known adverse health effects. Of importance in this context, fumes produced from soldering operations are dangerous to workers. The process may generate a fume which is a combination of lead oxide (from lead based solder) and colophony (from the solder flux).
Each of these constituents has been shown to be potentially hazardous. In addition, if the amount of lead in electronics were reduced, it would also reduce the pressure to mine and smelt it. Mining lead can contaminate local ground water supplies. Smelting can lead to factory, worker, and environmental contamination.

Reducing the lead stream would also reduce the amount of lead in discarded electronic devices, lowering the level of lead in landfills and in other less secure locations. Because of the difficulty and cost of recycling used electronics, as well as lax enforcement of legislation regarding waste exports, large amounts of used electronics are sent to countries such as China, India, and Kenya, which have lower environmental standards and poorer working conditions.

Thus, there are marketing and legislative pressures to reduce tin/lead solders. In particular, the Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (commonly referred to as the Restriction of Hazardous Substances Directive or RoHS) was adopted in February 2003 by the European Union. The RoHS directive took effect on July 1, 2006, and is required to be enforced and become law in each member state. This directive restricts the use of six hazardous materials, including lead, in the manufacture of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC which sets collection, recycling and recovery targets for electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic electronic device waste.

RoHS does not eliminate the use of lead in all electronic devices. In certain devices requiring high reliability, such as medical devices, continued use of lead alloys is permitted.
Thus, lead in electronics continues to be a concern. The electronics industry has been searching for a practical substitute for tin/lead solders. The most common substitutes in present use are SAC varieties, which are alloys containing tin (Sn), silver (Ag), and copper (Cu).

SAC solders also have significant environmental consequences. For example, mining tin is disastrous both locally and globally. Large deposits of tin are found in the Amazon rain forest. In Brazil, this has led to the introduction of roads, clearing of forest, displacement of native people, soil degradation, and creation of dams, tailing ponds, and mounds, and smelting operations. Perhaps the most serious environmental impact of mining tin in Brazil is the silting up of rivers and creeks. This degradation modifies forever the profile of animal and plant life, destroys gene banks, alters the soil structure, introduces pests and diseases, and creates an irrecoverable ecological loss.

Worldwide ecological problems stemming from mismanagement of Brazil's environment are well known. These range from pressures on global warming from the destruction of rain forest to the long term damage to the pharmaceutical industry by the destruction of animal and plant life diversity. Mining in Brazil is simply one example of the tin industry's destructive effects. Large deposits and mining operations also exist in Indonesia, Malaysia, and China, developing countries where attitudes toward economic development overwhelm concerns for ecological protection.

SAC solders have additional problems. They require high temperatures, wasting energy, are brittle, and cause reliability problems. The melting temperature is such that components and circuit boards may be damaged. Correct quantities of individual alloy
constituent compounds are still under investigation and the long term stability is unknown. Moreover, SAC solder processes are prone to the formation of shorts (e.g., "tin whiskers") and opens if surfaces are not properly prepared. Whether tin/lead solder or a SAC variety is used, dense metal adds both to the weight and height of circuit assemblies.

Therefore there is a need for a substitute for the soldering process and its attendant environmental and practical drawbacks.

While solder alloys have been most common, other joining materials have been proposed and/or used such as so-called "polymer solders" which are a form of conductive adhesive. Moreover, there have been efforts to make connections separable by providing sockets for components. There have also been electrical and electronic connectors developed to link power and signal carrying conductors described with various resilient contact structures all of which require constant applied force or pressure.

At the same time, there has been a continual effort to put more electronics into ever smaller volumes. As a result, over the last few years there has been interest within the electronics industry in various methods for integrated circuit (IC) chip stacking within packages and the stacking of IC packages themselves, all with the intent of reducing assembly size in the Z or vertical axis. There has also been an ongoing effort to reduce the number of surface mounted components on a printed circuit board (PCB) by embedding certain components, mostly passive devices, inside the circuit board.

In the creation of IC packages, there has also been an effort to embed active devices by placing unpackaged IC devices directly inside a substrate and interconnecting them by drilling and plating directly to the chip contacts. While such solutions offer benefits in
specific applications, the input/output (I/O) terminals of the chip can be very small and very challenging to make such connections accurately. Moreover the device after manufacturing may not successfully pass burn in testing making the entire effort valueless after completion.

Another area of concern is in management of heat as densely packaged ICs may create a high energy density that can reduce the reliability of electronic products.

SUMMARY OF THE INVENTION

The present invention provides an electronic assembly and a method for its manufacture. Pre-tested and burned in components including electrical, electronic, electro-optical, electro-mechanical and user interface devices with external I/O contacts are placed onto a planar base. The assembly is encapsulated with a solder mask, dielectric, or electrically insulating material (collectively referred to as "insulating material" in this application including claims) with holes, known as vias, formed or drilled through to the components' leads, conductors, and terminals (collectively referred to as "leads" in this application including claims). Then the assembly is plated and the encapsulation and drilling process repeated to build up desired layers.

The assembly, built with a novel reverse-interconnection process (RIP), uses no solder, thus bypassing the use of lead, tin, and heat associated problems. The term "reverse" refers to the reverse order of assembly; components are placed first and then circuit layers manufactured rather than creating a PCB first and then mounting components. No conventional PCB is required (although one may be optionally integrated), shortening
manufacturing cycle time, reducing costs and complexity, and lessening PCB reliability problems.

RIP products are robust with respect to mechanical shock and thermal cycle fatigue failure. In comparison to conventional products placed on PCB boards, components incorporated into RIP products require no standoff from the surface and thus have a lower profile and can more densely spaced. Moreover, because no solderable finish is required and fewer materials and fewer process steps are required, RIP products are lower-cost. In addition, RIP products are amenable to in-place thermal enhancements (including improved heat dissipation materials and methods) that also may provide integral electromagnetic interference (EMI) shielding. Moreover the structure may be assembled with embedded electrical and optical components.

The present invention overcomes numerous disadvantages in the prior art by:

- Obviation of the need for circuit boards
- Obviation of the need for soldering
- Obviation of the problem of "tin whiskers"
- Obviation of the need for difficult cleaning between fine pitch component leads
- Obviation of the need for compliant leads or compliant solder connections
- Obviation of many of the problems associated with electronic waste at many different levels of manufacturing and end of life
- Obviation of the thermal concerns related to the use of high temperature lead-free solders on vulnerable components
Benefits of the present invention include:

- Low manufacturing waste, as structures are almost completely additive
- Lower material use in construction
- Environmentally friendly as potentially toxic metals are not needed
- Fewer processing steps
- Reduced testing requirements
- Low heat processing, thus resulting in energy savings
- Lower cost
- Lower profile assemblies
- Increased reliability
- Potentially higher performance or longer battery life
- Better protection of ICs against mechanical shock, vibration and physical damage
- Full shielding of the electronics as a final metal coating can be applied
- Improved thermal performance
- Integral edge card connector capable
- Improved design for memory modules
- Improved design for phone modules
- Improved design for computer card modules
- Improved design for smart and RFID cards
- Improved lighting modules

The details of the present invention, both as to its structure and operation, and many of the attendant advantages of this invention, can best be understood in reference to the
following detailed description, when taken in conjunction with the accompanying drawings, in which like reference numerals refer to like parts throughout the various views unless otherwise specified, and in which:

5 BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of a prior solder assembly employing a gull wing component on a PCB.

Figure 2 is a cross-sectional view of a prior solder assembly employing either a Ball Grid Array (BGA) or a Land Grid Array (LGA) component on a PCB.

Figure 3 is a cross-sectional view of a prior solderless assembly employing an electrical component.

Figure 4 is a cross-sectional view of a portion of a RIP assembly employing a LGA component.

Figure 5 is a cross-sectional view of a portion of a RIP assembly employing a LGA component with an optional heat spreader and heat sink.

Figure 6 is a cross-sectional view of a two layer RIP assembly showing mounted discrete, analog, and LGA components.

Figure 7 is a cross-sectional view of a pair of mated two layer RIP subassemblies.

Figure 8 is a cross-sectional view of a stage in the manufacture of a representative RIP assembly.

Figure 9 is a cross-sectional view of a stage in the manufacture of a representative RIP assembly.
Figure 10 is a cross-sectional view of a stage in the manufacture of a representative RIP assembly.

Figure 11 is a perspective representation of a RIP subassembly.

Figure 12 is a cross-sectional view of a stage in the manufacture of a representative RIP assembly.

Figure 13 is a perspective representation of a RIP subassembly.

Figure 14 is a cross-sectional view of a side drawing of a RIP subassembly.

Figure 15 is a cross-sectional view of a stage in the manufacture of a representative RIP assembly.

Figure 16 is a cross-sectional view of shows a stage in the manufacture of a representative RIP assembly.

Figure 17 is a cross-sectional view of a stage in the manufacture of a representative RIP assembly.

Figure 18 is a cross-sectional view of the registration and bringing together of two RIP subassemblies.

Figure 19 is a cross-sectional view of a completed mated pair of two RIP subassemblies.

DETAILED DESCRIPTION

In the following description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, the interconnection between
conductor elements of components (i.e., component VO leads) may be shown or described as having multi-conductors interconnecting to a single lead or a single conductor signal line connected to multiple component contacts within or between devices. Thus each of the multi-conductor interconnections may alternatively be a single-conductor signaling, control, power or ground line and vice versa. Circuit paths shown or described as being single-ended may also be differential, and vice-versa. The interconnected assembly may be comprised of standard interconnections; microstrip or stripline interconnections and all signal lines of the assembly may be either shielded or unshielded.

Figure 1 shows a prior completed assembly 100, with solder joint 110, of a gull wing component package 104 solder-mounted on a PCB 102. Component package 104 contains electrical component 106. The component 106 may be either an IC or another discrete component. Gull wing lead 108 extends from package 104 to flow solder 110 which in turn connects lead 108 to pad 112 on PCB 102. Insulating material 114 prevents flow solder 110 from flowing to and shorting component 106 with other components (not shown) on PCB 102. Pad 112 connects to through hole 118 which in turn connects to proper traces such as ones indicated by 116. In addition to the aforementioned problems with solder joints, this type of assembly, including the internal structure of PCB 102, is complex and requires height space that is reduced in the present invention.

Figure 2 shows a prior completed assembly 200, with solder joint 202, of either a BGA IC or a LGA IC package 204 on a PCB 214. A primary difference from Figure 1 is the use of ball solder 202 as opposed to flow solder 110.
Component package 204 contains component 206. Lead 208 extends from package 204 through support 210 (typically composed of organic or ceramic material) to ball solder 202 which in turn connects lead 208 to pad 212 on PCB 214. Insulating material 216 prevents ball solder 202 from shorting other leads (not shown) contained in package 204. Insulating material 218 prevents ball solder 202 from flowing to and shorting component 206 with other components (not shown) on PCB 214. Pad 212 connects to through hole 220 which in turn connects to proper traces such as ones indicated by 222. The same problems are present with this configuration as with the assembly shown in Figure 1: In addition to the aforementioned problems with solder joints, this type of assembly is complex, particularly because of the PCB 214, and requires height space that is reduced in the present invention.

Figure 3 illustrates a prior solderless connection apparatus 300. See U.S. Patent 6,160,714 (Green). In this configuration, substrate 302 supports a package 304. Package 304 contains an electrical component (not shown) such as an IC or other discrete component. Overlying substrate 302 is insulating material 306. On the other side of the substrate 302, is a conductive, polymer-thick-film ink 308. To improve conductivity, a thin film of copper is plated 310 on polymer-thick-film 308. A via extends from the package 304 through substrate 302. The via is filled with a conductive adhesive 314. The point of attachment 316 of package 304 to adhesive 314 may be made with fusible polymer-thick-film ink, silver polymer-thick-film conductive ink, or commercial solder paste. One disadvantage of this prior art assembly over the present invention is the additional thickness added by the adhesive 314 as illustrated by bump 318.

RIP Apparatus
Figure 4, an apparatus 400 illustrative of the present invention, shows a LGA component package (402, 406, 408, 410, 412, 414) mounted on a substrate 416 which does not have to be a PCB. It will be obvious to one skilled in the art that a BGA, gull wing, or other IC package structure or any type of discrete component may substitute for the LGA component. The connection is simpler, solder free, and lower profile than the assemblies shown in Figures 1, 2, and 3.

Adhering to package 402 is electrically insulating material 404. Material 404 is shown attached to 1 side of package 402. However, material 404 may be attached to 2 sides of package 402, more than 2 sides of package 402, or may in fact envelop package 402. As applied, material 404 may give the apparatus strength, stability, structural integrity, toughness (i.e., it is non-brittle), and dimensional stability. Material 404 may be reinforced by the inclusion of a suitable material such as a glass cloth.

Component package 402 contains electrical component 406 (such as an IC, discrete, or analog device; collectively referred to as "component" in this application including claims), supports 408 and 410 (preferably composed of organic or ceramic material), lead 412, and insulating material 414. While component package 402, as manufactured and shipped in many cases, incorporates insulating material 414, this legacy feature may potentially be eliminated in the future thus reducing the profile of the assembly 400. Either supports 408 and 410 or, if present, insulating material 414 sit on substrate 416 which is preferably made of insulating material. Some portion or all of substrate 416 may be made of electrically conductive material if it is desired to short leads (e.g., 412) extending from package 402.
Attachment of lead 412 to insulating material 414 and substrate 416 may be realized by adhesive dots as well as by other well known techniques.

A first set of vias, an example of which is via 420, extends through substrate 416, extends through insulating material 414, if present, reaches, and exposes leads such as lead 412. The vias 420 are plated or filled with an electrically conductive material (in many cases copper (Cu), although silver (Ag), gold (Au), or aluminum (Al) as well as other suitable materials, may be substituted). The plate or fill fuse with leads 412 forming an electrical and mechanical bond.

The substrate 416 may include a pattern mask (not shown) which is plated, or the plate or fill introduced into the first set of vias (e.g., via 420) may extend under the substrate 416 and provide a required first set of traces. Other traces may be created. A layer 422, also of insulating material, may underlay substrate 416 and first traces. The purpose of 422 is to provide a platform for a second set of traces (if required) and to electrically insulate the first set of traces from the second set of traces.

A second set of vias, an example of which is via 426, extends through layer 422, reaches, and exposes traces and/or leads (e.g., lead 428) under substrate 416. As discussed above, referring to the first set of vias (e.g., via 420), the second set of vias may be plated or filled so that they fuse with desired leads (e.g., lead 428) under substrate 416. As above, one or more traces 430 may extend under layer 422.

This layering continues as needed. By repeating the above structure, multiple layers (not shown), and additional traces and vias may be built. A surface insulating material 432 under coats the last layer. Leads or electrical connectors (e.g., lead 434) may extend beyond
the surface insulating material 432. This provides contact surfaces (e.g., surface 436) to permit connection with other electrical components or circuit boards.

Figure 5, apparatus 500, shows optional heat dissipation features. Subassembly 400, previously described in Figure 4, may have on top of the package 402 and material 404 a heat spreader 506 and/or a heat sink 508 to dissipate heat generated by component 406. A thermal interface material (not shown) may be used to join the heat sink to the heat spreader. Optionally, material 404 may include in its composition a heat conductive (although electrically insulating) material such as silicon dioxide (SiC\(^\text{\textregistered}\)) or aluminum dioxide (\(\text{AlO}_2\)) to enhance heat flow from package 402. If heat spreader 506 and heat sink 508 are made of one or more substances well known in the art, they may provide electromagnetic interference (EMI) protection to the subassembly 400 and help protect against static electricity discharges.

In accordance with a two layer RIP apparatus, a section of which is shown in Figure 5, Figure 6 shows apparatus 600 with a mounted sample set of components, including a discrete gull wing component 602, an analog component 604, and a LGA IC 606.

It will be apparent to someone skill in the art that the RIP apparatus is less complicated than a PCB containing soldered components. That is, just a PCB by itself is a complex device requiring dozens of steps to manufacture. The RIP apparatus, by not requiring a PCB board, is simpler and requires fewer steps to manufacture a complete electronic assembly.

As an option, the Figure 7 apparatus 700 shows two RIP subassemblies, 702 and 704, joined together at the plated and/or filled vias (e.g., 706a, 706b) and/or at the leads (e.g., 708a, 708b).

RIP Method of Manufacture
Figures 8 to 17 show a method of manufacture of a RIP assembly. It will be apparent to one skilled in the art that the sequence of steps may be varied without departing from the scope and spirit of this invention.

Figure 8, stage 800, shows the initial mounting of packaged components, 802, 804, and 806 on a substrate 808. The components may be held in place by a number of different techniques and/or substances well known in the art including applying spot or conductive adhesive or by bonding to a tacky film of component leads to substrate 808. The material for applying or bonding may be suitable for holding and later releasing the components.

Figure 9, stage 900, shows another step in the RIP method of manufacture. At this stage, the partial apparatus of Figure 8 is flipped. The initially mounted packaged components 802, 804, and 806 are encased in electrically insulating material 908. Material 908 provides support for packaged components 802, 804, and 806 as well as electrical insulation from each other. If material 908 contains heat conductive, but electrically insulating matter, such as AlO2 or SiCh, it will also aid in dissipating heat.

Figure 10, stage 1000, shows another step in the RIP method of manufacture. Vias (e.g., 1002) through substrate 808 are created, reaching and exposing leads of packaged components 802, 804, and 806. Vias (e.g., 1002) may be formed or drilled (collectively referred to as "formed" in this application including claims) by any number of known techniques including laser drilling.

Figure 11, partial assembly 1100, as shown at the completion of stage 1000, is a perspective view of a top side of substrate 808 showing vias (e.g., 1102).

Figure 12, stage 1200, illustrates how direct printing of circuits can be achieved. Vias (e.g., 1202) may be plated or filled with electrically conductive material and traces and
leads (e.g., 1208) on substrate 808 may be created by device 1206. Using any number of techniques well known in the art, device 1206 may fill vias 1202, print leads and traces 1208, and/or plate leads and traces 1208 onto substrate 808.

Traces (e.g., 1302) and leads (e.g., 1304), created in accordance with stage 1200 on substrate 808, are shown in perspective view in Figure 13, partial apparatus 1300.

Partial apparatus 1400, created in accordance with stage 1200 is shown in side view in Figure 14. Filled vias (e.g., via 1402) are shown extending through substrate 808 to component leads (e.g., lead 1406).

In Figure 15, showing stage 1500, a layer of insulating material 1502 and a second set of vias (e.g., via 1504) are formed on top of substrate 808. The vias extend to and expose leads (e.g., 1506) on top of substrate 808.

In Figure 16, a stage showing creation of subassembly 1600, plating and/or filling vias (e.g., 1602) and making traces (e.g., 1604) are completed on layer 1502.

In this manner, additional layers may be built up. Eventually, as shown in Figure 17, stage 1700, insulating material 1702 is laid on top of the top layer of subassembly 1600. In addition, heat spreader 1706 and heat sink 1708 may be attached underneath material 908.

An alternative to laying material 1702 on top of subassembly 1704 is shown in Figure 18, stage 1800, and Figure 19, stage 1900. In Figure 18, the leads, fills, and traces of subassemblies 1600 are registered with each other and then brought together.

Figure 19 shows the addition of a bonding agent 1908, using any suitable process and material (e.g., applying anisotropic conductive film), joining together subassemblies 1600.

As described above and shown in Figure 17 for one subassembly, but not shown in Figure 19,
heat spreaders and heat sinks may be added underneath support material 1904 and on top of support material 1906.

While the particular system, apparatus, and method for ELECTRONIC ASSEMBLIES WITHOUT SOLDER as herein shown and described in detail is fully capable of attaining the above-described objects of the invention, it is to be understood that it is the presently preferred embodiment of the present invention and is thus representative of the subject matter which is broadly contemplated by the present invention, that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular means "at least one". All structural and functional equivalents to the elements of the above-described preferred embodiment that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.
I claim:

1. A circuit assembly 400 comprising:
   a substrate 416,
   a component package 402 with one or more leads 412,
   an insulating material 404 attaching the component package 402 with the substrate 416; and
   at least one via 420 extending through the substrate 416 to the one or more leads 412.

2. A circuit assembly 400 comprising:
   a substrate 416 having a planar first side and a planar second side,
   a least one component 406 with a first set of one or more leads 412, the component 406 having at least two sides,
   a first electrically insulating material 404 attaching at least one of said two sides of the component 406 with said first planar side of said substrate 416, and
   at least one via 420 extending from the second planar side of the substrate 416 exposing the first set of one or more leads 412.

3. A circuit assembly 400 comprising:
   a substrate 416 having a planar first side and a planar second side,
   a least one component package 402 with a first set of one or more leads 412, the component package 402 having at least two sides;
   a first electrically insulating material 404 attaching at least one of the two sides of the component package 406 with the first planar side of the substrate 416, and
at least one via 420 extending from the second planar side of the substrate 416 exposing the first set of one or more leads 412.

4. The assembly of claim 3 wherein the substrate 416 is electrically insulating.

5. The assembly of claim 3 wherein the first electrically insulating material 404 envelopes the component package 402.

6. The assembly of claim 3 wherein the first electrically insulating material 404 is thermally conductive.

7. The assembly of claim 3 wherein the assembly further comprises a heat spreader 506.

8. The assembly of claim 3 wherein the assembly further comprises a heat sink 508.

9. The assembly of claim 3 further comprising the at least one via 420 filled with a conductive material electrically connecting with the first set of one or more leads 412.

10. The assembly of claim 9 wherein the conductive material is selected from a group comprising copper, silver, aluminum, gold, tin, a metal alloy, electrically conductive film, electrically conductive adhesive, and electrically conductive ink.

11. The assembly of claim 9 wherein the conductive material is plated to the substrate 416.
12. The assembly of claim 9 wherein the conductive material is printed on the substrate 416.

13. The assembly of claim 9 wherein the conductive material forms a second set of one or more leads 428 on the substrate 416.

14. The assembly of claim 9 further comprising a second electrically insulating material 422 on the second side of the substrate 416, the second material 422 covering at least one of the least one via 420.

15. The assembly of claim 14 further comprising a second set of at least one via 426, the second set of the at least one via 426 extending through the second insulating material 422 and exposing at least one of the first set of one or more leads 412.

16. A method of making a circuit assembly comprising:

placing 800 at least one component 406 on a substrate 808, the component 406 having at least two sides, the substrate 808 having a first planar side and a second planar side, incorporating 900 a first electrically insulating material 908, the insulating material 908 attaching at least one side of the at least one component 406 with the first planar side of the substrate 808, and

forming 1000 a first set of at least one via 1002 through the second planar side of substrate 808 to expose a first set of at least one lead 412 of the at least one component 406.
17. A method of making a circuit assembly comprising:
placing at least one component package on a substrate, the component package having at least two sides, the substrate having a first planar side and a second planar side,
incorporating a first electrically insulating material, the insulating material attaching at least one side of the component package with the first planar side of the substrate, and
forming a first set of at least one via through the second planar side of substrate to expose a first set of at least one lead of the component package.

18. The method of claim 17 further comprising filling the first set of at least one via with a first electrically conductive material.

19. The method of claim 18 wherein the first electrically conductive material forms a second set of at least one lead.

20. The method of claim 19 further comprising:
forming a first layer of a second electrically insulating material on the substrate wherein the second insulating material covers the first electrically conductive material.

21. The method of claim 20 further comprising:
forming 1500 a second set of at least one via 1504 extending through the layer 1502 exposing; a second set of at least one lead 1208, 1506.

22. The method of claim 21 further comprising:

filling 1602 the second set of at least one via 1504 with a second electrically conductive material.

23. A product manufactured by the process of claim 17.
Figure 13
Figure 14

Figure 15
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

INV. H05K1/18 H01L23/538

According to International Patent Classification (IPC) or to both national classification and IPC

**B. RELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

HOIL H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>WO 2004/001848 A (BJORSELL STEN [IE]) 31 December 2003 (2003-12-31) the whole document</td>
<td>1-23</td>
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**D. Further documents are listed in the continuation of Box C**

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- Date of the actual completion of the international search: 8 September 2008

- Date of mailing of the international search report: 16/09/2008

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