Abstract: In one embodiment of the invention, an error-correcting receiver includes an input buffer for storing received codewords, a first error correction syndrome circuit coupled to receive a first codeword and produce an output word, and a second error correction syndrome circuit coupled to receive a second codeword and produce an output word. An error-trapping-and-decoding circuit alternately receives the output words of the first and second error correction syndrome circuits. An error correction circuit coupled to the error-trapping-and-decoding circuit and the input buffer is adapted to provide corrected codewords.
INTERNATIONAL SEARCH REPORT

International application No
PCT/US 06/30208

A CLASSIFICATION OF SUBJECT MATTER
IPC(8)- H03M 13/00; G06F 11/00 (2007.01)
USPC - 714/785; 714/758; 714/699

According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC 714/785, 714/758, 714/699

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC All classes/subclasses (text search - see terms below)

Electronic database consulted during the international search (name of database and, where practicable, search terms used)
PubWEST(PGPT,PGPB,EPAB,JPAB),
Search Terms syndrome error correction circuit, syndrome circuit,

C DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Category</th>
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<th>Relevant to claim</th>
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<td>X</td>
<td>US 2004/01 77312 A1 (Xm) 9 September 2004 (09 09 2004), entire document</td>
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<td>Y</td>
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Further documents are listed in the continuation of Box C

Date of the actual completion of the international search
27 January 2007 (27 01 2007)

Date of mailing of the international search report
8 MAR 2008

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