Title: VOLTAGE LEVEL SHIFTER CIRCUIT HAVING HIGH SPEED AND LOW SWITCHING POWER

Abstract: A voltage level shifter (500) comprises a plurality of PMOS transistors (510A, 512A) coupled in series with NMOS transistors (510B, 512B) to form a plurality of pull-down inverters (510, 512). When the second voltage level is enabled to connect, the pull-down inverters pull down faster than the pull-down NMOS transistors alone. The pull-up PMOS transistors (514, 516) pull up immediately to connect the first voltage level to the second voltage level. Thus, the PMOS transistors added to form pull-down inverters improve the switching time and eliminate the kinks in the output voltage.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H03L 5/00; H03K 19/0175
US CL : 327/333; 326/68, 81

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/333; 326/68, 81

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data bases consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>WO 98/58382(TANAKA et al.) 23 December 1998 (23.12.98), Figures 6, 27</td>
<td>1-3, 5</td>
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<td>Y</td>
<td>Applicant Admitted Prior Art, Figure 3</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

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Date of the actual completion of the international search: 23 June 2004 (23.06.2004)

Date of mailing of the international search report: OCT 2004

Name and mailing address of the ISA/US

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Form PCT/ISA/210 (second sheet) (July 1998)