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(54) Title: METHOD OF MANUFACTURING OPTICAL DEVICES AND RELATED IMPROVEMENTS

(57) Abstract: There is disclosed an improved method of manufacturing of an optical device (40), particularly semiconductor optoelectronic devices such as laser diodes, optical modulators, optical amplifiers, optical switches, and optical detectors. The invention provides a method of manufacturing optical device (40), a device body portion (15) from which the device (40) is to be made including a Quantum well (QW) structure (30), the method including the step of: processing the device body portion (15) so as to create extended defects at least in a portion (53) of the device portion (5). Each extended defect is a structural defect comprising a plurality of adjacent "point" defects.

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METHOD OF MANUFACTURING OPTICAL DEVICES
AND RELATED IMPROVEMENTS

FIELD OF INVENTION

This invention relates to a method of manufacturing of optical devices, and in particular, though not exclusively, to manufacturing integrated optical devices or optoelectronic devices, for example, semiconductor optoelectronic devices such as laser diodes, optical modulators, optical amplifiers, optical switches, optical detectors, and the like. The invention further relates to Optoelectronic Integrated Circuits (OEICs) and Photonic Integrated Circuits (PICs) including such devices.

BACKGROUND TO INVENTION

Quantum Well Intermixing (QWI) is a process which has been reported as providing a possible route to monolithic optoelectronic integration. QWI may be performed in III–V semiconductor materials, eg Aluminium Gallium Arsenide (AlGaAs) and Indium Gallium Arsenide Phosphide (InGaAsP), which may be grown on binary substrates, eg Gallium Arsenide (GaAs) or Indium Phosphide (InP). QWI alters the band-gap of an as-grown structure through interdiffusion of elements of a Quantum Well (QW) and associated barriers to produce an alloy of the constituent components. The alloy has a band-gap which is larger than that of the as-grown QW. Any optical radiation (light) generated within the QW where no QWI has taken place can therefore pass through a QWI or "intermixed" region of alloy which is effectively transparent to the said optical radiation.

Various QWI techniques have been reported in the literature. For example, QWI can be performed by high temperature diffusion of elements such as Zinc into a semiconductor material including a QW.

QWI can also be performed by implantation of elements such as silicon into a QW
semiconductor material. In such a technique the implantation element introduces point defects in the structure of the semiconductor material which are moved through the semiconductor material inducing intermixing in the QW structure by a high temperature annealing step.

Such QWI techniques have been reported in "Applications of Neutral Impurity Disordering in Fabricating Low-Loss Optical Waveguides and Integrated Waveguide Devices", Marsh et al, Optical and Quantum Electronics, 23, 1991, s941 – s957, the content of which is incorporated herein by reference.

A problem exists with such techniques in that although the QWI will alter (increase) the band-gap of the semiconductor material post-growth, residual diffusion or implantation dopants can introduce large losses due to the free carrier absorption coefficient of these dopant elements.

A further reported QWI technique providing intermixing is Impurity Free Vacancy Diffusion (IFVD). When performing IFVD the top cap layer of the III–V semiconductor structure is typically GaAs or Indium Gallium Arsenide (InGaAs). Upon the top layer is deposited a silica (SiO₂) film. Subsequent rapid thermal annealing of the semiconductor material causes bonds to break within the semiconductor alloy and Gallium ions or atoms – which are susceptible to silica (SiO₂) – to dissolve into the silica so as to leave vacancies in the cap layer. The vacancies then diffuse through the semiconductor structure inducing layer intermixing, eg in the QW structure.

IFVD has been reported in "Quantitative Model for the Kinetics of Compositional Intermixing in GaAs–AlGaAs Quantum-Confined Heterostructures", by Helmy et al, IEEE Journal of Selected Topics in Quantum Electronics, Vol 4, No 4, July/August 1998, pp 653 – 660, the content of which is incorporated herein by
reference.

It is an object of at least one aspect of the present invention to obviate or at least mitigate at least one of the aforementioned disadvantages/problems in the prior art.

It is also an object of at least one aspect of the present invention to provide an improved method of manufacturing an optical device using an improved QWI process.

**SUMMARY OF INVENTION**

According to a first aspect of the present invention, there is provided a method of manufacturing an optical device, a device body portion from which the device is to be made including a Quantum Well (QW) structure, the method including the step of processing the device body portion so as to create extended defects at least in a portion of the device portion.

Each extended defect may be understood to be a structural defect comprising a plurality of adjacent "point" defects.

Preferably said step of processing the device body portion comprises performing a plasma etch on the device body portion. Preferably and advantageously the said step of performing a plasma etch on the device body portion may be performed in a sputterer. In said step of sputtering from the device body portion a magnetic field may be provided around the device body portion. In said step of sputtering from the device body portion, a magnetron sputterer may be used.

In said step of performing a sputter etch on the device body portion a (reverse) electrical bias may be applied across an electrode upon which the device body portion is provided so as to provide a "pre-etch" or cleansing of the device body
portion. Preferably the sputter-etch is carried out for between 0.5 and 10 minutes at a power between 300 and 750 W, at a sputter pressure between 1 and 5 µm Hg.

The method may include the preferred step of depositing a dielectric layer on at least one other portion of the device body portion. The dielectric layer may therefore act as a mask in defining the at least one portion. The method may also include the subsequent step of depositing a further dielectric layer on the dielectric layer and/or on the at least one portion of the device body portion.

Advantageously the dielectric layer and/or further dielectric layer may be deposited by use of a sputterer. Alternatively, the dielectric layer and/or the further dielectric layer may be deposited by a deposition technique other than by use of a sputterer, eg Plasma Enhanced Chemical Vapour Deposition (PECVD). By either of these deposition techniques at least one low damage dielectric layers is provided which does not substantially affect an adjacent portion of the device body portion.

The dielectric layer or layers may beneficially substantially comprise silica (SiO₂); or may comprise another dielectric material such as Aluminium Oxide (Al₂O₃).

Preferably, the sputterer includes a chamber which may be substantially filled with an inert gas such as argon, preferably at a pressure of around 2 microns of Hg, or a mixture of argon and oxygen, eg in the proportion 90% / 10%.

The step(s) of depositing the dielectric layer(s) may comprise part of a Quantum Well Intermixing (QWI) process used in manufacture of the device. The QWI process may comprise Impurity-Free Vacancy Disordering (IFVD).

Preferably, the method of manufacture also includes the subsequent step of
annealing the device body portion including the dielectric layer at an elevated temperature.

It has been surprisingly found that by performing the plasma etch on the device body portion as a step in a QWI technique such as IFVD, preferably by use of a sputterer, damage induced extended defects appear to be introduced into the at least one portion of the device body portion; the at least one portion may, for example, comprise at least a part of a top or "capping" layer. It is believed that the damage arises due to breakage of bonds in the capping layer before annealing, eg the application of thermal energy by rapid thermal annealing, thereby inhibiting transfer of Gallium from the at least one portion, eg into the further dielectric layer.

Preferably the method of manufacture also includes the preceding steps of:

- providing a substrate;
- growing on the substrate:
  - a first optical cladding layer;
  - a core guiding layer including a Quantum Well (QW) structure; and
  - a second optical cladding layer.

The first optical cladding layer, core guiding layer, and second optical cladding layer may be grown by Molecular Beam Epitaxy (MBE) or Metal Organic Chemical Vapour Deposition (MOCVD).

In a preferred embodiment the method may comprise the steps of:

- depositing the dielectric layer on a surface of the device body portion;
- defining a pattern in photoresist on a surface of the dielectric layer and lifting off at least part of the photoresist so as to provide the dielectric layer on said at least one other portion of the device body portion.
In said preferred embodiment, the method may also include the step of depositing the further dielectric layer on a portion of the surface of the device body and on a surface of the dielectric layer prior to annealing.

In said preferred embodiment, the dielectric layer may comprise an intermixing cap; while the at least one portion of the device body portion and/or the further dielectric layer may comprise an intermixing suppressing cap. The thickness of the dielectric layer(s) may be between 10 and 1000 nm. More preferably, the thickness of the dielectric layers may be 200 or 300 nm.

A subsequent annealing step may occur at a temperature of between 700 and 1000°C for between 0.5 and 5 minutes, more preferably between 800 and 1000°C and in one embodiment at substantially 900°C for around 1 minute.

According to a second aspect of the present invention there is provided a method of manufacturing an optical device, a device body portion from which the device is to be made including a Quantum Well (QW) structure, the method including the step of performing a plasma etch on the device body portion. Preferably the step of performing a plasma etch on the device body portion is carried out using a sputterer.

According to a third aspect of the present invention there is provided an optical device fabricated from a method according to either of the first or second aspects of the present invention. The optical device may be an integrated optical device or an optoelectronic device.

The device body portion may be fabricated in a III–V semiconductor materials system. In a most preferred embodiment the III–V semiconductor materials
system may be a Gallium Arsenide (GaAs) based system, and may operate at a
wavelength(s) of substantially between 600 and 1300 nm. Alternatively, in a less
preferred embodiment the III–V semiconductor materials system may be an
Indium Phosphide based system, and may operate at a wavelength(s) of
substantially between 1200 and 1700 nm. The device body portion may be made
at least partly from Aluminium Gallium Arsenide (AlGaAs) and / or Indium
Gallium Arsenide (InGaAs), Indium Gallium Arsenide Phosphide (InGaAsP),
Indium Gallium Aluminium Arsenide (InGaAlAs) and/or Indium Gallium
Aluminium Phosphide (InGaAlP).

The device body portion may comprise a substrate upon which are provided a first
optical cladding layer, a core guiding layer, and a second optical cladding layer.
Preferably the Quantum Well (QW) structure is provided within the core guiding
layer. The core guiding layer, as grown, may have a smaller band-gap and higher
refractive index than the first and second optical cladding layers.

According to a fourth aspect of the present invention there is provided an optical
integrated circuit, optoelectronic integrated circuit (OEIC), or photonic integrated
circuit (PIC) including at least one optical device according to the third aspect of
the present invention.

According to a fifth aspect of the present invention there is provided a device body
portion ("sample") when used in a method according to either the first or the
second aspects of the present invention.

According to a sixth aspect of the present invention there is provided a wafer of
material including at least one device body portion when used in a method
according to either of the first or second aspects of the present invention.
According to a seventh aspect of the present invention there is provided a plasma etching apparatus when used in a method according to the second aspect of the present invention. Preferably the sputtering apparatus is a sputterer, which may be a magnetron sputterer.

According to an eighth aspect of the present invention there is provided use of a sputtering apparatus in a method according to either of the first or second aspects of the present invention.

**BRIEF DESCRIPTION OF DRAWINGS**

Embodiments of the present invention will now be described, by way of example only, and with reference to the accompanying drawings, which are:

Figure 1 a side view of a device body portion, as grown, for use in a method of manufacture of an optical device according to an embodiment of the present invention;

Figure 2 a side view of an optical device according to an embodiment of the present invention manufactured from the device body portion of Figure 1;

Figure 3 a schematic view of band-gap energies of a part of the device body portion of Figure 1 the part comprising a core layer including a Quantum Well (QW) therein;

Figure 4 a schematic view similar to Figure 3 of band-gap energies of a corresponding part of the optical device of Figure 2 when Quantum Well Intermixed (QWI);

Figures 5 (a) to (g) a series of schematic side views of a device body portion during various steps of a method of manufacture of the optical device of Figure 2;

Figure 6 a simplified schematic representation of a magnetron sputterer apparatus suitable for use in the method of manufacturing
Figures (a) to (g);

Figure 7 a more detailed schematic representation of the magnetron sputterer Figure 6;

Figures 8 (a) and (b) more detailed schematic side views of the device body portion of Figures 5 (a) to (g) before and after an annealing step shown in Figure 5(g); and

Figures 9 (a) to (c) schematic representations of various possible configurations of the magnetron sputterer apparatus of Figure 6.

10 **DETAILED DESCRIPTION OF DRAWINGS**

Referring initially to Figure 1, there is shown a device body portion, generally designated 5, as grown, for use in a method of manufacture of an optical device according to a first embodiment of the present invention. The optical device is an integrated optical device or an optoelectronic device.

15 The device body portion 5 is suitably fabricated in a III-V semiconductor material system, most preferably such as Gallium Arsenide (GaAs), and operating at a wavelength(s) of substantially between 600 and 1300 nm, or alternatively, though less preferably, Indium Phosphide (InP), and operating at a wavelength(s) of substantially between 1200 and 1700 nm. The device body portion 5 may be made at least partly from Aluminium Gallium Arsenide (AlGaAs) and/or Indium Gallium Arsenide (InGaAs), Indium Gallium Arsenide Phosphide (InGaAsP), Indium Aluminium Gallium Arsenide (InGaAlAs) and/or Indium Gallium Aluminium Phosphide (InGaAlP). In this described first embodiment, the device body portion is made from AlGaAs.

The device body portion 5 may form part of a semiconductor wafer together with a plurality of other possibly like optical devices which may be cleaved from the wafer after processing. The device body portion 5 comprises substrate 10 upon
which is provided a first optical cladding layer 15, a core guiding layer 20, and a second optical cladding layer 25. A Quantum Well (QW) structure 30, including at least one Quantum Well, is provided within the core guiding layer 20, as grown. On the second optical cladding layer 30 there is provided a capping layer 35.

As will be appreciated, the core guiding layer 20, as grown, has a smaller band-gap and higher refractive index than the first and second optical cladding layer 15, 25.

In particular, the process described herein is optimised for use in conjunction with an InGaAs–InAlGaAs–InP material emitting at 1450 to 1550 nm, the structure of which is defined in the table below:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Fig 1 ref</th>
<th>Material</th>
<th>Comp. %</th>
<th>Comp. range %</th>
<th>Thickness (nm)</th>
<th>Thickness Range (nm)</th>
<th>Dopant Conc. (cm²)</th>
<th>Dopant conc. range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>10</td>
<td>InP</td>
<td>-</td>
<td>-</td>
<td>3500</td>
<td>3000-5000</td>
<td>n(Si)</td>
<td>1e18</td>
</tr>
<tr>
<td>1st Opt Cladding</td>
<td>15</td>
<td>InP</td>
<td>-</td>
<td>-</td>
<td>500</td>
<td>500-2500</td>
<td>n(Si)</td>
<td>8e17</td>
</tr>
<tr>
<td>Core Guiding</td>
<td>20</td>
<td>InAlGaAs</td>
<td>53% In, 31% Ga, 16% Al</td>
<td>53% In, 0-35 %, 15-47%</td>
<td>210</td>
<td>100-400</td>
<td>i</td>
<td>-</td>
</tr>
<tr>
<td>QW</td>
<td>30</td>
<td>InGaAs</td>
<td>53% In, 45-70%</td>
<td>7</td>
<td>3-10</td>
<td>i</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2nd Opt Cladding</td>
<td>25</td>
<td>InP</td>
<td>-</td>
<td>-</td>
<td>2100</td>
<td>1000-2500</td>
<td>p(Zn)</td>
<td>7e17</td>
</tr>
<tr>
<td>Cap</td>
<td>35</td>
<td>InGaAs</td>
<td>53% In, -</td>
<td>150</td>
<td>100-300</td>
<td>p(Zn)</td>
<td>2e19</td>
<td>5e18-1e20</td>
</tr>
</tbody>
</table>

The parameters above refer to MOVPE-grown material of preferred thickness, and preferred thickness range. In InGaAs–InGaAsP–InP material, the core guiding layer 20 InAlGaAs is replaced with InGaAsP with similar properties, i.e. band gap. For MBE-grown material the p-type dopant becomes Be while other parameters can remain the same.

Referring now to Figure 2, there is shown an optical device, generally designated 40, manufactured from the device body portion 5 of Figure 1, by a method which will be described in detail hereinafter. As can be seen from Figure 2, the device 40 comprises an active region 45 and a passive region 50. In this embodiment the active region 45 comprises a Quantum Well (QW) amplifier. However, it should
be understood that the active region 45 may in other embodiments, comprise a laser, modulator, switch, detector or like active (electrically controlled) optical device. Further, the passive region 50 comprises a low-loss waveguide wherein the Quantum Well structure 30 has been at least partially removed by a Quantum Well Intermixing (QWI) technique, as will hereinafter be described in greater detail.

The device 40 has excellent alignment between the core layer 20 waveguiding regions of the active region 45 and passive region 50, and has a reflection coefficient between the active region 45 and passive region 50 which is substantially negligible (of the order of 10^{-6}). Further, mode matching between the active region 45 and the passive region 50 is intrinsic to the device 40.

Typically, the substrate 10 is n-type doped to a first concentration, while the first cladding layer 15 is n-type doped to a second concentration. Further, the core layer 20 is typically substantially intrinsic, while the second cladding layer 25 is typically p-type doped to a third concentration. Further, the cap layer (or contact layer) 35 is p-type doped to a fourth concentration. It will be appreciated by those skilled in the art that the cap layer 35 and second cladding layer 25 may be etched into a ridge (not shown), the ridge acting as an optical waveguide to confine optical modes within the core layer 20 both within the optically active region 45 and the optically passive region 50. Further, contact metallisations (not shown) may be formed on at least a portion of a top surface of the ridge within the optically active region 45, and also on an opposing surface of the substrate 10, as is known in the art.

It will further be appreciated that the device 40 may comprise part of an optical integrated circuit, optoelectronic integrated circuit (OEIC), or photonic integrated circuit (PIC) which may comprise one or more of such optical devices 40.
Referring now to Figure 3, there is shown a schematic representation of the band-gap energies of a Quantum Well 31 of the Quantum Well structure 30 within the core layer 20 of the device body portion 5, as grown. As can be seen from Figure 3, the AlGaAs core layer 20 includes at least one Quantum Well 31, with the Quantum Well structure 30 having a lower Aluminium content than the surrounding core layer 20, such that the band-gap energy of the Quantum Well structure 30 is less than that of the surrounding AlGaAs core layer 20. The Quantum Well structure 30 is typically around 3 to 20 nm thick, and more typically around 10 nm in thickness.

Referring now to Figure 4, there is shown a corresponding portion 32 of the core layer 20 as in Figure 3, but which has been Quantum Well Intermixed (QWI) so as to effectively increase the band-gap energy (meV) of the part 32 which corresponds to the Quantum Well 31 of the Quantum Well structure 30. Quantum Well Intermixing (QWI) therefore essentially "washes out" the Quantum Well structure 30 from the core layer 20. The portion shown in Figure 4 relates to the passive region 50 of the device 40. As will be understood, optical radiation transmitted from or generated within the optically active region 45 of device 40 will be transmitted through the low loss waveguide provided by the Quantum Well Intermixed (QWI) region 32 of the core layer 20 of the passive region 50.

Referring now to Figures 5(a) to (g), there is illustrated a first embodiment of a method of manufacturing an optical device 40 from a device body portion 5, including a Quantum Well (QW) structure 30 according to the present invention, the method including the steps (see Figures 5(d) to (e)) of processing the device body portion 5 so as to create extended defects at least in a portion 53 of the device body portion 5.
The method of manufacture begins (see Figure 5(a) with the step of providing substrate 10, growing on the substrate 10 first optical cladding layer 15, core guiding layer 20 including at least one Quantum Well (QW) 30, second optical cladding layer 25, and cap layer 35.

5

The first optical cladding layer 15, core guiding layer 20, second optical cladding layer 25, and cap layer 35 may be grown by known semiconductor epitaxial growth techniques such as Molecular Beam Epitaxy (MBE) or Metal Organic Chemical Vapour Deposition (MOCVD).

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Once the device of body 5 has been grown – normally as part of a wafer (not shown) including a plurality of such device body portions 5, a dielectric layer 51 is deposited on a surface 52 of the cap layer 35 (see Figure 5(b). A pattern is then defined in Photoresist (PR) 55 on a surface 54 of the dielectric layer 51. The Photoresist 55 is then lifted off so as to leave at least one portion 56 of the dielectric layer 51 exposed (see Figure 5(c)).

Referring to Figure 5(d), the Photoresist 55 and at the least one portion 56 of the dielectric layer 51 are then removed by known etching techniques, eg wet or dry etching. In the case of wet etching Hydrofluoric (HF) acid may be employed.

20

Referring to Figure 5(e), the device body portion 5 is processed so as to create extended defects at least in a portion 53 of the device body portion 5. The step of processing the device body portion 5 comprises performing a plasma etch on the device body portion 5 using a sputterer 65 as will hereinafter be described in greater detail. This step may be referred to as a "pre-etch", and involves reversing the conventional electrical bias voltage configuration of the sputterer 65.

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Referring to Figure 5(f), a further dielectric layer 60 is then deposited on the
dielectric layer 51 and on the at least one portion 53 of the device body portion 5. The dielectric layer 51 and further dielectric layer 60 are deposited by use of the sputterer 65. In a modification the dielectric layer 51 and/or the further dielectric layer 60 may be deposited by a deposition technique other than by the use of a sputterer, eg Plasma Enhanced Chemical Vapour Disposition (PECVD).

Referring briefly to Figures 6 and 7, the dielectric layer 51 is deposited by sputtering, and in this embodiment the dielectric layer 51 is deposited by sputtering using a magnetron sputterer apparatus, generally designated 65. The dielectric layer 51 substantially comprises Silica (SiO₂), but may in a modification comprise another dielectric material such as Aluminium Oxide (Al₂O₃).

As can be seen from Figure 6, the sputterer apparatus 65 includes a chamber 70 which, in use, is substantially filled with an inert gas such as argon which is preferably provided within the chamber 70 at a pressure of around 2 microns of Hg. The sputterer 65 also comprises an RF source 75 connected to a target electrode 80 and to a substrate electrode 85 of the sputterer 65 respectively. A silica target 81 is provided on the target electrode 80, while the device body portion 5 (on wafer 82) is provided on the substrate electrode 85 of the sputterer 65. In use, an argon plasma (not shown) is generated between the target electrode 80 and substrate electrode 85 with first and second dark spaces being provided between the Silica target 81 and the argon plasma and between the argon plasma and the device body portion 5, respectively.

The step of processing the device body portion 5 so as to create extended defects at least in a portion of the device body portion 5 comprises part of a Quantum Well Intermixing (QWI) process used in the manufacture of the device 40, the QWI process comprising – in a preferred embodiment – an Impurity-Free Vacancy Disordering (IFVD) technique. It has been surprisingly found that by sputtering
from the device body portion 5 using the sputterer 65, damage induced extended defects appear to be introduced into the portion 53 of the device body portion 5; the portion 53 in this case comprising part of the cap layer 35. It is believed that the damage in the cap layer 35 prior to annealing (which will hereinafter be described), eg the application of thermal energy by rapid thermal annealing, inhibits transfer of Gallium from the portion 53 of the cap layer 35 into the further dielectric layer 60.

The dielectric layer 51 is preferably between 10 to 1000 nm, and typically 200 nm or 300 nm, in thickness. The method of manufacture includes a further step as shown in Figure 5(f) of depositing a further dielectric layer 60 on the surface 52 of device body 5 and on a surface of the dielectric layer 51 prior to annealing. The further dielectric layer 60 may be deposited by a technique other than sputtering, e.g. by Plasma Enhanced Chemical Vapour Deposition (PECVD).

The dielectric layer 51 therefore comprises an intermix cap layer, while the further dielectric layer 60 comprises an intermix suppressing cap layer. The intermix suppressing cap layer is used to protect the surface 52 from Arsenic desorption. The method will work without the intermix suppressing cap layer; however the quality of the surface 52 may not be so good.

As shown in Figure 5(g), subsequent to deposition of the further dielectric layer 60, the device body portion including the dielectric layer 51 and further dielectric layer 60 is annealed at an elevated temperature. The annealing stage comprises a rapid thermal annealing stage, the annealing temperature being between 700 and 1000°C, and more preferably between 800 and 1000°C, for between 0.5 to 5 minutes. In a preferred implementation, the rapid thermal anneal is approximately 900°C for approximately 1 minute.
The action of the annealing step of Figure 5(g) is illustrated diagrammatically in Figures 8(a) and (b). As can be seen from Figures 8(a) and (b), the annealing step causes "out diffusion" of Gallium from the cap layer 35 to the intermixing cap, ie dielectric layer 51. However, portions of the cap layer 35 below portion 53 and the suppressing cap, ie further dielectric layer 60, are subject to significantly less Gallium "out-diffusion". The portions of the cap layer 35 which lie within an area of the intermixing cap, ie dielectric cap 51, are subject to greater out-diffusion of Gallium as shown in Figure 8(b). The out-diffusion of Gallium leaves vacancies behind which migrate from the cap layer 35, through the second cladding layer 25, and into the core layer 20, and hence to the Quantum Well structure(s) 30, thereby changing the effective band-gap of the Quantum Well (QW) structure 30, and effectively washing-out the Quantum Wells of the Quantum Well structure 30 below the intermixing cap layer.

It will be appreciated that the intermixing cap, ie dielectric layer 51, is provided within the area of the passive region 50 to be formed in device 40, while the suppressing cap, ie further dielectric layer 60, is provided on the device body portion 5 in areas such as the optically active region 45 to be formed on the device 5, which areas are not to be Quantum Well Intermixed (QWI).

Once the device body portion 5 has been processed to the stage of Figure 5(g), and annealed, the dielectric layer 51 and further dielectric layer 60 may be removed by conventional methods, eg wet or dry etching.

It will be appreciated that in the step of processing the device body portion 5 so as to produce extended defects at least in a portion 53 of the device body portion 5, any sputtering apparatus may be employed. Particularly magnetron sputterers such as the magnetron sputterer 65 illustrated in Figures 6 and 7 can be used.
In magnetron sputterers it is attempted to trap electrons near the "target" so as to increase their ionising effect. This is achieved with electric and magnetic fields which are generally perpendicular. It will be appreciated that a number of magnetron sputterer configurations are known such as the cylindrical magnetron illustrated in Figure 9(a), the circular magnetron illustrated in Figure 9(b), or the planar magnetron illustrated in Figure 9(c). The various parts of the magnetron sputterer apparatus 65 a, b, c of Figures 9 a, b, c, respectively are identified by the same reference integers as the magnetron apparatus 65 of Figures 6 and 7.

It will be appreciated that in the step of Figure 5(b) the device body portion 5 comprises the substrate 82 of the sputtering apparatus 65 of Figures 6 and 7, while the silica target 81 is the target from which silica deposition occurs. This is also the case in the deposition stage of the further dielectric layer 60 of Figure 5(f). However, in the step of Figure 5(e) the bias voltages are reversed, and the wafer 82 in effect becomes the sputtering target from which sputtering occurs. This so-called "pre-etch" stage appears to introduce the extended defects into the portion 53 of the device body portion 5. Between the step Figure 5(e) and Figure 5(f), the bias voltages are again reversed.

**EXAMPLE**

There now follows an example which illustrates a typical band-gap shift which can be obtained using IFVD in a method of manufacturing an optoelectronic device according to the present invention in an aluminium alloy such as Aluminium Gallium Arsenide (AlGaAs), grown on a Gallium Arsenide (GaAs) substrate.

The sputter chamber 70 is configured as follows. A plate separation of the order of 70 to 100 mm between the target electrode and the substrate electrode is provided, preferably 70 mm. The electrode configuration is a 4 or 8 inch circular plate (preferably 8 inch). The gas used in the system is typically argon but other
gases may be used. Also a small amount of oxygen may be added to the plasma (approximately 10% by volume) to improve the stoichiometry when performing dielectric film deposition. The dielectric used for the process is typically SiO₂, but others such as Al₂O₃ can be used. The pressure used within the chamber 70 for both the pre-etch and the silica deposition process is around 2 microns of Hg.

The following table outlines the resulting shifts for samples with 200 nm of sputtered silica deposited on top of them. One sample had a 5 minute pre-etch at power level of 500 W. The figures in the Table detailing the shift are for an anneal at 900°C for 1 minute.

<table>
<thead>
<tr>
<th>Deposition conditions</th>
<th>Shift</th>
</tr>
</thead>
<tbody>
<tr>
<td>Only sputtered Silica</td>
<td>45 nm</td>
</tr>
<tr>
<td>Sputter-etched then encapsulated with sputtered silica</td>
<td>2 nm</td>
</tr>
</tbody>
</table>

Table 1 illustrates that performing a sputter etch on the device body portion prior to silica (SiO₂) encapsulation provides an improved intermix suppressing cap.

To process a wafer to produce more than one band gap a film of sputtered or PECVD silica is deposited on to the wafer. Photolithography techniques are then used to delineate a pattern on top the sputtered silica and either wet or dry etching can then be used to transfer the pattern into the sputtered silica.

The sample is then placed into the sputtering apparatus (rig) for pre-etching and a subsequent further sputtered silica deposition.

A rapid thermal anneal is now performed at a suitable temperature (700°C –
1000°C, and more preferably 800°C – 1000°C) for the required period of time (0.5 to 5 min). This enables the point defects generated at the surface in the magnetron silica to propagate through the structure and cause interdiffusion of the elements.

It will be appreciated that the embodiments of the invention hereinbefore described are given by way of example only, and are not meant to limit the scope thereof in any way.

It should be particularly understood that sputtered silica is suitable for performing the IFVD process in around 980 nm GaAs/AlGaAs material. Furthermore, using a combination of a sputter pre-etch and sputtering to deposit another silica layer, provides an effective QWI suppression layer.

It is believed that using the pre-etch causes high levels of damage and the occurrence of extended defects in the cap (top layer) layer of the epitaxial wafer. These extended defects effectively trap point defects and stop them from diffusing down to the QW, thus effectively stopping any intermixing of the QW. The damage arises from the bombardment of ions at the sample surface.

In the sputtering arrangement used for the process the substrate can be switched from being the anode / cathode of the system. Initially, the electrode on which the sample is located (the “substrate electrode”) is made negative and the positive ions in the plasma are accelerated to the surface thereof causing a high degree of damage to the cap layer, (ie the extended defects).

Further, it will be appreciated that using effectively the same type of silica for the whole process circumvents a problem of IFVD with dielectric caps, namely mismatch of the expansion of coefficients thereof. This allows the post anneal quality of the material to be kept to a high quality.
It will further be appreciated that an optical device according to the present invention may include a waveguide such as a ridge or buried heterostructure or indeed any other suitable waveguide.

It will also be appreciated that the Quantum Well Intermixed (QWI) regions may comprise optically active device(s).

Further, it will be appreciated that sequential processing including using several RF powers may be used to provide a device with several different QWI band-gaps.
CLAIMS

1. A method of manufacturing an optical device, a device body portion from which the device is to be made including a Quantum Well (QW) structure, the method including the step of processing the device body portion so as to create extended defects at least in a portion of the device body portion.

2. The method of claim 1 wherein said step of processing the device body portion comprises performing a plasma etch on the device body portion.

3. The method of claim 2 wherein in said step of performing a plasma etch on the device body portion comprises performing a sputter-etch on the device body portion.

4. The method of claim 3 wherein in said step of performing a sputter-etch comprises using a magnetron sputterer.

5. The method of claim 3 or claim 4 wherein in said step of performing a sputter-etching on the device body portion includes applying a reverse electrical bias across an electrode upon which the device body portion is provided so as to provide a pre-etch of the device body portion.

6. The method of any preceding claim, wherein the method includes the preceding step of depositing a dielectric layer on at least one other portion of the device body portion, which dielectric layer may therefore act as a mask in defining the at least one portion.

7. The method of claim 6 further including the subsequent step of depositing a further dielectric layer on the dielectric layer and/or on the at least one portion of the device body portion.
8. The method of claim 7 wherein the dielectric layer and/or the further dielectric layer are deposited by use of a sputterer.

9. The method of claim 7 wherein the dielectric layer and/or the further dielectric layer are deposited by a deposition technique other than by use of a sputterer.

10. The method of any of claims 7 to 9 wherein the dielectric layer and the further dielectric layer substantially comprise Silica or Aluminium Oxide.

11. The method of any of claims 3 to 5 or 8 to 10 wherein the sputterer includes a chamber which is substantially filled with an inert gas.

12. The method of any of claims 6 to 10 wherein the step of depositing the dielectric layer comprises part of a Quantum Well Intermixing (QWI) process used in manufacture of the device.

13. The method of claim 12 wherein the QWI process comprises Impurity-Free Vacancy Disordering.

14. The method of any preceding claim further including the step of annealing the device body portion at an elevated temperature.

15. The method any preceding claim further including the preceding steps of: providing a substrate; growing on the substrate:

   a first optical cladding layer;

   a core guiding layer including a Quantum Well structure; and
a second optical cladding layer.

16. The method claim 15 wherein the first optical cladding layer, core guiding layer, and second optical cladding layer are grown by a growth technique selected from Molecular Beam Epitaxy and Metal Organic Chemical Vapour Deposition.

17. The method of any of claims 6 to 10 further comprising the steps of:
depositing the dielectric layer on a surface of the device body portion; and
defining a pattern in photoresist on a surface of the dielectric layer and
lifting off at least part of the photoresist so as to provide the dielectric layer on said
at least one other portion of the device body portion.

18. The method of any of claims 7 to 10 wherein the method also includes the
step of depositing the further dielectric layer on a portion of the surface of the
device body and on a surface of the dielectric layer prior to annealing.

19. The method of any of claims 7 to 10 wherein the dielectric layer comprises
an intermixing cap; while the at least one portion of the device body portion and/or
the further dielectric layer comprises an intermixing suppressing cap.

20. The method of any of Claims 7 to 10 wherein the thickness of the dielectric
layer and the further dielectric layer is between 10 and 1000 nm.

21. The method of claim 14 wherein the annealing step occurs at a temperature
of between 800°C and 1000°C for between 0.5 and 5 minutes.

22. A method of manufacturing an optical device, a device body portion from
which the device is to be made including a Quantum Well (QW) structure, the
method including the step of performing a plasma etch on the device body portion.
23. The method of claim 22 wherein the step of performing a plasma etch on
the device body portion is carried out using a sputterer.

24. An optical device fabricated using the method of claim 1 or claim 22.

25. The optical device of claim 24 wherein the optical device is an integrated
optical device or an optoelectronic device.

26. The optical device of either of claims 24 or 25 wherein the device body
portion is fabricated in a III–V semiconductor materials system.

27. The optical device of claim 26 wherein the III–V semiconductor materials
system is a Gallium Arsenide based system adapted to operate at at least one
wavelength between 600 and 1300 nm.

28. The optical device of claim 26 wherein the III–V semiconductor materials
system is an Indium Phosphide based system adapted to operate at at least one
wavelength between 1200 and 1700 nm.

29. The optical device of any of claims 26 to 28, wherein the device body
portion is made at least partly from one or more of Aluminium Gallium Arsenide,
Indium Gallium Arsenide, Indium Gallium Arsenide Phosphide, Indium Gallium
Aluminium Arsenide and Indium Gallium Aluminium Phosphide.

30. The optical device of any of Claims 24 to 29 wherein the device body
portion comprises a substrate upon which are provided a first optical cladding
layer, a core guiding layer, and a second optical cladding layer.
31. The optical device of claim 30 wherein the Quantum Well (QW) structure is provided within the core guiding layer.

32. An optical integrated circuit, optoelectronic integrated circuit (OEIC), or photonic integrated circuit (PIC) including at least one optical device according to any of claims 24 to 31.

33. A device body portion when used in a method according to any of claims 1 to 22.

34. A wafer of material including at least one device body portion when used in a method according to any of claims 1 to 22.

35. The method of any of claims 1 to 23 in which the device body portion is formed from an InGaAs–InAlGaAs–InP system adapted to operate at at least one wavelength between 1450 and 1550 nm.

36. The method of any of claims 1 to 23 including the steps of forming the device body portion from a system comprising any one or more of the following layers: a substrate of InP; a first optical cladding layer of InP, a core guiding layer of InAlGaAs and/or InGaAsP; a quantum well of InGaAs; a second optical cladding layer of InP; and a cap of InGaAs.

37. A method of manufacturing an optical device as described herein with reference to the accompanying drawings.

38. An optical device as described herein with reference to the accompanying drawings.
Fig. 3

Fig. 4
Fig. 5(a)

1. As Grown

GaAs Cap
Upper Clad
Waveguide
Lower Clad

Fig. 5(b)

2. Magnatron Silica dep

Magnatron Silica

GaAs Cap
Upper Clad
Waveguide
Lower Clad
3. PR deposition and patterning

**Fig. 5(c)**

4. Lift off

**Fig. 5(d)**
Fig. 5(e)

Fig. 5(f)
6. RTA

Fig. 5(g)