Title: DAMASCENE STRUCTURE AND METHOD FOR FORMING A DAMASCENE STRUCTURE

Abstract: A damascene structure having a reduced overall dielectric constant and a method for forming such a structure is disclosed. In one embodiment, the present embodiment deposits a blanket coating (206, 306) of etch stop layer material over an underlying structure. In the present embodiment, the underlying structure includes a first region (202, 302) to which an interconnect will be subsequently be formed. Next, the present embodiment selectively removes portions of the blanket coating of the etch stop layer material. More specifically, in the present embodiment, the etch stop layer material is removed from above a second region (208, 304) of the underlying structure. In the present embodiment, the second region of the underlying structure will not subsequently have the interconnect formed thereto. In so doing, the present embodiment eliminates the presence of superfluous etch stop layer material. As a result, the overall dielectric constant of the intermetal filmstack is reduced as compared to conventional damascene structures.
DAMASCENE STRUCTURE AND METHOD FOR FORMING A DAMASCENE STRUCTURE

TECHNICAL FIELD

The present disclosure relates to the field of semiconductor devices. More specifically, the present disclosure relates to a damascene formed structure and methods for forming damascene structures. In particular, the use of patterned stop layers in a dual damascene structure to reduce the dielectric constant of the intermetal filmstack is disclosed.

BACKGROUND ART

Computer chip manufacturing processes typically include the formation of P-n junctions in a semiconductor substrate which are connected by polysilicon which is deposited, masked, and etched to form a patterned polysilicon surface. The patterned polysilicon surface connects with the p-n junctions so as to form numerous semiconductor devices on the semiconductor substrate. Typically, one or more layers of dielectric is then deposited over the surface of the semiconductor. The dielectric is then masked and etched to expose portions of the polysilicon surface through openings which are commonly referred to as vias. A layer of metal or "first metal" is then deposited over the surface of the semiconductor substrate. Typically aluminum is used since it is easy to deposit and form and since it has good conductivity. The metal overlies the layer of dielectric and fills the vias so as to form contacts or "plugs" that make contact between the metal layer and the polysilicon layer so as to allow for electrical contact between the first metal layer and the semiconductor devices. The first
metal layer is then masked and etched so as to form metal lines or "interconnects" which connect to the various semiconductor devices by the contacts. Alternate layers of dielectric and metal are then formed over the first metal layer.

As the complexity of computing devices and data storage devices has increased, there has been a need to place more semiconductor devices on each computer chip. This need has led to smaller and smaller devices and interconnects. However, as devices and interconnects have become smaller and smaller the process limitations of depositing and etching metal so as to form interconnects has imposed limitations on further size reductions in processing technology. This is primarily due to the limitations imposed by the etch process. These limitations make increasingly smaller interconnects difficult if not impossible to etch since the interconnects are extremely small, and since they must be spaced closely together. The inability to control the metal etch process with the needed degree of accuracy leads to non uniform interconnect width and depth. The non-uniform interconnect width and depth, in turn, leads to interference between interconnects and non uniform resistivity between interconnects of equal length. As devices get smaller and smaller, the inaccuracies in the depth and width of the metal layer interfere to an increasing degree with signal processing. Much of this interference is due to signal delay which creates timing problems and results in signal interference. In addition, the problems of non uniformity of metal etch processes decreases yield and throughput.
One recent process for obtaining the small metal lines and contacts needed for the .18 micrometer process generation and for subsequent smaller processing generations is the use of damascene processing techniques. In damascene processing techniques, the dielectric layer which is typically an oxide, commonly referred to as an intermetal dielectric (IMD) is deposited over the semiconductor surface. The oxide layer is polished so as to obtain a planar upper surface. A series of well-known process steps are then performed in order to form interconnects between various metal layers. The damascene process allows for the formation of small, closely spaced interconnects and contacts.

The success of damascene processes is primarily due to the fact that it is easier to etch oxides than it is to etch metal. Moreover, by using oxide etch processes, thinner structures and closer spacing between structures are possible than are possible using metal etch techniques. Another advantage of damascene processes is the ability to use copper as a material for interconnects and contacts. Since copper is hard to etch, it is seldom used in current wafer processing systems. However, copper may be deposited such that it fills the trenches and vias and it may be polished so as to obtain a damascene structure with copper interconnects and contacts.

However, as shown in Prior Art Figure 1, conventional damascene processes and structures are not without disadvantages. A conventional dual damascene structure 100 is shown in Prior Art Figure 1. In the embodiment of Prior Art Figure 1, the metal layers (M1 102, M2 104) are aluminum (Al) or copper (Cu). Additionally, the IMD 106 is preferably a
low-k (low dielectric constant) material, and the intervening stop layers 108 of silicon nitride, "nitride", are used as etch stop layers. Unfortunately, the dielectric constant of many conventional stop layer materials is greater than that of the low-k (< 3.5) dielectric typically used for the intermetal dielectric. As an example, nitride has a k value of about 7 as compared to silicon oxide ("oxide") which only has a k value of about 3.5. The presence of such conventional high dielectric stop layers increases the overall k value of the intermetal filmstack separating different metal layers (for example, between M1 102 and M2 104). This increased overall k value due to conventional, high k value, etch stop layer materials significantly reduces interconnect performance.

Thus, a need exists for a damascene formed structure and method wherein a high k value etch stop layer does not significantly increase the overall dielectric constant of the intermetal filmstack, and wherein the presence of a high k value etch stop layer material does not significantly reduce interconnect performance.
DISCLOSURE OF THE INVENTION

The present invention provides a damascene formed structure and method wherein a high k value etch stop layer does not significantly increase the overall dielectric constant of the intermetal filmstack, and wherein the presence of a high k value etch stop layer material does not significantly reduce interconnect performance.

In one embodiment of the present invention, the present embodiment deposits a blanket coating of etch stop layer material over an underlying structure. In the present embodiment, the underlying structure includes a first region to which an interconnect will be subsequently be formed. Next, the present embodiment selectively removes portions of the blanket coating of the etch stop layer material. More specifically, in the present embodiment, the etch stop layer material is removed from above a second region of the underlying structure. In the present embodiment, the second region of the underlying structure will not subsequently have the interconnect formed thereto. In so doing, the present embodiment eliminates the presence of superfluous etch stop layer material. As a result, the overall dielectric constant of the intermetal filmstack is reduced as compared to conventional damascene structures.

In another embodiment, the present invention over polishes a metal portion of a damascene structure in which a metal portion has a dielectric region adjacent thereto. In this embodiment, the over polishing of the metal portion causes the top surface of the metal portion to be recessed with respect to the top surface of the adjacent dielectric region. Next, the present embodiment, deposits a blanket coating of etch stop layer material
over the top surface of the metal portion and the top surface of the adjacent dielectric region. After the blanket deposition, the present embodiment selectively removes portions of the blanket coating of the etch stop layer material. More specifically, the present embodiment removes the etch stop layer material from above at least a portion of the top surface of the adjacent dielectric region. Moreover, the etch stop layer material remains above the top surface of the metal portion. As in the above-described embodiment, in so doing, the present embodiment eliminates the presence of superfluous etch stop layer material. As a result, the overall dielectric constant of the intermetal filmstack is reduced as compared to conventional damascene structures.

These and other advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.
BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

PRIOR ART FIGURE 1 is a cross-sectional view illustrating a prior art damascene structure.

FIGURES 2A-2F are cross-sectional views illustrating steps and structures associated with the formation of a damascene device in accordance with one embodiment of the present claimed invention.

FIGURES 3A-3B are cross-sectional views illustrating steps and structures associated with the formation of a damascene device in accordance with one embodiment of the present claimed invention.

FIGURE 4 is a flow chart of steps performed in accordance with one embodiment of the present claimed invention.

The drawings referred to in this description should be understood as not being drawn to scale except if specifically noted.
BEST MODE FOR CARRYING OUT THE INVENTION

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

With reference now to Figure 2A, a side sectional view of a damascene structure 200 being formed according to one embodiment of the present claimed invention is shown. As an overview, in the present invention, the etch stop layers are selectively patterned to leave the high k value etch stop layer material only where needed to act as an etch stop or barrier layer. In so doing, large portions of the relatively high dielectric etch stop layer material can be removed from the intermetal filmstack. As a result, the present invention lowers the overall dielectric constant of the intermetal filmstack. The processes and structure of the present invention are set forth in detail below.
With reference still to Figure 2A, a starting step in the formation of a damascene structure 200 is shown. In the present embodiment, copper, Cu, is used as the metal 202a and 202b; fluorinated silica glass (FSG) is used as the low-k intermetal dielectric 204; and nitride is used as the stop layer material for stop layer 206. Although such materials are recited in the present embodiment, the present invention is also well suited to the use of various other materials for the metal, the low-k intermetal dielectric, and/or the stop layer material. For example, in one embodiment, silicon carbide is used as the stop layer material.

Referring still to Figure 2A, in the present embodiment, a blanket coating of etch stop layer material is deposited over the underlying structure comprised of metal 202a and 202b and low-k intermetal dielectric 204. For purposes of the following discussion, metal 202a of the above-described underlying structure will have an interconnect subsequently formed thereto.

With reference next to Figure 2B, in the present embodiment, after the blanket deposition of stop layer material, the stop layer 206 is patterned using photolithography process steps to selectively remove portions of the blanket coating of the etch stop layer material. More specifically, stop layer 206 is patterned to remove the stop layer material from region 208. Additionally, in the embodiment of Figure 2B, the stop layer material is removed from above the areas adjacent to metal 202a and metal 202b. Hence, in the present embodiment, the stop layer material resides primarily over metal 202a and 202b where it may be needed as an etch stop or barrier layer. As a result, the present embodiment reduces the
amount of etch stop layer material disposed above the underlying structure. The reduction in the amount of etch stop material beneficially reduces the overall dielectric constant of the damascene filmstack.

Referring now to Figure 2C, after the selective removal of portions of the etch stop layer 206, the present embodiment deposits another layer 210 of the low-k intermetal dielectric material. In present embodiment, a blanket coating 212 of etch stop layer material is deposited over the underlying structure comprised of metal 202a and 202b, low-k intermetal dielectric 204, etch stop layer portions 206a and 206b, and low-k intermetal dielectric 210.

With reference next to Figure 2C, there are different choices on how to proceed from here depending on the particular dual damascene flow chosen (via-first, trench-first, or self-aligned). For purposes of the present application, a via-first flow process will be described. Although such a damascene flow is described herein, the present embodiment is also well suited to the use of the various other damascene flows. For the via-first process flow of the present embodiment, after the blanket deposition of the stop layer material (the intermediate layer), the stop layer 212 is patterned using photolithography process steps to selectively remove portions of the blanket coating of the etch stop layer material. More specifically, stop layer 212 is patterned to remove the stop layer material from region 213. Hence, in the present embodiment, the stop layer material resides primarily above metal 202a and 202b where it may be needed as an etch stop. As a result, the present embodiment reduces the amount of etch stop layer material disposed above the underlying structure. Once again, the
reduction in the amount of etch stop material beneficially reduces the overall dielectric constant of the damascene filmstack.

Referring now to Figure 2D, the present embodiment deposits another layer 214 of the low-k intermetal dielectric material. After the deposition, a photoresist layer 216 is formed and patterned, and is then used as a mask to etch a via 218 down to etch stop layer portion 206a.

With reference next to Figure 2E, photoresist 216 of Figure 2D is stripped and a new layer of photoresist (not shown) is deposited and patterned to act as a mask for the trench etch. The present embodiment then etches trenches 218 and 220. After the trench etch, the intermediate nitride layer 212a and 212b and bottom nitride layer 206a are exposed. The photoresist layer used as a mask for the trench etch is then stripped. Both nitride layers are then etched away with a single etch step, removing most of remaining nitride from the filmstack.

With reference next to Figure 2F, once the nitride layers are removed, barrier and Cu seed layers are then deposited, followed by Cu fill and Cu chemical mechanical polishing to form structures 222 and 224. Thus, the present embodiment allows for a beneficial reduction in the amount of the high dielectric constant stop layer remaining between the metal layers.

In one embodiment, generation of the additional masks required for etching of the stop-layer material is simplified by merely using M1 and M2 masks and biasing them to account for misalignment. Therefore, in such
an embodiment, the mask used to pattern the first nitride is the M1 mask with each linewidth = M1 linewidth +/- 200% of allowable misalignment. Additionally, in another embodiment, the mask for the second stop layer is the M1 mask with each linewidth = M1 linewidth +/- 200% of allowable misalignment.

Referring now to Figure 3A, in an alternate embodiment 300 of the present invention is shown. In this embodiment, the etch stop layer material is preferentially left over metal regions using an overpolishing process. Specifically, in one embodiment, copper, Cu, is used as the metal 302a and 302b; oxide is used as the low-k intermetal dielectric 304; and nitride is used as the stop layer material for stop layer 306. Although such materials are recited in the present embodiment, the present invention is also well suited to the use of various other materials for the metal, the low-k intermetal dielectric, and/or the stop layer material. For example, in one embodiment, silicon carbide is used as the stop layer material.

Referring still to Figure 3A, in the present embodiment, a blanket coating of etch stop layer material is deposited over the underlying structure comprised of metal 302a and 302b and low-k intermetal dielectric 304. The recess of the metal 302a and 302b below that of the adjacent dielectric layer 304 was obtained by a deliberate overpolish during a metal chemical-mechanical polishing (CMP) process. For purposes of the following discussion, metal 302a of the above-described underlying structure will have an interconnect subsequently formed thereto.
With reference next to Figure 3B, in the present embodiment, after the blanket deposition of stop layer material, the stop layer 306 is polished using a chemical mechanical polishing process. In so doing, the stop layer material resides primarily above metal 302a and 302b where it may be needed as an etch stop or barrier layer. The present embodiment then continues with the process flow shown in Figures 2C-2F. Hence, the present embodiment eliminates at least one of the masks for preferential removal of the nitride.

Referring now to Figure 4, a flow chart 400 of steps performed in the present invention is shown. As recited at step 402, and as described above in detail, the present embodiment deposits a blanket coating of etch stop layer material over an underlying structure. The underlying structure includes a first region to which an interconnect will be subsequently be formed.

Referring now to step 404, the present invention then selectively removes portions of the blanket coating of the etch stop layer material such that the etch stop layer material is removed from above a second region (e.g. region 208 of Figure 2B) of the underlying structure. The second region of said underlying structure will not subsequently have said interconnect formed thereto. As a result, the reduction in the amount of etch stop layer material beneficially reduces the overall dielectric constant of the damascene filmstack.

Thus, the present invention provides a damascene formed structure and method wherein a high k value etch stop layer does not significantly
increase the overall dielectric constant of the intermetal film stack, and
wherein the presence of a high k value etch stop layer material does not
significantly reduce interconnect performance.

The foregoing descriptions of specific embodiments of the present
invention have been presented for purposes of illustration and description.
They are not intended to be exhaustive or to limit the invention to the
precise forms disclosed, and obviously many modifications and variations
are possible in light of the above teaching. The embodiments were chosen
and described in order to best explain the principles of the invention and its
practical application, to thereby enable others skilled in the art to best
utilize the invention and various embodiments with various modifications
as are suited to the particular use contemplated. It is intended that the
scope of the invention be defined by the Claims appended hereto and their
equivalents.
CLAIMS:

1. A method for forming an etch stop layer in a damascene structure, wherein the
   damascene structure has a reduced overall dielectric constant, said method comprising the
   steps of:

   a) depositing a blanket coating of etch stop layer material over an underlying
      structure, said underlying structure including a first region to which an interconnect will be
      subsequently be formed; and

   b) selectively removing portions of said blanket coating of said etch stop layer
      material such that said etch stop layer material is removed from above a second region of said
      underlying structure wherein said second region of said underlying structure will not
      subsequently have said interconnect formed thereto.

2. The method for forming an etch stop layer in a damascene structure as recited in
   Claim 1 wherein said etch stop layer material is comprised of nitride.

3. The method for forming an etch stop layer in a damascene structure as recited in
   Claim 1 wherein said etch stop layer material is comprised of silicon carbide.

4. The method for forming an etch stop layer in a damascene structure as recited in
   any one of Claims 1-3 wherein step b) comprises:

   using photolithography and etch process steps to selectively remove said portions of
   said blanket coating of said etch stop layer material.
5. A method for forming an etch stop layer in a damascene structure, wherein the damascene structure has a reduced overall dielectric constant, said method comprising the steps of:

   a) over polishing a metal portion of a damascene structure in which said metal portion has a dielectric region adjacent thereto, said over polishing of said metal portion causing a top surface of said metal portion to be recessed with respect to a top surface of said adjacent dielectric region;

   b) depositing a blanket coating of etch stop layer material over said top surface of said metal portion and said top surface of said adjacent dielectric region; and

   c) selectively polishing portions of said blanket coating of said etch stop layer material such that said etch stop layer material is removed from above at least a portion of said top surface of said adjacent dielectric region and remains above said top surface of said metal portion.

6. The method for forming an etch stop layer in a damascene structure as recited in Claim 5 wherein said etch stop layer material is comprised of nitride.

7. The method for forming an etch stop layer in a damascene structure as recited in Claim 5 wherein said etch stop layer material is comprised of silicon carbide.

8. The method for forming an etch stop layer in a damascene structure as recited in any one of Claims 5-7 wherein step a) comprises:

   using a chemical mechanical polishing process to over polish said metal portion of said damascene structure.
9. The method for forming an etch stop layer in a damascene structure as recited in any one of Claims 5-8 wherein step c) comprises:
   using a chemical mechanical polishing process to over selectively remove said portions of said blanket coating of said etch stop layer material.

10. The method as recited in any one of Claims 1-4 further comprising the steps of:
   c) depositing a layer of intermetal dielectric material above said underlying structure and said remaining portions of said etch stop layer material;

   d) depositing a second blanket coating of etch stop layer material above said layer of intermetal dielectric material; and

   e) selectively removing portions of said second blanket coating of said etch stop layer material such that said etch stop layer material is removed from above said second region of said underlying structure.

11. The method for forming an etch stop layer in a damascene structure as recited in Claim 10 wherein said etch stop layer material of said second blanket coating is comprised of nitride.

12. The method for forming an etch stop layer in a damascene structure as recited in Claim 10 wherein said etch stop layer material of said second blanket coating is comprised of silicon carbide.

13. The method for forming an etch stop layer in a damascene structure as recited in
any one of Claims 10-12 wherein step e) comprises:

using photolithography and etch process steps to selectively remove said portions of said second blanket coating of said etch stop layer material.

14. A damascene structure having a reduced overall dielectric constant, said damascene structure comprising:

a) an underlying structure including a first region to which an interconnect will be subsequently formed; and

b) an etch stop layer selectively disposed above said underlying structure such that said etch stop layer is not disposed above a second region of said underlying structure wherein said second region of said underlying structure will not subsequently have said interconnect formed thereto.

15. The damascene structure having a reduced overall dielectric constant of Claim 14 wherein said etch stop layer material is comprised of nitride.

16. The damascene structure having a reduced overall dielectric constant of Claim 14 wherein said etch stop layer material is comprised of silicon carbide.
Fig. 1
(Prior Art+)
Fig. 3A

Fig. 3B
Fig. 4
### INTERNATIONAL SEARCH REPORT

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC 7  H01L21/768  H01L23/522

According to international Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 7  H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO–Internal, PAJ, WPI Data, IBM–TDB

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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<th>Relevant to claim No.</th>
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<td>US 5 763 953 A (IIJIMA TADASHI ET AL) 9 June 1998 (1998–06–09) column 7, line 56 -column 8, line 51 column 10, line 16 -column 11, line 11 column 16, line 43 -column 17, line 19; figures 5A-D,17,33A-D</td>
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Further documents are listed in the continuation of box C. Patent family members are listed in annex.

* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
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Date of the actual completion of the international search

30 May 2001

Date of mailing of the international search report

07/06/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Lijnden
Tel. (+31–70) 940-2040, Tx. 31 651 epo nl, Fax (+31–70) 940-3016

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