A high voltage solid-state switch, which provides bidirectional blocking, consists of a first p-type semiconductor body (16) separated from a support member (semiconductor substrate) by a dielectric layer (14) with a p-type anode region (18) located at one end of the semiconductor body, an n-type cathode region (24) located at the other end, and an n-type gate region (20) located between the anode and cathode regions. The switch is capable of switching to an 'OFF' (blocking) state placing the gate region at the anode voltage. The carrier concentration of the bulk portion of the semiconductor body is 2 \times 10^{12} to 2 \times 10^{13} impurities/cm^2. A resistive path (R1) may connect anode and cathode regions. Unique control circuitry is disclosed.
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This invention relates to a structure comprising a semiconductor body whose bulk is of one conductivity type and which has a major surface; a localized first region which is of the one conductivity type; a localized second region which is of the opposite conductivity type; the localized first and second regions being of relatively low resistivity as compared to the bulk of the semiconductor body and separated by a portion of the bulk of the semiconductor body; each of the first and second regions having a portion that forms part of the major surface and having separate electrode coupled thereto; a third region of the opposite conductivity type which is in contact with the semiconductor body and has a separate electrode coupled thereto; the structure being adapted to selectively facilitate current flow between the first and second regions or to divert a sufficient portion of said current into the third region so as to substantially interrupt (cut off) said current flow between the first and second regions; and the third region being separated from the first and second regions by a portion of the bulk of the semiconductor body.

The paper "A 500V Monolithic Bidirectional 2 x 2 Cross Point Array," 1980 ISSCC Digest of Technical Papers, February, 1980, p. 170 describes a high voltage integrated circuit employing a device known as the gated diode switch (GDS), which, because of its high voltage and current handling capability, may be used as a replacement for electromechanical switches, particularly in telephone systems. The GDS comprises anode, cathode and gate regions each included within a dielectrically isolated, lightly doped semiconductor tub. Current between the cathode and anode is switched to the OFF condition by applying an appropriate voltage to the gate which is higher than the anode voltage. This depletes the bulk semiconductor of
current carriers between the anode and cathode to cut off conduction.

One problem in the design of the switch is the need for a high voltage on the gate to switch the device off. Also, it would be desirable to provide a switch of this type which has a faster response time. Another problem is that rather complicated control circuits are required for applying the proper gate potential to switch the device.

In accordance with the invention these problems are overcome in a structure of the type described above characterized in that the characteristics of the bulk portion of the semiconductor body are selected such that, with the first and third regions held at approximately the same potential, current flow between the first and second regions is substantially inhibited or interrupted, and with the potential of the third region floating or lower than that of the first region, significant current can flow between the first and second regions.

In the drawing:

FIG. 1 is a schematic view of a gated diode switch in accordance with one embodiment of the invention;
FIG. 2 is a schematic top view of a gated diode switch in accordance with another embodiment of the invention;
FIG. 3 is a schematic illustration of a gated diode control circuit in accordance with the invention; and
FIG. 4 is a schematic illustration of a gated diode control circuit in accordance with another embodiment of the invention.

Referring now to FIG. 1, there is illustrated a structure 10 comprising a support member 12 having a major surface 11 and a semiconductor body 16 whose bulk is of one conductivity type and which is separated from support member 12 by an insulator layer 14, which is typically a dielectric layer. The semiconductor body 16 has a portion that is common with surface 11.
A localized first anode region 18, which is of the one type conductivity, is included in body 16 and has a portion thereof that extends to surface 11. A localized second gate region 20, which is of the opposite conductivity, also is included in body 16 and has a portion thereof which extends to surface 11. A localized third cathode region 24, which is of the opposite type conductivity, is included in body 16 and has a portion which extends to surface 11. A region 22, which is of the one type conductivity and has a portion which extends to surface 11, surrounds region 24 and acts as a depletion layer punch-through shield. Region 22 separates cathode region 24 from the bulk portion of semiconductor body 16. In addition it acts to inhibit inversion of the portions of body 16 at or near surface 11 between regions 20 and 24. It also acts to increase the voltage blocking capability between gate region 20 and cathode region 24. Gate region 20 is located between anode region 18 and region 22 and is separated from both by bulk portions of body 16.

The resistivities of regions 18, 20, and 24 are low compared to that of the bulk portions of body 16. The resistivity of region 22 is intermediate between that of anode region 18 and that of the bulk portions of body 16.

Electrodes 28, 30, and 32 are conductors which make low resistance contact to the surface portions of regions 18, 20, and 24, respectively. A dielectric layer 26 covers major surface 11 so as to isolate electrodes 28, 30, and 32 from all regions other than those intended to be electrically contacted. An electrode 36 provides a low resistance contact to support 12 by way of a highly doped region 34 which is of the same conductivity type as support 12.

Advantageously, the support 12 and the body 16 are each of silicon and the support 12 may be either of n or p type conductivity. Each of electrodes 28, 30, and 32 advantageously overlaps the semiconductor region to which they make low resistance contact. Electrode 32 also
overlaps region 22. This overlapping, which is known as field plating, facilitates high voltage operation because it increases the voltage at which breakdown occurs.

In one illustrative embodiment, substrate 12 and body 16 and regions 18, 20, 22, 24, and 34 are of n-, p-, p+, n+, p, n+, and n+ type conductivity, respectively. Dielectric layer 14 is silicon dioxide and electrodes 28, 30, 32, and 36 are all aluminum.

A plurality of separate bodies 16 can be formed in a common support 12 to provide a plurality of switches.

Structure 10 is typically operated as a switch having a low impedance path between anode region 18 and cathode region 24 when in the ON state and a high impedance between said two regions when in the OFF (blocking) state.

The type of structure described herein is denoted as gated diode switch (GDS). Substrate 12 is typically held at the most positive potential level available when body 16 is of p- type conductivity. It is held at the most negative potential level available when body 16 is of n- type conductivity. With operating potentials applied to the regions 18 and 24, the potential applied to gate region 20 determines the state of the switch. Regions 18 and 24 serve as the anode and cathode regions, respectively, when semiconductor body 16 is of p- type conductivity.

Regions 19 and 24 serve as the cathode and anode regions, respectively, when semiconductor body 16 is of n- type conductivity.

With body 16 being of p- type conductivity, conduction between anode region 18 and cathode region 24 is inhibited or interrupted (cut off) if the potential of gate region 20 is sufficiently positive. The amount of positive potential needed to inhibit or interrupt (cut off) conduction is a function of the geometry and impurity concentration (doping) levels of structure 10. This positive gate potential causes a vertical cross-sectional portion of body 16 between gate region 20 and the portion of dielectric layer 14 therebelow to be depleted and the
potential of this portion of body 16 to be greater in magnitude than that of anode region 18, cathode region 24, and region 22. This essentially pinches off body 16 against dielectric layer 14 in the bulk portion thereof below gate region 20 and extending down to dielectric layer 14. The positive potential barrier of the aforesaid portion of body 16 is a potential which inhibits conduction of holes from anode region 18 to cathode region 24. If conduction exists between anode region 18 and cathode region 24 before the potential of the gate region 20 is raised to the high potential level, then gate region 20 serves to collect electrons emitted at cathode region 24 before they can reach anode region 18. This serves to help interrupt conduction between anode region 18 and cathode region 24. In addition, the high level potential of gate region 20 serves to cause a vertical cross-sectional portion of body 16 between gate region 20 and the portion of dielectric layer 14 therebelow to be depleted of current carriers. The blocking (essentially nonconducting) state, is the OFF state.

The voltage applied to semiconductor support 12 causes an electric field which extends through dielectric layer 14 and into semiconductor body 16. Normally, during the ON state, electrons coat the bottom of semiconductor body 16 and act to shield it from the effect of the positive bias applied to substrate 12. With structure 10 biased to the OFF state, these electrons are removed from the bottom of semiconductor body 16 and drawn into gate region 20. The biased substrate 12 thus acts as a second or back gate which aids in switching structure 10 to the OFF state.

With semiconductor body 16 being of p-type conductivity, conduction from anode region 18 to cathode region 24 occurs if region 18 is forward-biased with respect to region 24 and the potential of gate region 20 is below a level which inhibits or interrupts conduction between anode region 18 and cathode region 24. During the
ON state holes are injected into body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. These holes and electrons can be in sufficient numbers to form a plasma which conductivity modulates body 16. This effectively lowers the resistance of body 16 such that the resistance between anode region 18 and cathode region 24 is low when structure 10 is operating in the ON state. This type of operation is denoted as dual carrier injection. Positively biased substrate 12 creates an electrical field which passes through the dielectric layer 14 and tends to deplete the bulk portion of body 16. Electrons emitted from cathode region 24 coat the bottom of body 16 and thus act to shield the effect of the electrical field created by biased substrate 12. These electrons invert the bottom of the bulk portion of body 16 which is adjacent dielectric layer 14. This limits the effect of biased substrate 12 and thus allows conduction between anode region 18 and cathode region 24 in the ON state.

Region 22 helps limit the punch-through of a depletion layer formed during operation between gate region 20 and cathode region 24 and helps inhibit formation of a surface inversion layer between these two regions. In addition, it permits gate region 20 and cathode region 24 to be relatively closely spaced. This facilitates relatively low resistance between anode region 18 and cathode region 24 during the ON state. It also serves to increase maximum operating voltage and to reduce leakage currents.

During the ON state of structure 10, the junction diode comprising semiconductor body 16 and gate region 20 can become forward-biased. Current limiting means (not illustrated) are normally included to limit the conduction through the forward-biased diode.

The ON state can be achieved by having the potential of the anode region 18 greater than that of the cathode region 24 and forward-biasing the anode region 18 with respect to the gate region 20. Typically,
1-10 microamperes are extracted from the gate region 20 while the anode-gate junction is forward-biased to cause structure 10 to assume the ON state.

It is possible to operate structure 10 in the ON state with the potential of gate region 20 at the same or a more positive level than that of anode region 18, cathode region 24, and region 22, so long as the potential of gate region 20 is below a level which essentially completely depletes a vertical cross-sectional portion of semiconductor body 16 between anode region 18 and cathode region 24. With the gate region 20 held at such a potential level, the junction diode comprising semiconductor body 16 and gate region 20 has a zero forward bias or is reverse-biased.

It has been discovered that decreasing the impurity concentration of the bulk portion of semiconductor body 16 of structure 10 of FIG. 1 causes a modification in the mode of operation. Starting with known design parameters, but with the impurity concentration of the bulk of semiconductor body 16 at approximately $1 \times 10^{13}$ instead of a conventional quantity such as $9 \times 10^{13}$ impurities/cm$^3$, it has been found that with the gate region 20 at approximately the same voltage as anode region 18, conduction between anode region 18 and cathode region 24 is inhibited or interrupted (cut off) except for a relatively low level flow. This is the OFF (high impedance) state. With a positive bias applied to anode region 18 relative to cathode region 24, and with gate region 20 allowed to essentially electrically float in potential, substantial current can flow between anode region 18 and cathode region 24. This is the ON (low impedance) state. The relatively low level current flow of the OFF state helps in switching structure 10 to the ON state.

One major advantage of structure 10, which has a semiconductor body 16 whose impurity concentration is as described immediately hereinabove, is that the gate potential need only be at that of the anode potential to
switch the structure to the OFF state. It is thus not necessary to use a higher potential than exists at the anode in order to operate structure 10, which considerably simplifies power supply problems and circuit design. Many applications require high voltage and high current switches but the most positive potential available is that applied to one of the terminals of the switch.

Referring now to FIG. 2, there is illustrated a top view of a structure 10z which is very similar to structure 10 of FIG. 1 and all components thereof which are essentially identical or similar to structure 10 are denoted with the same reference number with the addition of an "z". The basic difference between structures 10z and 10 is the inclusion of a resistive-type region R1 in structure 10z which couples anode region 18z to shield region 22z. The inclusion of region R1 gives a dependably high turn-on speed and allows for a considerably wider variation in the impurity concentration of semiconductor region 15z than is possible if R1 is not utilized. R1 serves to provide a predictable high impedance path between anode region 18z and shield region 22z during the OFF state. Variations in the impurity concentration of semiconductor body 16z thus become less critical since a high impedance path is established between anode region 18z and shield region 22z and this path exists relatively independently of the impurity concentration of semiconductor body 16z. Typically, the impurity concentration of semiconductor body 16z is between $2 \times 10^{12}$ impurities/cm$^3$ and $2 \times 10^{13}$ impurities/cm$^3$. R1 can be ion implanted or diffused into semiconductor body 16z. A discrete resistor could be connected between anode electrode 28z and region 22z, provided an electrode (not illustrated) is provided which is in contact with region 22z. This resistor would serve essentially the same purpose as R1; that is, it would conduct a small current during the OFF state to increase switching speed when the device is turned ON. In a preferred embodiment, R1 is an ion implanted pinch type
resistor, of the same conductivity type as regions 13z and 22z and is ion implanted with a dose of $10^{11} - 10^{13}$ impurities/cm$^2$. Region 22z can be eliminated in some application, in which case R1 is extended so as to contact cathode region 24z.

Support member 12 may be an n type monocristalline silicon substrate, 18 to 22 mils (1 mil = 0.00254 mm) thick, with an impurity concentration of approximately $1 \times 10^{13}$ impurities/cm$^3$. Dielectric layer 14 is a silicon dioxide layer that is 2 to 4 microns thick. Body 16 is typically 35 to 65 microns thick, approximately 430 microns long, 300 microns wide, and is of p type conductivity with an impurity concentration in the range of approximately 5-9 $\times 10^{13}$ impurities/cm$^3$. Anode region 18 is of p+ type conductivity, is typically 2 to 4 microns thick, 44 microns wide, 52 microns long, and has an impurity concentration of approximately $10^{19}$ impurities/cm$^3$. Electrode 28 is typically aluminum, with a thickness of 1 1/4 microns, a width of 84 microns, and a length of 105 microns. Region 20 is of n+ type conductivity and is typically 2 to 30 microns thick, 15 microns wide, 300 microns long, and has an impurity concentration of approximately $10^{19}$ impurities/cm$^3$. The depth of region 20 is determined by the thickness of body 16. Electrode 30 is aluminum, 1 1/4 microns thick, 50 microns wide, and 210 microns long. The spacing between adjacent edges of electrodes 28 and 30 and between adjacent edges of electrodes 30 and 32 is typically 40 microns in both cases. Region 22 is p type conductivity and is typically 3-6 microns thick, 64 microns wide, 50 microns long, and has an impurity concentration of approximately $10^{17}$ to $5 \times 10^{18}$ impurities/cm$^3$. Cathode region 24 is n+ type conductivity and is typically 2-4 microns thick, 48 microns wide, 44 microns long, and has an impurity concentration of approximately $10^{19}$ impurities/cm$^3$. Electrode 32 is aluminum, 1 1/4 microns thick, 104 microns wide, and 104 microns long. The spacing
between the ends of regions 18 and 22 and the respective ends of region 16 is typically 55 microns. Region 34 is n+ type conductivity and is typically 2 microns thick, 26 microns wide, 26 microns long, and has an impurity concentration of $10^{19}$ impurities/cm$^3$. Electrode 36 is aluminum which is 1 1/4 microns thick, 26 microns wide, and 26 microns long. Insulating (dielectric) layer 26 is typically 3-5 microns thick. Resistor R1 may be 10-30 microns wide, 200-300 microns long with a sheet resistance of 2-200 kilohms per square, a resistance of 40 kilohms to 4 meegohms, a junction depth of 5-6 microns and a pinch-off current of .1 microamp to 10 microamps.

Structure 10, using the parameters denoted above, may be operated as a gated diode switch (GDS) with 500 volts between anode and cathode. A layer of silicon nitride (not illustrated) may be deposited by chemical vapor deposition on top of silicon dioxide layer 26 to provide a sodium barrier. Electrodes 28, 30, 32, and 36 may then be formed and thereafter a coating of radio frequency plasma deposited silicon nitride (not illustrated) applied to the entire surface of structure 10 except where electrical contact is made. The layers of silicon nitride serve to help prevent high voltage breakdown in the air between adjacent electrodes.

Typically the anode has +250 volts applied thereto, the cathode -250 volts applied thereto, and substrate 12 has +250 volts applied thereto. The -250 volts can also be applied to the anode and the +250 volts applied to the cathode without damage to structure 10. The anode and cathode remain essentially electrically isolated from each other and there is little or no current flow between anode and cathode. Thus, structure 10 bilaterally blocks voltage between anode and cathode. A potential of +250 volts applied to gate electrode 30 will interrupt or break 350 mA of current flow between anode region 18 and cathode region 24. When the potential of the gate electrode 30 is switched from the
anode voltage to essentially one junction voltage drop below the potential of the anode, the GDS switches from the OFF state to the ON state. The ON resistance of the GDS with 100 mA flowing between anode and cathode is approximately 15 ohms and the voltage drop between anode and cathode is typically 2.2 volts.

From the foregoing it can be appreciated that a GDS made in accordance with the invention will simplify the problems of providing appropriate power supplies.

Switching can be made at a relatively high speed. The advantages of simplified control circuitry are illustrated in FIG. 3 which shows how a low power light source can be used in a simple manner to control a GDS so as to switch relatively high voltages and currents.

Referring now to FIG. 3, there is illustrated control circuitry 40a (illustrated within the larger dashed line rectangle) which is coupled to a high voltage and current switch GDS1 which has anode, cathode, and gate terminals 40g, 40e, and 40f, respectively. GDS1 is assumed to be a switch of the type illustrated in FIG. 1 with the impurity concentration of semiconductor body 16 being selected such that GDS1 can be switched to an off (high impedance) state by coupling the gate terminal thereof to a potential whose magnitude is close to that applied to the anode. Control circuitry 40a comprises a photodiode D4, a diode D5, and a high voltage current switch GDS2 which is of the same type as GDS1. D4 is illustrated within dashed line rectangle 40b and may be denoted as a voltage control branch circuit or simply as a branch circuit. The anode of D4 is coupled to the gate of GDS2 and to a terminal 40c. The cathode of D4 is coupled to the anodes of GDS2 and D5, and to a terminal 40d. The cathode of D5 is coupled to the anode of GDS1 and to terminal 40g. The cathode of GDS2 is coupled to the gate of GDS1 and to terminal 40f.

Control circuitry 40a is adapted to selectively set the potential of the terminal 40f (the gate of GDS1) to a value close to that of the anode of GDS1 (terminal 40g)
or to allow terminal 40f to essentially electrically float in potential. Assume a positive potential of sufficient magnitude to forward bias D5 and GDS1 is applied to terminal 10d with respect to terminal 40e. If terminal 40f electrically floats in potential, then GDS1 is ON and conduction will occur between terminals 40d and 40e.

Photodiode D4 acts as a battery when light is incident thereon. As such it sets the potential of terminal 40c (the gate of GDS2) at approximately +0.7 V above that of terminal 40d. This sets GDS2 to an OFF state and thus isolates terminal 40f from terminal 40d by the high impedance of the anode-cathode of GDS2. Thus terminal 40f of GDS1 essentially electrically floats in potential. This sets GDS1 to an ON state and conduction occurs between terminals 40d and 40e.

D4 acts to isolate terminals 40d and 40c when there is no light incident thereon since the "dark" resistance of D4 is large. The gate of GDS2 (terminal 40c) electrically floats in potential and thereby sets GDS2 to an ON state. Any positive potential applied to terminal 40d is thus applied through the relatively low ON impedance of GDS2 to terminal 40f. Accordingly, terminal 40f assumes a potential of approximately one diode voltage drop (the voltage across the anode-cathode of GDS2) below that of terminal 40d. The potential of the anode of GDS1 (terminal 40g) is likewise one diode voltage (the voltage across D5) below terminal 40d. Since the anode and gate terminals of GDS1 are essentially at the same potential, GDS1 is switched to an OFF state. This leaves terminals 40d and 40e separated by the relatively high impedance of switched OFF GDS1.

Now referring to FIG. 4, there is illustrated control circuitry 40a0 (illustrated within the larger dashed line rectangle) which is coupled to a high voltage and current switch GDS10 which has anode, cathode, and gate terminals 40g0, 40e0, and 40f0, respectively. Control circuitry 40a0 is very similar to control circuitry 40a.
FIG. 3 and all components and terminals which are similar or identical have reference numerals which are the same as the reference numerals of the corresponding components and terminals of FIG. 3 with an added "0" at the end. The basic difference between control circuitry 40a0 and 40a is the inclusion of a diode D6, a capacitor circuit means C2 (typically referred to as a capacitor), and a current limiter circuit CL4. The anode of D6 is coupled to the anode of D40, a first terminal of C2, and to a terminal 40h. The cathode of D6 is coupled to terminal 40c0 and to the gate terminal of GDS20. A second terminal of C2 is coupled to terminal 40f0 and to CL4. CL4 is also coupled to the cathode of GDS10 and to terminal 40e0.

Without D6 reverse current can flow from terminal 40e0, through the cathode-gate terminals of GDS10 and GDS20, and then through D40 and into terminal 40d0. D6 serves to block this electrical path such that the combination of GDS10 and control circuitry 40a0 selectively blocks the flow of substantial current from terminal 40d0 to 40e0 or vice versa.

CL4 is typically a pinch resistor which bleeds off the low current through GDS20 which exists when GDS20 is in an OFF state. With light incident upon D40, GDS20 is in an OFF state. The low level of current passing through the anode-cathode of GDS20 could raise the potential of terminal 40f0 sufficiently to cause GDS10 to be maintained in the OFF state. CL4 serves to effectively lower the potential of terminal 40f0 such that GDS10 is switched to the ON state when light is incident upon D40.

C2 is used to decrease sensitivity to voltage transients that may appear at terminal 40d0. A positive going voltage pulse applied to terminal 40d0 is transmitted through the parasitic capacitance (not illustrated) of D40 and through D6 and the parasitic capacitance (not illustrated) thereof. This increases the potential of the gate (terminal 40c0) of GDS20 and can turn off GDS20 and thus allow GDS10 to turn ON and conduct substantial current.
even though it is supposed to be OFF since there is no illumination on D40. C2 acts to limit the magnitude of the voltage transient and to dissipate the resulting current flow relatively rapidly. The parasitic capacitance (not illustrated) of the gate-cathode junction of GDS20 can be increased relative to the parasitic capacitance of D4 to effect the same result as C2. Alternately, the parasitic capacitance of D40 can be decreased relative to that of the parasitic capacitance of the gate-cathode junction of GDS20 to effect the same result. In both cases C2 can be eliminated.

The combination of GDS10 and control circuitry 40a0 functions as a unidirectional relay which is controlled by a light signal. Two of such configurations can be coupled together with terminals 40d0 and 40e0, and 40f0 of the first coupled to terminals 40e0, 40d0, and 40f0, respectively, of the second. This results in a bidirectional relay which is controlled by light signals.

The invention may be used in conjunction with many embodiments of the gated diode switch other than those shown. For example, the invention may be used in conjunction with any of the gated diode switch embodiments described in the PCT application of Western Electric Co., International Publication No. WO 80/01337, 26 June 1980.
Claims

1. A switching device comprising a semiconductor body (16) whose bulk is of one conductivity type and which has a major surface; a localized first region (18) which is of the one conductivity type; a localized second region (24) which is of the opposite conductivity type; the localized first and second regions being of relatively low resistivity as compared to the bulk of the semiconductor body and separated by a portion of the bulk of the semiconductor body; each of the first and second regions having a portion that forms part of the major surface and having separate electrode coupled thereto; a third region (20) of the opposite conductivity type which is in contact with the semiconductor body and has a separate electrode coupled thereto; the structure being adapted to selectively facilitate current flow between the first and second regions or to divert a sufficient portion of said current into the third region so as to substantially interrupt (cut off) said current flow between the first and second regions; and the third region being separated from the first and second regions by a portion of the bulk of the semiconductor body;

CHARACTERIZED IN THAT

the characteristics of the bulk portion of the semiconductor body are selected such that, with the first and third regions held at approximately the same potential, current flow between the first and second regions is substantially inhibited or interrupted and with the potential of the third region floating or lower than that of the first region, significant current can flow between the first and second regions.

2. The device of claim 1

FURTHER CHARACTERIZED IN THAT

the bulk portion of the semiconductor body has an impurity concentration of $2 \times 10^{12}$ to $2 \times 10^{13}$ impurities/cm$^3$. 

3. The device of claim 1
FURTHER CHARACTERIZED IN THAT
a resistive path (R1) interconnects the first and
second regions.

4. The structure of claim 3
FURTHER CHARACTERIZED IN THAT
the resistive path has a resistance 40 kilohms to
4 megaohms.

5. The device of claim 4
FURTHER CHARACTERIZED IN THAT
the resistive path is a path ion implanted on the
surface of the bulk portion with a pinch-off current of
.1 microamp to 10 microamps.

6. The device of claim 1
FURTHER CHARACTERIZED IN THAT
an output terminal (40f) of a gated diode switch
(GDS2) is connected to the third region (20) and a branch
circuit (40b) controls conduction in the gated diode
switch.

7. The circuitry of claim 6
FURTHER CHARACTERIZED BY
the first diode (D5) having a first terminal
coupled to a first output terminal (40g) of the gated diode
switch and having a second terminal coupled to a first
output terminal of the switching device.

8. The circuitry of claim 7
FURTHER CHARACTERIZED IN THAT
the branch circuit comprises a second diode D4
which is a photo-diode and which has a first terminal
coupled to the control terminal of the gated diode switch
and which has a second terminal coupled to an output
terminal of the switching device and to a terminal of the
first diode (D5).

9. The circuitry of claim 8
FURTHER CHARACTERIZED IN THAT
a third diode D6 has an anode terminal coupled to
the anode terminal of the second diode (D40) and a cathode
terminal coupled to the control terminal of the gated diode switch (GDS20).
INTERNATIONAL SEARCH REPORT

International Application No. PCT/US82/00364

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols are given, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

US CL. 357/21, 30, 37, 38, 39, 49, 51, 55
INT. CL. H01L 29/74, 27/14,
29/747, 27/12, 27/02, 29/06

II. FIELDS SEARCHED

Minimum Documentation Searched

Classification System

U.S.

Classification Symbols

357/21, 30, 37, 38, 39, 49, 51, 55
307/252.(A,B,C,T)

Documentation Searched other than Minimum Documentation

to the extent that such documents are included in the fields searched

III. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>U S, A, 3,870,904, Published 11 March 1975, SCLOCK</td>
<td>1-9</td>
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<tr>
<td>A</td>
<td>U S, A, 4,016,433, Published 5 April 1977, BROOKS</td>
<td>1-9</td>
</tr>
</tbody>
</table>

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"A" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search 2

30 JUNE 1982

Date of Mailing of this International Search Report 3

14 JUL 1982

International Searching Authority 1

ISA/US

Signature of Authorized Officer 9

G. Stotevich

Form PCT/ISA/210 (second sheet) (October 1981)
FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

* H03K 3/35, 17/72

V. OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. Claim numbers ........., because they relate to subject matter not required to be searched by this Authority, namely:

2. Claim numbers ..........., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

VI. OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

This International Searching Authority found multiple inventions in this international application as follows:

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.