MULTI-CHARACTER ELECTRONIC DISPLAY

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ABSTRACT

Disclosed are multiple character electronic display devices utilizing plurality of character matrices, each of which includes plurality of thermally isolated semiconductor mesas which are heated by current passed through a resistance. The current in each mesa is controlled by a transistor formed therein, and such transistors may have a common collector voltage and a common emitter voltage supply lead which may be individually closed by a switch to enable a desired character. The bases of the transistors of corresponding mesas in all of the character matrices may be connected to common control lines so that all character matrices may be controlled by the same character generator.

A particular diffusion pattern for the individual elements of the matrices is also disclosed which utilizes an extended collector transistor having a longitudinally extending, double diffused tunnel to provide cross connections from the control lines to the base contacts of the elements of an array.

6 Claims, 6 Drawing Figures
MULTI-CHARACTER ELECTRONIC DISPLAY

This invention relates generally to electronic displays, and more particularly relates to an integrated semiconductor display having a plurality of character generation matrices.

A multicharacter electronic display has previously been disclosed in U.S. Pat. No. 3,496,333. The print head there described utilizes a plurality of matrices of thermally isolated semiconductor mesas each containing a resistor for thermal heating and a diode for switching current through the resistor. While this device has many advantages over the prior art devices, one problem is that the voltage drop of the common bus lines and drive lines results in temperature gradients between adjacent elements, producing print density variations. Mismatches in thermal expansion coefficients prevent material reduction of these voltage drops.

Single character electronic displays have been devised and are described in copending U.S. Pat. No. 3,501,615 which have advantages resulting from the use of a switching transistor on each matrix element and a buffer transistor on an adjacent integrated circuit. This device has the advantage of lower control currents and more uniform heating as a result of the gain of the transistor devices. However, it has not heretofore been practical to incorporate this type of matrix into a multicharacter device because of the large number of devices and leads required.

This invention is concerned with the use of the transistor type of character matrix in such a manner as to overcome the problems of variable printing density encountered in previous diode controlled multiple character devices. This is achieved by utilizing the collector-base junction of the transistors in the individual mesas for isolation during switching so that a single character generator and single set of buffers may be used to control all character matrices, and the individual characters selectively enabled by controlling the power supply to the individual matrix.

The invention is also concerned with a particular element geometry which provides another level of interconnections to permit the high element densities required for good resolution.

The novel features believed characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as other objects and advantages thereof, may best be understood by reference to the following detailed description of an illustrative embodiment, when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a simplified plan view of an electronic display in accordance with the present invention;
FIG. 2 is a partial perspective view of a portion of an electronic display in accordance with the present invention;
FIG. 3 is a schematic circuit diagram of an electronic display system in accordance with the present invention;
FIG. 4 is a schematic layout of the interior face of the semiconductor elements of the arrays;
FIG. 5 is an enlarged schematic plan view of one of the individual elements shown in FIG. 4; and
FIG. 6 is a schematic circuit diagram of a portion of the matrix represented in FIG. 4.

Referring now to the drawings, and in particular to FIGS. 1 and 2, three four-character electronic display devices in accordance with the present invention are indicated generally by the reference numerals 10a, 10b, and 10c. Each of the electronic display devices 10a–10c includes four character matrices 12a–12d. Each matrix includes a 5 x 7 array of elements E₁–E₅₇ each of which is air isolated around its periphery and which is bonded to a ceramic slice 14 by a thermal insulating epoxy layer 16. The devices 10a–10c can be fabricated using the various processes heretofore described in the above-referenced Nos. 3,496,333 and 3,501,615.

As will be presently described, a transistor with a series resistor in the collector branch is formed by a diffusion in the face of each element E₅₇ adjacent the epoxy layer 16. Thin film circuits deposited on the interior face of the semiconductor element are used to interconnect the diffused devices into an integrated circuit. For example, element E₁ in each of the characters includes a transistor T₁ and a resistor R₁ (See FIG. 3), and element E₅₇ in each character includes transistor T₅₇ and resistor R₅₇.

The collectors of all of the transistors T₁–T₅₇ of a particular character are connected through the respective resistors R₁–R₅₇ to a common collector voltage supply line 18. All of the emitters of the transistors T₁–T₅₇ of each of the characters 12a–12d are connected to common emitter supply lines 20a–20d, respectively. Each of the character matrices 12 may then be selectively enabled by selectively applying power across the resistor-transistor circuits of the elements of the particular matrix by closing the appropriate emitter circuit 20.

As illustrated in FIG. 3, the collector circuits 18 of all characters in the system are common, and the emitter circuits of each matrix are individually selected by a character select switch 22.

The base contacts of the transistors of the corresponding elements of all character matrices in the device are also common. For example, the bases of transistors T₁ of characters 12a–12d of all devices 10a–10c are connected to a common control line C₁, and transistors T₅₇ are connected to a common control line C₅₇. Of course, it will be understood that the bases of transistors T₁–T₅₇ (not illustrated) would be connected to corresponding control lines C₁–C₅₇ only a portion of which are illustrated in other figures presently to be described. The control lines C₁–C₅₇ extend from a character generator 24 which decodes electrical logic signal and produces a voltage sufficient to turn on the transistor T₁ on those control lines necessary to produce the desired character. As mentioned, the control lines C₁–C₅₇ are common to all character matrices in the system, which may typically be eighty characters for a line, so that only one character generator and one set of output buffer transistors are required. Higher speeds can be achieved, however, by utilizing parallel-connected multiple character generators and corresponding output buffer transistors for parallel selection and pulsing of corresponding character matrices (12a–12d) of each plural character electronic display device (10a–10c).

In the operation of the system, the character select switch 22 would typically scan from the left-hand character matrix to the right-hand character matrix in
sequence by selectively connecting the common emitter lines 20a–20d of the character matrices to ground. Then during the period that each particular character matrix is thus enabled, the collector voltage supply is applied to the common collector lead 18 and the character generator produces the positive voltage levels on the control lines C1–C16 necessary to generate the character to be displayed or printed at the selected position. For example, a positive voltage on the control line C1 would turn transistor T1 of the enabled character matrix “on”, thus causing element E1 to be heated by the power dissipated in resistor R1. The transistor connected to control lines at ground potential would remain turned “off”. For example, if control line C16 is at ground potential, transistor T16 of the enabled character would remain “off”. It is important to note that the collector-base junctions of all transistors of all disabled character matrices block current from the collector supply voltage line 18 from passing through the common control lines and turning on the transistors T16 of the enabled matrix that should be off to generate the desired character.

An alternative mode of selectively enabling a particular character matrix may also be employed. Instead of a common collector lead 18 for all character matrices, only the collectors of each matrix may be common and the common collectors of the disabled character matrices left floating. Then the collector-base junction of each transistor, the control line of which is positive, can be forward biased in each matrix in which the collector is floating. However, the collector-base junction of all other transistors of the matrices are reverse biased and block current from returning to the enabled matrix on a control line that is otherwise not positive, in the same manner as the free floating base-emitter junctions of the disabled matrices in the circuit illustrated in the drawings.

Similarly, the free-floating base-emitter junctions of the disabled matrices prevent current from passing from a positive control line through a forward biased base-emitter junction to common emitter line 20a, and back through the emitter-base junction to a control line that should not be positive.

Another aspect of the present invention is illustrated in FIG. 4 which depicts the general layout of the elements E of the matrices in 12a–12c of a device 10a.

The highly repetitive array has been simplified in FIG. 4 with the element E shown in greater detail in FIG. 5 as an example of the diffusion and contact geometry. N-type semiconductor material, which may be starting material, N-type diffused into P-type, or epitaxially grown, forms an expanded collector region 30. A P-type base diffusion 34 and a P-type tunnel diffusion 36 are performed simultaneously in the starting material. An N⁺-emitter diffusion 38 and N⁺-n type diffusion 40 are performed simultaneously. The surface of the element E is coated with a layer of insulating material, such as silicon dioxide, and a collector contact opening 42, a base contact opening 44, an emitter contact opening 46, and a shorting contact opening 48 are formed on all elements of the device. It will be noted that opening 48 extends across the junction between diffused regions 36 and 40 to short the base-emitter of the potential NPN transistor formed by diffusions 36 and 40 and the collector region 30. In addition, a control line contact is cut in the oxide at one of five positions I–V depending upon which column the particular element is located in. For example, elements E1, E6, etc. in the first column of the matrix would have contact openings at position I, elements E6, E11, etc. in the second column of the matrix would have openings cut at position II, etc. Since element E16 is in the third column, a contact opening 50 is made at position III.

A shorting lead 52 (all leads are shown in darkened outline in FIG. 5) electrically connects the diffused tunnel 40 to the base region 34 through contact openings 48 and 44.

The control lines C1–C16 are formed on the insulating layer and extend transversely across the rows of elements and are automatically electrically connected to the base of the appropriate transistor through the contact opening at the position I–V, the diffused tunnel 40 and shorting contact 52. For example, control line C6 is connected to the base of the transistor of element E6 through contact opening 50, the diffused tunnel 40, contact opening 48, shorting lead 52, and base contact opening 44.

As can be seen in FIG. 4, the alternate rows of elements are inverted so that a common conductor strip 54 extends through the collector contact openings 42 of elements E1–E16 of each of the successive character matrices 12a–12c. Similarly, common ground strips 56a–56c extend through the emitter contact openings 46 of elements E6–E16 of matrices 12a–12c, respectively. The collectors of elements E1–E16 are connected to collector supply voltage strip 58, the bases of elements E1–E6, of matrices 12a–12c are connected to strips 60a–60c, respectively, the collectors of elements E1–E6 are connected to strip 62, the emitters of elements E1–E6, of matrices 12a–12c are connected to strips 64a–64c, respectively, and the collectors of elements E1–E6 are connected to strip 66. The emitter strips 56a–56c, 60a–60c, and 64a–64c are connected to the common character select lines 20a–20d, respectively.

Control lines C1–C16, C11–C16, C1–C16, C1–C16, C11–C16, C1–C16, and C1–C16 extend over elements E1–E6, E1–E6, E1–E6, E1–E6, E1–E6, E1–E6, and E1–E6 of all matrices 12a–12d of all devices 10b in the system, if desired.

The schematic circuit diagram for the elements shown in FIG. 4 are illustrated in FIG. 6 wherein corresponding parts are designated by the corresponding reference characters.

Although the transistors described above with regard to a preferred embodiment of this invention are NPN type, PNP type could be employed in lieu thereof. Also in the above described preferred embodiment the resistance for heating each mesh of each matrix is the collector saturating resistance of the diffused transistor. Such resistance can be a separate component formed in or on each mesh of each matrix. It is also contemplated that other size arrays, e.g., 7 × 9, 11 × 15, may be utilized in lieu of the 5 × 7 array described in detail herein; that meshes having geometric shapes other than that disclosed herein may be employed depending upon the desired print font; and that each display device may incorporate more or less characters than the four disclosed herein.

Although a preferred embodiment of the invention has been described and illustrated, it is to be un-
What is claimed is:

1. In an electronic display, the combination comprising:
   a plurality of character matrices with each matrix having rows and columns of a corresponding number of semiconductor elements each including a transistor and a resistance,
   means for electrically interconnecting the collectors of each transistor in each matrix through its respective resistance,
   means electrically interconnecting the emitters of each transistor of each matrix,
   means for selectively sequentially enabling said matrices, and
   separate control lines respectively common to the bases of the transistors of said rows of corresponding ones of said semiconductor elements in said matrices, wherein the collector-base junctions of the transistors connected to the unactivated control lines in a disabled matrix are reverse biased and block current that may return to the enabled matrix.

2. The combination of claim 1 wherein:
   said means for electrically interconnecting the collectors electrically interconnects all the collectors of each transistor of all of said matrices, and
   said means for selectively sequentially enabling said matrices selectively electrically connects the emitters of each transistor of each matrix to ground.

3. The combination of claim 1 wherein:
   said means for electrically interconnecting the emitters electrically interconnects all the emitters of each transistor of all of said matrices, and
   said means for selectively sequentially enabling said matrices selectively electrically connects the collectors of each transistor in each matrix to a voltage supply.

4. In an electronic display, the combination comprising:
   a row of semiconductor elements each including a transistor and a resistance,
   means for electrically interconnecting the collectors of a first and another second group of the collectors of each transistor in each of said groups through its respective resistance,
   means for electrically interconnecting the emitters of each transistor of each group,
   means for selectively sequentially enabling said groups and separate control lines respectively common to different bases of the transistors in different ones on said groups wherein the collector-base junctions of the transistors connected to the unactivated control lines in a disabled group are reverse biased and block current that may return to the enabled group.

5. The combination of claim 4 wherein:
   said means for electrically interconnecting the collectors electrically interconnects all the collectors of each transistor of all of said matrices, and
   said means for selectively sequentially enabling said groups selectively electrically connects the emitters of each transistor of each group to ground.

6. The combination of claim 4 wherein:
   said means for electrically interconnecting the emitters electrically interconnects all the emitters of each transistor of all of said groups, and
   said means for selectively sequentially enabling said groups selectively electrically connects the collectors of each transistor in each group to a voltage supply.

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