SYSTEM FOR MULTI-BYTE READING

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ABSTRACT
A control device, system and method for multi-pixel reading provides a processor receiving multi-pixel, uses memory units wherein each memory unit sequentially receiving a writing enable signal, and then receiving and storing multi-pixel. Simultaneously, the processor having multi-data bus receives multi-pixel of the each memory unit output. The clock of the enabling all the memory units is less than the delay of the processor reading, so that reducing the spare time of the image decoding system and reducing the reading time of the reading image.
FIG. 1 (Prior Art)

FIG. 2
FIG. 3B
At least one buffer full of data

Inform processor to read data

Write in register with buffer’s data

Processor read register’s data once
SYSTEM FOR MULTI-BYTE READING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 11/001,636 (Att. Docket VI8438P), filed on Dec. 2, 2004 and entitled CONTROLLER FOR OUTPUTTING MULTI-BYTE IMAGE DATA SIMULTANEOUSLY, which claims the benefit of U.S. Provisional Application No. 60/526,294, filed on Dec. 3, 2003 and entitled VIDEO DECODER, the entire contents of all which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention
[0003] 2. Description of Related Art
[0004] [0005] JPEG, Joint Photographic Experts Groups, is basically a data processing method that normally includes a recovery (decoding) method. Referring to FIG. 1, it shows a system, which normally decodes something with a dual buffer within a system. The image data is processed by a Huffman decoder (not shown) and an inverse quantifier (not shown). Then, the IDCT (Inverse Discrete Cosine Transform) block 110 processes the data and outputs it to be stored in the first buffer 120. When IDCT block 110 fills the first buffer 120 with data, a signal is sent to inform the 32-bit processor 150. And the 32-bit processor 150 reads the first buffer's data by switching the multiplexer 140. At this time, the IDCT block 110 continuously processes the image data and outputs the data to be stored in the second buffer 130.

[0006] Generally, it is an I/O (input and output) action that the processor reads the first buffer's data. It means that a delay happens between the time that the processor is informed and the time of the actual reading. For example: based on the clock unit, the delay is about 6 to 7 system clocks. However, the delay in the prior art causes the processor to idle. Next, the processor reads the data of the first buffer based on an 8-bit unit for JPEG. It only can process 8 bits of data for JPEG even the processor with 32 bits can process 32 bits of data. As a result, the processor cannot work efficiently.

[0007] According to the previous mentioned disadvantage of the multi-bit reading, a new and improved device, system and process is needed for multi-bit reading to solve the problem in the prior art such as: how to use the delay when the processor reads the data, how to provide the multi-bit data for reading and how to improve the efficiency of the processor.

SUMMARY OF THE INVENTION

[0008] According to the defects of the prior art, the well-known multi-bit reading, such as: the processing time is delayed and the system is idle, and the efficiency of the processor is questioned. The object of the invention provides a device, system and method for multi-bit reading, which improves the above-mentioned disadvantage.

[0009] The object of the invention provides a device, system and method for processor reading. For the processor reading and writing image data into registers is in the delay period of the processor reading clock.

[0010] The object of the invention also provides a device, system and method for improving the efficiency of the processor reading. By storing multi-byte image data, the processor reads the reading multi-byte data during a reading sequence. This is the way to fully utilize the data bus.

[0011] The object of the invention further provides a device, system and method for processing data of the different compressing format. The invention can utilize JPEG and MPEG2 format data.

[0012] Accordingly, the objects of the invention provide a device, system and method for multi-byte reading. It provides a processor receiving multi-byte image data. By utilizing a portion of the memory units, after every memory unit sequentially receives the writing, the signals are enabled respectively, therefore, receiving and storing the multi-byte image data. When IDCT (Inverse Discrete Cosine Transform) unit informs the processor to read data, by the multi-byte bus of the processor, the processor simultaneously receives the output of these memory units. Hence, the clock that's enabling all the memory units has less delay for the processor reading.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0014] FIG. 1 is a schematic block diagram illustrating a normal decompresing image data system with a dual buffer according to the prior art;

[0015] FIG. 2 is a schematic block diagram illustrating a decompresing image data system with a dual buffer according to the invention;

[0016] FIG. 3A and FIG. 3B are different schematic block diagrams illustrating one control circuit according to the invention;

[0017] FIG. 4 is a schematic flow chart illustrating decoding system.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] Some sample embodiments of the invention will now be described in greater detail. Nevertheless, it should be recognized that the present invention could be practiced in a wide range of procedures.

[0019] The present invention will be described in detail with reference to the accompanying drawings. It should be noted that the drawings are in greatly simplified form and in order to provide a clear illustration and understanding of the present invention.

[0020] Referring to FIG. 2, it is an embodiment of decompressing image data according to this invention. The IDCT (Inverse Discrete Cosine Transform) unit 210 connects to a plurality of buffers (for example, the first buffer 220 and the second buffer 230) for receiving image data, writing data to buffers and transmitting a signal to the processor 250. A plurality of buffers connects to the control circuit 260 through the multiplexer 240, and the control circuit 260 connects to the processor 250. In one embodiment, the first buffer 220 and second buffer 230 are general memory devices, for example, Random Access Memory (RAM). Next, the processor 250 is a general processor with the 32-bit bus and the input/output function. However, it is not limited to this. The more bits the processor has, the more merit the invention has. Between the time of preparing to send and receive the data and the time of...
actually receiving the data, the processor 250 has a clock delay, which is induced by the physical characters of the hardware device. In one embodiment, the processor 250 has a 6 to 7 system clocks delay. The clock delay is not limited here, and the more clock delays with the processor 250 the more distinct merits the present invention has.

[0021] The control circuit 260 receives data from the first buffer 220 and the second buffer 230, and provides image data to the processor 250. The processor 250 does not directly read the data of the buffers that is connected to the IDC unit 210. It means that the first buffer 220 or the second buffer 230 could transmit the image data through the multiplexer 240 to the control circuit 260 when the processor 250 reads in the “idle” state. Then, the processor 250 reads the data directly from the control circuit 260, while the buffer processing the reading data. There, the processor 250 could read the data with a wide range for improving the efficiency of the processor. For example: the range of the data read can be increased from 1 byte to 2 bytes or 4 bytes. It is noted that the time of transmitting the image data to the control circuit 260 must take less time than the clock reading of the processor 250.

[0022] The multiplexer 240 controls the image data that is transmitted from the first buffer 220 or the second buffer 230 to the control circuit 260. The multiplexer 240 provides a data path for the data of first buffer 220 transmitting to the control circuit 260, when the stored data of the first buffer 220 is waiting for the processor 250 to read. At the same time, the IDC unit 210 receives the processed image data and stores them in the second buffer 230. Similarly, when the data of the second buffer 230 is waiting for the processor 250 to read, the multiplexer 240 provides a data path for the data of the second buffer 230 transmitting to the control circuit 260. At this time, the IDC unit 210 receives the processed image data and stores them in the first buffer 220.

[0023] Referring to FIG. 3A, it is an embodiment of the control circuit according to this invention. The control circuit 260 includes the input selection unit and memory units. The input selection unit in one embodiment, for instance: the multiplexer 240, is used to receive a plurality of the input image data 22a and 22b and to output data 23 to memory unit(s). Herein, the input image data 22a comes from the first buffer, and the input image data 22b comes from the second buffer. It is noted that the control circuit of this invention is not limited in that the multiplexer as the input selection unit. The control circuit is suitable for any designed logic circuit to replace the multiplexer. The memory units, for example: the registers 2602, 2604, 2606 and 2608, respectively receives the writing enable signals 24a, 24b, 24c and 24d, that are corresponded and controlled by the control signal units 25a to 25d respectively. After receiving the corresponding writing enable signal, each memory unit respectively receives the data 23 from the multiplexer 240 and further outputs the necessary data 26a, 26b, 26c, 26d and 26e to the corresponding processor, such as processor 250. It is noted that the writing enable signals 24a, 24b, 24c and 24d, by corresponding clock times, sequentially writing enable the register 2602, 2604, 2606 and 2608. The control signal units 25a to 25d can be inside of the control unit 260 or outside of the control unit 260. In the embodiment, the time of the enabling all registers is no more than the delay of the processor reading clock. In the embodiment, every writing enable signal enables a register for a clock and the embodiment for example is 4 accumulated clocks. The enabling time, 4 clocks, does not exceed the processor delay clock, 6 to 7 clocks. In the embodiment, it further includes a data bus of a plurality of byte data (not shown). The data bus is for receiving and transmitting the data of all the memory units (register 2602, 2604, 2606 and 2608).

[0024] Next, the invention suits many kinds of compressed image data, such as: Motion Picture Experts Group 2, MPEG 2, and JPEG. Different compressed image data has different bit numbers (especially for writing enable signal), for example: MPEG 2 has 9 bits data and JPEG has 8 bits data. Referring to FIG. 3B, the invention can further include a multiplexer 2603 for selecting between different bit data and the multiplexer 2603 outputs a data 26c (the multiplexer is not needed as the FIG. 3A, if the input is not different bit data). The register 2602 and the register 2604 connected to the multiplexer 2603 have different pin numbers from each other. In one embodiment, the register 2602 and the multiplexer 240 connected with 9 pins and the register 2604 and the multiplexer 240 connected with 8 pins. In addition, the register 2606, the register 2608 and the multiplexer 240 connect with 8 pins, too. Next, the register 2602 has two different data outputs, one is 8 bits output, data 26a, and the other one is the highest bit or lowest bit of the output. And the register 2604 has the output, one is 7 bits output, data 26b, and the other one is the first bit of the output to the multiplexer 2603. When the decoding system applies in data inputting of MPEG 2, the multiplexer 2603 select the data from the register 2602 and outputs the bit data 26a and 8 bit data, 26c. The bit data 26a, 26c, and the 8 bit data combine a 9 bit data for doing motion compensation. When the decoding system applies in data inputting of JPEG, the multiplexer 2603 selects the data from the register 2604 and outputs a bit data, 26c and 7 bit data, 26b. The bit data 26c, and the 7 bit data combine an 8 bit data. In other words, the multiplexer 2603 outputs different data 26c by referring to the input format, and then the processor 250 controlled by the control circuit 260, can select the data from the register 2602 or the register 2604. Herein, the other registers are not connected to the multiplexer 2603, in the embodiment such as: register 2606 and 2608, have 8 bits output data, respectively, such as 26c and 26d.

[0025] According to the previous discussion, the received data of the processor is 32 bits and is equal to the bit numbers of the data bus. In the invention, the bit numbers of the output of the plurality of register is strongly close to the bit numbers of the data bus, so that the processor can read once for receiving the data that is equal to the bit numbers of the data bus. The processor can read multi-byte image data, efficiently utilizing the bit numbers of the data bus and have maximum performance of the data bus. One must explain that 32 bits do not limit the control circuit of the invention. And it is not limited by the 4-clock system delay. The only limitations are the following: the bit number of the data is no more than the bit number of the data bus of the processor, the processor can read the multi-byte data, and the total clock is not more than the reading delay of the processor. Any variation limited by the above limitations is included in the scope of the invention.

[0026] FIG. 4 shows a flow chart of an embodiment of the decoding system in the invention. After that the typical image data goes through the Huffman decoder and the Inverse quantizer, the typical data are inputted to the IDC unit 210. The data goes through the IDC unit and is written in a buffer and then at least one buffer full of data (step 410). When the buffer is full, the IDC unit informs the processor to read the data (step 420). The processor has an “m” bit data bus and a delay “n” that is the time between the reading signal received and that of the execution started. At the time of sending the read signal,
the data of the buffer write in registers in sequence (step 430). The total time of the data writing in a plurality of registers is less than the time of the delay "n". The processor reads the data of the registers at the same time (440). The processor reads the data and has a bit number, which is substantially equal (or not less than) to "m".

[0027] Because the control circuit of this invention applies to a decoding system with the dual buffer, the idle of reading image data and the writing in buffer of the IDCT unit do not depend on the acting of the processor. Next, the control circuit includes some registers. The register can receive data when clocks delay in the processor. This reduces the idle time. The total output bit of the register is close to the data bus, so as the processor can have the maximum performance of the data bus.

[0028] Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A controlling system for outputting multi-byte image data, comprising:
   an inverse discrete cosine transform (IDCT) unit for processing a plurality of image data;
   a plurality of buffers for receiving said plurality of image data processed by said inverse discrete cosine transform (IDCT) unit;
   a multiplexer connected to said plurality of buffers;
   a control circuit connected to said multiplexer for utilizing said multiplexer to move said image data from said buffers to said control circuit;
   a processor, connected to said control circuit, for receiving said image data from said control circuit simultaneously.

2. The controlling system according to claim 1, further comprising a data bus for transmitting data from said control circuit to said processor, wherein the bit number of said data bus is not less than the total bit number of said buffers.

3. The controlling system according to claim 1, when said processor is being idle, said buffers transmit said plurality of image data through said multiplexer to said control circuit, and when said processor is reading, said processor reads a plurality of said image data from said control circuit directly.

4. The controlling system according to claim 1, wherein said multiplexer controls said image data transmitted between said buffers and said control circuit, and at the same time, only one said buffer transmits data to said control circuit and other said buffers receive said image data processed by said inverse discrete cosine transform (IDCT) unit.

5. The controlling system according to claim 1, when any said buffer is full of data, said control circuit moves data of said filled buffer to said control circuit for enabling said buffer to receive data from said inverse discrete cosine transform (IDCT) unit.

6. The controlling system according to claim 1, when said control circuit is full of data, said IDCT unit sends a signal to said processor for informing said processor to read said control circuit.

7. A controlling system for outputting multi-byte image data, comprising:
   an inverse discrete cosine transform (IDCT) unit for processing a plurality of image data;
   a plurality of buffers for receiving said plurality of image data processed by said inverse discrete cosine transform (IDCT) unit;
   a multiplexer connected to said plurality of buffers;
   a control circuit connected to said multiplexer for utilizing said multiplexer to move said image data from said buffers to said control circuit and including:
   a plurality of memory units, each said memory unit receiving and storing a plurality of bit image data, wherein said plurality of memory units simultaneously and correspondingly output said plurality of bit image data, and the sum of said plurality of said bit image data equal to a plurality of byte image data; and
   a plurality of control signal units for generating a plurality of writing enable signals, said plurality of writing enable signals being corresponding to said plurality of memory units, respectively, wherein said plurality of writing enable signals control said plurality of memory units to be stored in said plurality of bit image data in sequence; and
   a processor, connected to said control circuit, for receiving said image data from said control circuit simultaneously.