METHOD OF MANUFACTURING A CHIP AND A CHIP STACK

Inventors: Chull Won Ju, Daejeon (KR); Byoung Gue Min, Daejeon (KR); Seong II Kim, Daejeon (KR); Jong Min Lee, Daejeon (KR); Kyung Ho Lee, Daejeon (KR); Young II Kang, Daejeon (KR)

Correspondence Address:
BLAKEY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040 (US)

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ABSTRACT
Provided are a chip, a chip stack, and a method of manufacturing the same. A plurality of chips which each include at least one pad formed on a wafer; and a metal layer which protrudes up to a predetermined thickness from the bottom of the wafer and is formed in a via hole exposing the bottom of the pad are stacked such that the pad and the metal layer of adjacent chips are bonded. This leads to a simplified manufacturing process, high chip performance and a small footprint for a chip stack.
METHOD OF MANUFACTURING A CHIP AND A CHIP STACK
CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of
Korean Patent Application No. 2005-89724, filed on Sep. 27,
2005, the disclosure of which is incorporated herein by ref-
ence in its entirety.

BACKGROUND

[0002] 1. Field of the Invention
[0003] The present invention relates to a chip, a chip stack,
and a method of manufacturing the same, and more particu-
larly, to a chip, a chip stack, and a method of manufactur-
ing the same in which a chip manufacturing process is simpli-
fied, chip performance is improved, and a footprint for a chip stack
is made small by forming a metal layer protruding from the
bottom of a wafer up to a predetermined thickness in a via
hole penetrating the wafer to expose the bottom of a pad
formed on the wafer.

[0004] 2. Discussion of Related Art
[0005] The ongoing development of wireless communica-
tion and digital multimedia technology, coupled with increas-
ing consumer demand, continues to fuel the trend toward
miniaturization, high performance, high integration, and
multi-functionality of portable digital electronic devices such as
portable phones, personal digital assistants (PDA), and
high performance multimedia devices.

[0006] For miniaturization of such portable digital elec-
tronic devices, system on chip (SoC) technology, in which
integrated circuits (ICs) having different functions are inte-
grated into one chip to function as a system, has been exten-
sively researched.

[0007] However, SoC technology can only integrate ICs
manufactured by the same processes into one chip. For
example, SoC technology cannot be applied to a metal oxide
semiconductor, a bipolar semiconductor, and a RF chip
because these ICs are fabricated on different wafers.

[0008] As an alternative to SoC, research into system on
package (SoP) technology is currently progressing. SoP inte-
grates ICs not integrated into one chip by SoC. In order to
implement SoP technology, a method of stacking ICs to be
mounted has been suggested as a way to reduce a footprint
of the ICs.

[0009] Such a chip stack is classified into a package stack
and a bare chip stack. The bare chip stack has a relatively
small footprint and the advantage of small size compared to
the package stack.

[0010] Many chip stacking methods have been suggested
to date. The package stack has the disadvantage of involving
a bulky process using wire bonding or a chip carrier. This
results in large inductance which degrades the performance of
ICs. Thus, the chip stack better facilitates miniaturization.

[0011] PCT/US1999-08744, entitled "Chip Stack and
Method of Making the same" discloses a conventional chip
stack technique using a carrier. The method involves sticking
chips by putting a chip on a chip carrier and forming a bump
on the carrier. However, conventional art using the chip car-
rier has the problem of a large footprint.

[0012] U.S. Pat. No. 6,395,630, entitled "Stacked Inte-
grated Circuits" discloses a chip stack technique in which a
bump is formed in the chip such that a hole having an aspect
ratio of 100 to 200 is formed to penetrate a wafer and a coaxial
conductor is formed in the hole using a chemical vapor depo-
sition (CVD) technique.

[0013] However, the conventional art in which the bump
is formed in the chip has several problems. These are, it is
difficult to form a hole having a high aspect ratio, a process for
forming the coaxial conductor in the hole using the CVD
 technique has a low deposition rate (e.g., 100 A/min) and
requires a long processing time, and an inner conductor pro-
cess and an outer conductor process should be performed
separately.

SUMMARY OF THE INVENTION

[0014] The present invention is directed to a chip, a chip
stack, and a method of manufacturing the same in which a
plurality of chips, which each comprise at least one pad
formed on a wafer and a metal layer which protrudes up to a
predetermined thickness from the bottom of the wafer in a via
hole penetrating the wafer to expose the bottom of the pad,
are stacked such that the pad and the metal layer of adjacent chips
are bonded. This leads to a simplified manufacturing process,
high chip performance and a small footprint for a chip stack.

[0015] A first aspect of the present invention provides a
chip, comprising: at least one pad formed on a wafer; and a
metal layer formed to protrude up to a predetermined thick-
ness from the bottom of the wafer in a via hole penetrating
the wafer to expose the bottom of the pad.

[0016] A second aspect of the present invention provides
a chip stack, comprising: a plurality of chips which include at
least one pad formed on a wafer and a metal layer formed to
protrude up to a predetermined thickness from the bottom of
the wafer in a via hole penetrating the wafer to expose the
bottom of the pad, wherein the pad and the metal layer of
adjacent chips are bonded to each other.

[0017] A third aspect of the present invention provides a
method of manufacturing a chip, comprising: (a) depositing
a seed metal layer on the entire surface of a wafer on which
at least one pad is formed; (b) lapping a lower portion of
the wafer so that the wafer has a predetermined thickness
and then forming a via hole forming pattern on the exposed wafer;
(c) etching the wafer to expose the bottom of the pad using
the via hole forming pattern as an etching mask to form a via hole;
and (d) forming a plated metal layer to protrude tip to a
predetermined thickness from the bottom of the wafer in the
via hole to contact the exposed bottom of the pad and then
removing the seed metal layer and the via hole forming pat-
tern.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The above and other features and advantages of the
present invention will become more apparent to those of
ordinary skill in the art by describing in detail preferred
embodiments thereof with reference to the attached drawings
in which:

[0019] FIG. 1 is a cross-sectional view of a chip according
to an exemplary embodiment of the present invention;
[0020] FIG. 2 is a cross-sectional view of a chip stack
according to an exemplary embodiment of the present inven-
tion; and
[0021] FIGS. 3a to 3g are cross-sectional views illustrating a method of manufacturing a chip according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0022] Hereinafter, an exemplary embodiment of the present invention will be described in detail. However, the present invention is not limited to the embodiments disclosed below, but can be implemented in various types. Therefore, the present embodiment is provided for complete disclosure of the present invention and to fully inform the scope of the present invention to those ordinarily skilled in the art.

[0023] FIG. 1 is a cross-sectional view of a chip according to an exemplary embodiment of the present invention, and FIG. 2 is a cross-sectional View of a chip stack according to an exemplary embodiment of the present invention.

[0024] Referring to FIG. 1, the chip of the present invention comprises at least one pad 200 formed on a wafer 100, a via hole (see 600 in FIG. 3a) which penetrates the wafer to expose the bottom of the pad 200, and a metal layer 700 which protrudes from the bottom of the wafer 100 by a predetermined thickness.

[0025] Referring to FIG. 2, the chip stack of the present invention has a structure that a plurality of chips are stacked so that the pad 200 and the metal line 700 of adjacent chips are bonded to each other.

[0026] For the convenience of description, FIG. 2 shows that only three chips are stacked, but the number of chips to be stacked is not limited. That is, two or more chips can be stacked.

[0027] FIGS. 3a to 3g are cross-sectional views illustrating a method of manufacturing a chip according to an exemplary embodiment of the present invention.

[0028] Referring to FIG. 3a, at least one pad 200 is formed on a wafer 100 at a regular interval, and then a seed metal layer 300 is deposited on the entire surface of the wafer 100 including the pad 200. The seed metal layer 300 is made of, e.g., titanium/copper (Ti/Cu) and deposited by a sputtering technique. The titanium/copper (Ti/Cu) layer is formed to a thickness of about 400 Å to 600 Å/2000 Å to 4000 Å (preferably, about 500 Å/3000 Å).

[0029] The seed metal layer 300 serves as an electrode when, e.g., an electroplating technique is used to fill a metal layer (see 700 in FIG. 3f) in a via hole (see 600 in FIG. 3e) which will be described later.

[0030] Referring to FIG. 3b, the bottom surface of the wafer 100 is subjected to a lapping process so that the wafer 100 has a relatively thin thickness of about 100 μm to 400 μm (preferably, about 300 μm).

[0031] The lapping process may reduce a processing time of a dry-etching process for forming the via hole (see 600 in FIG. 3e) since it reduces the thickness of the wafer 100. The lapping process may also reduce a lapping time when an electroplating technique is used to form the metal layer (see 700 in FIG. 3f) in the via hole. In addition, the thickness of the metal layer 700 can be easily adjusted by reducing an aspect ratio of the via hole 600.

[0032] Referring to FIG. 3c, an oxide layer 400 is deposited on the exposed bottom of the wafer 100, and then a photosist is coated on the oxide layer 400. The photosist is etched by exposure and developing techniques using a via hole forming mask (not shown) to thereby form a photosist pattern 500.

[0033] Referring to FIG. 3d, the oxide layer 400 is etched using the photosist pattern (see 500 in FIG. 3c) as an etching mask, and then the photosist pattern 500 is removed, thereby forming a pattern 400 for forming a via hole.

[0034] Here, the oxide layer 400 is preferably dry-etched by reactive ion etching (RIE) equipment using, e.g., CF₄ or CCl₄.

[0035] Referring to FIG. 3e, the wafer 100 is etched using the via hole forming pattern 400 as an etching mask to expose the bottom of the pad 200, thereby forming the via hole 600 having a constant aspect ratio (e.g., about 1 to 3).

[0036] Preferably, the via hole 600 is formed by a dry etching technique employing the RIE equipment using a gas containing fluorine (F) such as CF₄ and SF₆ to etch silicon (Si) or a gas such as SF₆ and BCl₃ to etch a gallium arsenide (GaAs).

[0037] Referring to FIG. 3f, the wafer 100 is mounted in plating equipment of a foundation type to which a lead free solder solution is sprayed, and a plating metal layer 700 is formed in the via hole 600 to protrude up to a predetermined thickness from the bottom of the wafer in the via hole using an electroplating technique so that the plating metal layer 700 contacts the exposed bottom of the pad 200.

[0038] At this time, the metal layer 700 is formed such that a first metal layer is formed to a predetermined thickness by the electroplating technique using a copper plating solution and then a second metal layer is formed on the first metal layer to protrude up to a predetermined thickness from the bottom of the wafer 100 by the electroplating technique using a plating solution which is lead-free and has a low melting point such as stannum/copper (Sn/Cu), stannum (Sn) and stannum/bismuth (Sn/Bi).

[0039] Here, a portion of the metal layer 700 from the bottom of the pad 200 to the bottom of the wafer 100 is referred to as a via metal layer, and a portion of the metal layer which protrudes up to a predetermined thickness from the bottom of the wafer 100 is referred to as a bump.

[0040] When the metal layer 700 is formed by the electroplating technique, the plating speed is fast and uniformity of the plating layer can be adjusted within about 5%, and thus the bump with a thickness of several tens of micrometers μm can be formed in a short time.

[0041] Referring to FIG. 3g, the seed metal layer 300 and the via hole forming pattern 400 are etched and thus removed, thereby completing the chip having the bump protruding from the bottom of the wafer 100 according to the present invention.

[0042] The chip stack of FIG. 2 can be formed by stacking at least two chips manufactured with reference to FIGS. 3a to 3g in the way that the pad 200 and the metal layer 700 are bonded by a fusion bonding technique.

[0043] As described above, since the protruding bump is formed on the bottom of the wafer 100, there is no need for flip when the chips are stacked, and since the bump made of a lead free metal has a low melting point of about 220°C, it can be melted on a typical hot plate, leading to high processing efficiency.

[0044] The chips can be stacked using the bump protruding from the bottom of the chip without a conventional adhesive, and the bump serves as a heat path for dissipating heat generated in the chip, and thus the present invention has an advantage in that heat dissipation efficiency is improved and the footprint is reduced compared to conventional chip stack technology using a wire.
As described above, according to the present invention, a chip, a chip stack, and a method of manufacturing the same have an advantage in that at least one pad is formed on the wafer, and the metal layer which protrudes up to a predetermined thickness from the bottom of the wafer is formed in the via hole penetrating the wafer to expose the bottom of the pad, i.e., a signal of the pad is led to the bottom of the chip, so that a metal layer, i.e., a bump protruding from the bottom of the wafer can be formed without redistributing the signal line, leading to a simplified manufacturing process.

Further, since the bump protruding from the bottom of the wafer serves as an interconnection point as well as a contact point when the chips are stacked, the bonding length is short and degradation of the chip performance is small compared to the interconnection of the conventional art using wire bonding.

Furthermore, it is easy to stack the chips and it is possible to stack the chips using the bump, and thus the footprint for the chip stack can be small, and since the bump serves as a heat sink for dissipating the heat generated from the chips when the chips are stacked, heat dissipation efficiency is improved.

While the invention has been shown and described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made. Therein without departing from the spirit and scope of the invention as defined by the appended claims.

1. A chip, comprising:
   at least one pad formed on a wafer; and
   a metal layer formed to protrude up to a predetermined thickness from the bottom of the wafer in a via hole penetrating the wafer to expose the bottom of the pad.

2. The chip of claim 1, wherein the via hole has an aspect ratio of 1 to 3.

3. The chip of claim 1, wherein the metal layer includes a first metal layer formed to a predetermined thickness from the exposed bottom of the pad using a copper and a second metal layer formed on the first metal layer to protrude up to a predetermined thickness from the bottom of the wafer using one of tin/tin/copper (Sn/Cu), tin/tin (Sn) and tin/tin/bismuth (Sn/Bi).

4. A chip stack, comprising:
   a plurality of chips which include at least one pad formed on a wafer and a metal layer formed to protrude up to a predetermined thickness from the bottom of the wafer in a via hole penetrating the wafer to expose the bottom of the pad,
   wherein the pad and the metal layer of adjacent chips are bonded to each other.

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