(19) United States
(12) Patent Application Publication
(10) Pub. No.: US 2002/0012416 A1
Thompson et al.
(43) Pub. Date: Jan. 31, 2002

(54) METHOD TO FIND A VALUE WITHIN A RANGE USING WEIGHTED SUBRANGES

(75) Inventors: William N. Thompson, Meridian, ID (US); John D. Porter, Meridian, ID (US); Lauren Gene Weber, Caldwell, ID (US)

Correspondence Address:
Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: Danny J. Padyk
P.O. Box 2938
Minneapolis, MN 55402 (US)

(73) Assignee: Micron Technology, Inc.

(21) Appl. No.: 09/922,983
(22) Filed: Aug. 6, 2001

Related U.S. Application Data
(62) Division of application No. 09/382,525, filed on Aug. 25, 1999, now Pat. No. 6,275,119.

Publication Classification
(51) Int. Cl. H03K 23/00
(52) U.S. Cl. 377/118

(57) ABSTRACT

A method of finding an unknown value from within a range of values is disclosed that divides the range into weighted subranges and then, beginning with an arbitrary search value within the range, performs a number of simple comparisons to determine the value for each subrange that will result in a match with the target value. This method can also detect those cases where the target value lies outside the range. In one embodiment, the method of finding an unknown value within a range of values is applied to impedance matching. In this embodiment, the output impedance of a pin on an integrated circuit is automatically matched to the impedance of the load connected to it. The output driver has a controllable impedance that can be adjusted within a specific range of impedances to match the external load impedance it is to drive.

```
100 -> 102
INITIALIZE
SET LOS=0
SET N=NUMBER OF SUBRANGES

104 -> SET HOS=N-1

106
SET =LOS

108
Y
SEARCH=TARGET

110
? Y
SEARCH=TARGET

114
? Y
SEARCH=TARGET

118
? Y
SEARCH=TARGET

120
INCREMENT S(i)

122
INCREMENT S(i)

126
HOS=LOS

148
SOLUTION FOUND
STORE SOLUTION

132
134
N
Y
SET S(i)=MIN(i)
INCREMENT i

138
N
Y
DECIMATE S(i)=140
SEARCH=TARGET

144
Y
UNDERFLOWT

124
N
OVERFLOW

142
N
SEARCH=TARGET

130
Y
136
140
SET S(i)=MIN(i)

112
Y
116
SET HOS=i

114
? Y
SEARCH=TARGET

118
? Y
SEARCH=TARGET

120
INCREMENT S(i)

122
INCREMENT S(i)

126
HOS=LOS

148
SOLUTION FOUND
STORE SOLUTION
```

**FIGURE 1**

- **SET LOS=0**
- **SET N=NUMBER OF SUBRANGES**
- **SET HOS=N-1**
- **SET i=LOS**
- **SET S(i)=MIN(i)**
- **INCREMENT i**
- **SEARCH>TARGET**
- **S(i)=MIN(i)**
- **UNDERFLOW**
- **DECREMENT S(i)**
- **SEARCH>TARGET**
- **SOLUTION FOUND STORE SOLUTION**

**HOS—HIGHEST ORDER SUBRANGE**
**LOS—LOWER ORDER SUBRANGE**
**S(i)—VALUE OF SUBRANGE**
**MIN(i)—MINIMUM VALUE OF SUBRANGE**
**MAX(i)—MAXIMUM VALUE OF SUBRANGE**
FIGURE 4B
METHOD TO FIND A VALUE WITHIN A RANGE USING WEIGHTED SUBRANGES

FIELD OF THE INVENTION

[0001] This invention relates to the field of information processing, and more particularly, to the matching of values in information systems.

BACKGROUND OF THE INVENTION

[0002] Information processing applications must often find a value within a range of values. For example, a sorting system may organize discrete units of information into groups defined by numerical boundaries. Before assigning each discrete unit of information to a group, the relationship between each discrete unit of information and the numerical boundaries must be established. Defining these relationships often requires finding a value within a range of values. In some sorting systems, this is accomplished using a compute intensive sort algorithm in combination with a high performance microprocessor. Unfortunately, high performance microprocessors are expensive, and therefore not suitable for use in products directed to the consumer market.

[0003] An analog-to-digital (A/D) converter generates digital output information related to analog input information. The conversion process associated with one type of A/D converter requires manipulating discrete pieces of information, the on and off states of resistor ladder switches, in such a way that the final configuration of resistor ladder switches matches a value within a range of values. Modern A/D converters are designed to operate on a single chip and to function in a variety of end user applications, such as cellular telephones and video games. A single A/D converter design may be required to function in an application that requires eight, twelve, sixteen or more bits of resolution. Designers attempt to provide this flexibility in an A/D converter by providing an on chip microprocessor. Unfortunately, the supplied microprocessor often has a limited instruction set, and operates at a low frequency, so the requirements for applications that must operate at both high frequency and high resolution, such as quickly matching a two byte value within a range of values, are difficult to meet.

[0004] Some control systems seek to drive a difference signal, which is the difference between an output information signal and an input signal, to zero in order to maintain a constant relationship between the input signal and the output information signal. This process of driving the difference signal to zero may require the identification of a value within a range of values.

[0005] In modern digital control systems, the control function is often performed by a microprocessor. In some systems designed primarily for high reliability, such as systems designed for use in satellites, high function may also be required. High function microprocessors tend to fail more often than low function microprocessors, so it is difficult to meet both requirements, and often a low function microprocessor is selected for a particular application. Unfortunately, the same algorithms and software that accomplish tasks on a high function microprocessor, such as identifying a value within a range of values, do not work on low function microprocessors.

[0006] For these and other reasons there is a need for the present invention.

SUMMARY OF THE INVENTION

[0007] The above-mentioned problems and other problems are addressed by the present invention and will be understood by one skilled in the art upon reading and studying the following specification. A method of finding an unknown value from within a range of values is disclosed that divides the range into weighted subranges and then, beginning with an arbitrary search value within the range, performs a number of simple comparisons to determine the value for each subrange that will result in a match with the target value. This method can also detect those cases where the target value lies outside the range.

[0008] In one embodiment, the method of finding an unknown value within a range of values is applied to impedance matching. In this embodiment, the output impedance of a pin on an integrated circuit is automatically matched to the impedance of the load connected to it. The output driver has a controllable impedance that can be adjusted within a specific range of impedances to match the external load impedance it is to drive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a flowchart of the general operation of the method of finding a value within range using weighted subranges.

[0010] FIG. 1A is a block diagram of one embodiment of an impedance matching system including a controllable impedance.

[0011] FIG. 1B is a block diagram of one embodiment of an impedance matching system including a variable impedance and a control system.

[0012] FIG. 2A is a diagram of a metal-oxide-semiconductor field-effect transistor (MOSFET) suitable for use in connection with one embodiment of the present invention.

[0013] FIG. 2B is a graph of the drain-to-source conductance of a MOSFET suitable for use as a variable impedance in one embodiment of the present invention.

[0014] FIG. 2C is a schematic diagram of a parallel connection of serially connected resistor-transistor pairs suitable for use in connection with one embodiment of the present invention.

[0015] FIG. 3 is a block diagram of a control system for use in connection with one embodiment of the present invention.

[0016] FIG. 4A is part one of a flowchart of one embodiment of an impedance matching method.

[0017] FIG. 4B is part two of a flowchart of one embodiment of an impedance matching method.

DETAILED DESCRIPTION OF THE INVENTION

[0018] In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which are shown, by way of illustration, specific embodiments in which the invention may be practiced. The embodiments are intended to describe aspects of the invention in sufficient detail to enable those skilled in the art to practice the invention. Other embodi-
ments may be utilized and changes may be made without
departing from the scope of the present invention. The
following detailed description is not to be taken in a limiting
sense, and the scope of the present invention is defined only
by the appended claims.

GENERAL ALGORITHM DESCRIPTION

[0019] A method of finding an unknown value from within
a range of values operates by dividing the range into
weighted subrange. Beginning with an arbitrary search
value within the range, the method performs a number of
simple comparisons to determine the value for each sub-
range that will result in a match with the target value. This
method can also detect those cases where the target value
lies outside the range.

[0020] The first general step of the method is to define the
allowable range and the subranges that will be used. The
subranges are defined such that higher order subranges
represent some multiple of the next lower order subrange.
An example would be the use of the place order of digits in
a search value becomes the subranges for ones, tens, hundreds,
etc. In this example the ones subrange is the lowest order
subrange and offers the finest resolution. Each higher order
subrange is a multiple of the subrange that precedes it,
offering a reduction in resolution as a trade off for a larger
step size for use in searching for the target value. With the
subranges defined, the unknown target becomes a reference
to compare the search value against.

[0021] Depending on the results of an initial comparison,
the search branches to either of two paths to determine the
corresponding subrange of the highest order subrange needed to
achieve a match condition. Upon successful completion of either path, a lower order subrange will be
marked as the new highest order subrange for subsequent
comparisons and the search continues by branching to the
other path. The search alternates between the two paths until
the lowest order subrange has been adjusted and a match has
been achieved.

[0022] In the first path, the search value is greater than or
not less than the target value. Beginning with the lowest
order subrange, the subrange is set to its minimum value and
the resulting new search value is compared against the target
value. This process is repeated with higher order subranges until a) the highest subrange is reached or b) the
search value is no longer greater than the target value. If the
search value is still greater than the target value when the
highest order subrange is reached, then the highest order
subrange is decremented until the search value is no longer
greater than the target value or until the highest order
subrange reaches its minimum value, whichever occurs first.
In either case, the highest order subrange has been set to its
correct value. If the search value becomes less than or no
longer greater than the target value, the next lower subrange
is marked as the new highest order subrange for subsequent
comparisons and the search branches to a second path. If the
search value becomes less than or no longer greater than the
target value before the highest order subrange is reached,
then all of the higher order subranges have been already set
to their correct value. The subrange whose change caused
the search value to no longer be greater than the target value
is marked as the new highest order subrange and the search
branches to the second path. If all subranges become set to
their minimum values and the search value is still greater
than the target value then an underflow condition has been
detected and the search is ended.

[0023] In the second path, the search value is less than or
not greater than the target value. Beginning with the lowest
order subrange, set the subrange to its maximum value and
compare the resulting new search value against the target.
This process is repeated with higher order subranges until a) the highest order subrange is reached or b) the
search value is greater than or no longer less than the target value.
If the search value is still less than the target value when the
highest order subrange is reached, then the highest order
subrange is incremented until either the search value is no
longer less than the target value or the highest order
subrange reaches its maximum value. Either of these stopping
conditions is a result of the highest order subrange being set
to its correct value. If the search value is no longer less than
the target value, the next lower order subrange is marked as
the new highest order subrange and the search branches to
the first path. If the search value becomes greater than or not
less than the target value before the highest order subrange
is reached, then the subrange whose change caused this
condition is marked as the new highest order subrange and
the search branches to the first path. If all subranges become
set to their maximum value for ones, tens, hundreds, etc.,
the search continues in this loop until the search index i is equal to the
highest order subrange index HOS at 130 or until the search
value is no longer less than the target value. If the search
value is not greater than the target value, the control flows to
116 where the highest order subrange index HOS is set equal to
the search index i.

[0024] One embodiment of the algorithm 100 can gener-
ally be described with reference to FIG. 1. Initialization
occurs at 102 where the lowest order subrange index LOS is
set equal to zero and the number of subranges N is selected.
The highest order subrange index HOS is set equal to N-1,
or one less than the number of subranges, in 104. The search
index i is set equal to the lowest order subrange index LOS
at 106.

[0025] A search value is compared to a target value at 108.
If the search value is greater than the target value, then the
search proceeds along a first search path by comparing the
search index i to the highest order subrange index HOS at
130. If the search index i is not equal to the highest order
subrange index HOS, then the value of the subrange indexed
by i is set to its minimum value and the search index i is
incremented at 132. The new search value resulting from
the operation at 132 is then compared to the target value at
134, and if the search value is greater than the target value
then the comparison at 130 is performed again. The search
will continue in this loop until the search index i is equal to the
highest order subrange index HOS at 130 or until the search
value is not greater than the target value at 134. If the search
value is not greater than the target value at 134, then the
control flows to 116 where the highest order subrange index
HOS is set equal to the search index i.

[0026] If the search index i is equal to the highest order
subrange index HOS at 130, then all the lower order
subranges have been set to their minimum values and it is
necessary to decrease the value of the highest order subrange
until the search value is not greater than the target value.
The search continues at 138 by comparing the value of subrange
indexed by the search index i to its minimum value. If the
value of the subrange is not equal to its minimum value, then
the value of the subrange is decremented at 140. The new
search value resulting from the operation at 140 is compared
to the target value at 142. If the search value is not greater
than the target value at 142, then the control flows back to
the comparison at 138. If the search value is not greater than
the target value at 142 then the correct value for the subrange
indexed by the highest order subrange index HOS has been
found and the control flows to 126.
[0027] If the subrange indexed by the search value i is equal to its minimum value at 138 then an underflow condition has been detected and the control flows to 144. This underflow results from the following conditions being met: 1) the highest order subrange being compared at 138 equals its minimum value, 2) the lower order subranges all equal their minimum values, 3) the search value is greater than the target value. Since the first two of these conditions indicate that the search value is set to its minimum value, it is not possible to decrease the search value further to make it match the target value. From this point control flows to 148.

[0028] Returning focus to the original comparison at 108, if the search value is less than the target value, then the search proceeds along a second search path by comparing the search index i to the highest order subrange index HOS at 110. If the search index i is not equal to the highest order subrange index HOS, then the value of the subrange indexed by i is set to its maximum value and the search index i is incremented at 112. The new search value resulting from the operation at 112 is then compared to the target value at 114, and if the search value is not greater than the target value then the comparison at 110 is performed again. The search will continue in this loop until the search index i is equal to the highest order subrange index HOS at 110 or until the search value is greater than the target value at 114. If the search value is greater than the target value at 114, then the control flows to 116 where the highest order subrange index HOS is set equal to the search index i.

[0029] If the search index i is equal to the highest order subrange index HOS at 110, then all the lower order subranges have been set to their maximum values and it is necessary to decrease the value of the highest order subrange until the search value is greater than the target value. The search continues at 118 by comparing the value of the subrange indexed by the search index i to its maximum value. If the value of the subrange is not equal to its maximum value, then the value of the subrange is incremented at 120. The new search value resulting from the operation at 120 is compared to the target value at 122. If the search value is not greater than the target value at 122, then the control flows back to the comparison at 118. If the search value is greater than the target value at 122 then the correct value for the subrange indexed by the highest order subrange index HOS has been found and the control flows to 126.

[0030] If the subrange indexed by the search value i is equal to its maximum value at 118 then an overflow condition has been detected and the search control flows to 124. This overflow results from the following conditions being met: 1) the highest order subrange being compared at 118 equals its maximum value, 2) the lower order subranges all equal their maximum values, 3) the search value is not greater than the target value. Since the first two of these conditions indicate that the search value is set to its maximum value, it is not possible to increase the search value further to make it match the target value. From this point control flows to 148.

[0031] In the comparison at 126, if the highest order subrange HOS and the lowest order subrange index LOS are equal, then all the subranges have been set to the values that cause the search value to match the target value. From here the control flows to 148. If the highest order subrange index HOS does not equal the lowest order subrange index LOS at 126, then it is necessary to continue the search to find the correct setting for at least one lower order subrange. The control flows to 128 where the search index i is decremented and the highest order subrange index HOS is set equal to this new value of i, indexing the next lower subrange.

[0032] Setting the highest order subrange index HOS to a new value, either at 116 or at 128, marks the successful completion of the current search path control flows to 106 where the search index i is set equal to the lowest order subrange index LOS. Following this the search value is compared to the target value at 108. At the successful completion of the first path, the search value will not be greater than the target value so the control flows to the second path at 110. Likewise, at the completion of the second path, the search value will be greater than the target value so the control flows to the first path at 130. Thus the search alternates between the two search paths until a solution is obtained.

[0033] Once a solution has been found, or an underflow or overflow condition has been detected, control flows to 148. At this point the results of the search are stored and control flows to 104 in preparation for a new search to begin.

[0034] The embodiment described above has several advantages. First, it rapidly converges to the target value. Second, the individual operations map easily into the instruction set of inexpensive microprocessors, which makes this an attractive method of identifying a target value in a range of values in inexpensive consumer products.

[0035] The dynamic operation of one embodiment of a system embodying the method of FIG. 1 and described above is best understood by studying Tables 1-4 that follow.

[0036] Tables 1-4 show in detail the progress through a system embodying the method illustrated in the flowchart of FIG. 1 for specific search and target values. For example, in Table 1, the initial search value is 4961 and the initial target value is 0375, and as can be seen in the beginning search value column the search starts with 4961 and ends with 375, which is the last entry in the ending search value column. Similarly, for Table 2, the initial search value is 1756 and the target value is 2104, for Table 3, the initial search value is 4961 and the target value is 375, and for Table 4, the initial search value is 1756 and the target value is 5104. References to path #1 refer to the “yes” branch out of decision block 108, and references to path #2 refer to the “no” branch out of decision block 108.

<table>
<thead>
<tr>
<th>TABLE 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lowest Order Subrange (LOS)- ONES</td>
</tr>
<tr>
<td>2nd LOS (LOS + 1)- TENS</td>
</tr>
<tr>
<td>3rd LOS (LOS + 2)- HUNDREDS</td>
</tr>
<tr>
<td>Highest Order Subrange (HOS)- THOUSANDS</td>
</tr>
<tr>
<td>EXAMPLE #1: Initial Search Value &gt; Target Value</td>
</tr>
<tr>
<td>Search Range: 0000-9999</td>
</tr>
<tr>
<td>Initial Search Value: 4961</td>
</tr>
<tr>
<td>Target Value: 0375</td>
</tr>
<tr>
<td>Beginning Value: 4961</td>
</tr>
<tr>
<td>Ending Value: 4960</td>
</tr>
<tr>
<td>Comments</td>
</tr>
<tr>
<td>4961</td>
</tr>
<tr>
<td>4960</td>
</tr>
<tr>
<td>4900</td>
</tr>
<tr>
<td>4900</td>
</tr>
<tr>
<td>4900</td>
</tr>
<tr>
<td>3900</td>
</tr>
</tbody>
</table>
### TABLE 1-continued

<table>
<thead>
<tr>
<th>2000</th>
<th>1000</th>
<th>Dec HOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>0000</td>
<td>Dec HOS</td>
</tr>
<tr>
<td>0000</td>
<td>0009</td>
<td>LOS set to max.</td>
</tr>
<tr>
<td>0009</td>
<td>0099</td>
<td>LOS + 1 set to max.</td>
</tr>
<tr>
<td>0099</td>
<td>0199</td>
<td>Inc LOS + 2</td>
</tr>
<tr>
<td>0199</td>
<td>0299</td>
<td>Inc LOS + 2</td>
</tr>
<tr>
<td>0299</td>
<td>0399</td>
<td>Inc LOS + 2</td>
</tr>
<tr>
<td>0399</td>
<td>0390</td>
<td>LOS set to min.</td>
</tr>
<tr>
<td>0390</td>
<td>0380</td>
<td>Dec LOS + 1</td>
</tr>
<tr>
<td>0380</td>
<td>0370</td>
<td>Dec LOS + 1</td>
</tr>
<tr>
<td>0370</td>
<td>0371</td>
<td>Inc LOS</td>
</tr>
<tr>
<td>0371</td>
<td>0372</td>
<td>Inc LOS</td>
</tr>
<tr>
<td>0372</td>
<td>0373</td>
<td>Inc LOS</td>
</tr>
<tr>
<td>0373</td>
<td>0374</td>
<td>Inc LOS</td>
</tr>
<tr>
<td>0374</td>
<td>0375</td>
<td>Inc LOS</td>
</tr>
<tr>
<td>0375</td>
<td>0399</td>
<td>Search = Target, end.</td>
</tr>
</tbody>
</table>

#### [0037]

### TABLE 2

<table>
<thead>
<tr>
<th>Lowest Order Subrange (LOS)</th>
<th>ONES</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd LOS (LOS + 1)</td>
<td>TENS</td>
</tr>
<tr>
<td>3rd LOS (LOS + 2)</td>
<td>HUNDREDS</td>
</tr>
</tbody>
</table>

| Highest Order Subrange (HOS) | THOUSANDS |

<table>
<thead>
<tr>
<th>EXAMPLE #2 Initial Search Value</th>
<th>&lt; Target Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Search Range: 0000–9999</td>
<td>Initial Search Value: 1756</td>
</tr>
<tr>
<td>Target Value: 2104</td>
<td>Beginning Ending</td>
</tr>
<tr>
<td>Value</td>
<td>Search</td>
</tr>
<tr>
<td>-------</td>
<td>--------</td>
</tr>
<tr>
<td>1756</td>
<td>1759</td>
</tr>
<tr>
<td>1759</td>
<td>1799</td>
</tr>
<tr>
<td>1799</td>
<td>1999</td>
</tr>
<tr>
<td>1999</td>
<td>2999</td>
</tr>
<tr>
<td>2999</td>
<td>2990</td>
</tr>
<tr>
<td>2990</td>
<td>2900</td>
</tr>
<tr>
<td>2900</td>
<td>2800</td>
</tr>
<tr>
<td>2800</td>
<td>2700</td>
</tr>
<tr>
<td>2700</td>
<td>2600</td>
</tr>
<tr>
<td>2600</td>
<td>2500</td>
</tr>
<tr>
<td>2500</td>
<td>2400</td>
</tr>
<tr>
<td>2400</td>
<td>2300</td>
</tr>
<tr>
<td>2300</td>
<td>2200</td>
</tr>
<tr>
<td>2200</td>
<td>2100</td>
</tr>
<tr>
<td>2100</td>
<td>2109</td>
</tr>
</tbody>
</table>

### [0038]

### TABLE 3

<table>
<thead>
<tr>
<th>Lowest Order Subrange (LOS)</th>
<th>ONES</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd LOS (LOS + 1)</td>
<td>TENS</td>
</tr>
<tr>
<td>3rd LOS (LOS + 2)</td>
<td>HUNDREDS</td>
</tr>
</tbody>
</table>

| Highest Order Subrange (HOS) | THOUSANDS |

<table>
<thead>
<tr>
<th>EXAMPLE #3 Target Value &lt; Min Range Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Search Range: 1000–4999</td>
</tr>
<tr>
<td>Target Value: 0375</td>
</tr>
<tr>
<td>Beginning</td>
</tr>
<tr>
<td>Value</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>4961</td>
</tr>
<tr>
<td>4960</td>
</tr>
<tr>
<td>4900</td>
</tr>
<tr>
<td>4000</td>
</tr>
<tr>
<td>3000</td>
</tr>
<tr>
<td>2000</td>
</tr>
<tr>
<td>1000</td>
</tr>
<tr>
<td>0399</td>
</tr>
</tbody>
</table>

### [0039]

### TABLE 4

<table>
<thead>
<tr>
<th>Lowest Order Subrange (LOS)</th>
<th>ONES</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd LOS (LOS + 1)</td>
<td>TENS</td>
</tr>
<tr>
<td>3rd LOS (LOS + 2)</td>
<td>HUNDREDS</td>
</tr>
</tbody>
</table>

| Highest Order Subrange (HOS) | THOUSANDS |

<table>
<thead>
<tr>
<th>EXAMPLE #4 Target Value &gt; Max Range Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Search Range: 1000–4999</td>
</tr>
<tr>
<td>Initial Search Value: 1756</td>
</tr>
<tr>
<td>Target Value: 5104</td>
</tr>
<tr>
<td>Beginning</td>
</tr>
<tr>
<td>Value</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>1756</td>
</tr>
<tr>
<td>1759</td>
</tr>
<tr>
<td>1799</td>
</tr>
<tr>
<td>1999</td>
</tr>
<tr>
<td>2999</td>
</tr>
<tr>
<td>2990</td>
</tr>
<tr>
<td>2900</td>
</tr>
<tr>
<td>2800</td>
</tr>
<tr>
<td>2700</td>
</tr>
<tr>
<td>2600</td>
</tr>
<tr>
<td>2500</td>
</tr>
<tr>
<td>2400</td>
</tr>
<tr>
<td>2300</td>
</tr>
<tr>
<td>2200</td>
</tr>
<tr>
<td>2100</td>
</tr>
<tr>
<td>2109</td>
</tr>
<tr>
<td>2108</td>
</tr>
<tr>
<td>2107</td>
</tr>
<tr>
<td>2106</td>
</tr>
<tr>
<td>2105</td>
</tr>
<tr>
<td>2104</td>
</tr>
</tbody>
</table>

### ONE EMBODIMENT OF THE GENERAL ALGORITHM TO IMPEDANCE MATCHING

[0040] The present invention has practical applications in many types of electronic systems. In one application, the present invention may be embodied in memory devices such as static random access memories (SRAM’s), as part of a memory package such as single in line memory modules (SIMM’s) or dual in line memory modules (DIMM’s). As additional SIMM’s or DIMM’s are added to motherboards...
of computer systems, the characteristic impedance of the memory bus may change. The present invention allows for the adaptation to changes in the impedance on a memory bus when new memory is added to or removed from the bus by dynamically matching the bus driver impedance with the resulting bus impedance.

[0041] Referring to FIG. 1A, impedance matching system 1, in one embodiment of the present invention, comprises voltage source 5, first signal line 10, second signal line 20, and controllable impedance 25. First signal line 10 is connected to second signal line 20, and controllable impedance 25 is connected between voltage source 5 and first signal line 10 and second signal line 20.

[0042] Signal line 10 and signal line 20 are transmission devices capable of carrying electronic signals. For example, signal line 10 and signal line 20 can be signal carrying lines in an integrated circuit or a memory device, a conductive wire, a wiring pattern on a system board, a strip line, or a coaxial cable. In addition, signal line 10 and signal line 20 need not be the same type of transmission device, nor need they exist in the same electronic subsystem. For example, signal line 10 can be a signal carrying line in an integrated circuit, while signal line 20 can be a coaxial cable connected to the signal carrying line in the integrated circuit.

[0043] Controllable impedance 25 is an electronic device having an impedance or a resistance that can be controlled. In one embodiment, controllable impedance 25 comprises a plurality of parallel resistor-transistor pairs. The parallel resistor-transistor pairs define a resistance ladder, and by switching on a transistor in one of the resistor-transistor pairs, a resistor is added to the resistance ladder. After the first resistor is added to the ladder, adding additional resistors to the resistor ladder by turning on a transistor decreases the resistance of the controllable impedance. A parallel arrangement of resistor-transistor pairs is shown in FIG. 2C and is described in more detail below.

[0044] In an alternate embodiment, controllable impedance 25 comprises a transistor that has a controllable impedance or resistance. For example, a metal-oxide-semiconductor (MOSFET) transistor is an electronic device that has a resistance that can be controlled.

[0045] Voltage source 5 can be selected to provide an appropriate value for controllable impedance 25. If controllable impedance 25 requires a positive voltage source to operate, then a positive voltage is selected for voltage source 5. If controllable impedance 25 requires a negative voltage source to operate, then a negative voltage is selected for voltage source 5. In addition voltage source 5 can be powered from a source of voltage, which is often referred to as a system voltage and designated as $V_{CC}$ or $V_{DD}$.

[0046] Impedance matching system 1 ensures that information signals originating on signal line 10 are not reflected back along signal line 10 as they are transmitted to signal line 20. Controllable impedance 25 is dynamically changed to match the impedance of signal line 10 to the impedance of signal line 20. This dynamic matching eliminates reflections at the point where signal line 10 is connected to signal line 20.

AN ALTERNATE EMBODIMENT OF THE GENERAL ALGORITHM TO IMPEDANCE MATCHING

[0047] Referring to FIG. 1B, impedance matching system 100, in one embodiment of the present invention, comprises voltage source 105, external pin 110 having a pin voltage and a pin circuit impedance, and signal source 120 having signal source impedance 130, variable impedance 140, and control system 150 having a first input port, a second input port and an output port. Variable impedance 140 couples voltage source 105 to the external pin 110. The first input port of control system 150 is coupled to voltage source 105, the second input port of control system 150 is coupled to external pin 110, and the output signal of control system 150 is coupled to variable impedance 140. Signal source 120 is also coupled to external pin 110. External pin 110 may be an input pin, an output pin, or a bidirectional input-output (I/O) pin, which is suitable for use with a tristate device.

[0048] Variable impedance 140, in one embodiment of the present invention, is a metal-oxide-semiconductor field-effect transistor (MOSFET), which is controlled by the control system 150 to adjust the impedance on input-output (I/O) pin 110. Both n-type and p-type metal-oxide semiconductor field-effect transistors are suitable for use in connection with the present invention, and can be configured with an appropriate voltage source, either positive or negative. FIGS. 2A and 2B show a diagram of a MOSFET suitable for use in the present invention and a family of MOSFET curves showing drain current versus drain-to-source voltage for various gate-to-source voltages. Those skilled in the art will recognize that the voltage between the gate and source terminals of a MOSFET can be used to control the impedance between the drain and source terminals. For example, referring to FIG. 2A, MOSFET 200 comprises gate terminal 205, source terminal 210, drain terminal 215, drain current $I_D$ 220, and drain-to-source voltage, $V_{DS}$ 225. A voltage between gate terminal 205 and source terminal 210 can control the impedance between drain terminal 215 and source terminal 210.

[0049] The relationship between the drain-to-source voltage, $V_{DS}$ 225, and the drain current, $I_D$ 220, of FIG. 2A, is shown in FIG. 2B. Graph 230 in FIG. 2B comprises x-axis 235, y-axis 240, and a family of conductance curves 245. X-axis 235 represents the drain-to-source voltage, $V_{DS}$ 225, and y-axis 240 represents the drain current, $I_D$ 220, for MOSFET 200 of FIG. 2A. A family of conductance curves 245 shows the drain current, $I_D$ 220, versus the drain-to-source voltage, $V_{DS}$ 225, for MOSFET 200 of FIG. 2A having a range of gate-to-source voltages. Those skilled in the art will recognize that for MOSFET 200 of FIG. 2A, the slope of each of the conductance curves in the family of conductance curves 245 of FIG. 2B, can be varied by varying the gate-to-source voltage, and thereby changing the conductance between the drain and source terminals of MOSFET 200. Using a MOSFET as a variable impedance permits a broad range of impedance values to be easily obtained.

[0050] Variable impedance 140, in an alternate embodiment of the present invention, is a parallel arrangement of serially connected resistor-transistor pairs coupling voltage source 105 to external pin 110. Those skilled in the art will recognize that the resistance of the parallel arrangement of
the serially connected resistor-transistor pairs is controlled by switching each transistor on or off in order to either include the resistor in the circuit or exclude the resistor from the circuit.

[0051] Referring to FIG. 2C, a parallel arrangement of a plurality of serially connected resistor-transistor pairs comprising transistor 250, transistor 255, resistor 260, and resistor 265 is shown. Also shown are control lines 275, external pin 280, and internal input/output (I/O) signal 285. The transistor selected for use in each resistor-transistor pair is not critical to the practice of the invention. Any transistor capable of functioning as a switch is suitable for use in practicing the invention. The resistor value for each resistor-transistor pair is selected based on the impedances of the signal source in the system. If the impedance of the signal source varies over a wide range of values, then a weighted set of resistor values is preferred. If the impedance of the signal source varies over a narrow range of values, then a set of resistors having the same value is preferred.

[0052] Referring again to FIG. 1B, an advantage of using a parallel arrangement of serially connected resistor-transistor pairs is that the impedance between the V SOURCE voltage 105 and the external pin 110 is capable of being digitally controlled, and a digitally controlled variable impedance 140 is easily coupled to control system 150. Another advantage of using a parallel arrangement of serially connected resistor-transistor pairs is that variable impedance 140 can be implemented in a variety of semiconductor technologies, since the transistor is only required to function as a switch.

AN EMBODIMENT OF A CONTROL SYSTEM FOR USE WITH THE GENERAL ALGORITHM

[0053] FIG. 3 shows a block diagram of one embodiment of a control system 300 suitable for use in the present invention. Control system 300 comprises voltage reduction circuit 305, comparator 310, state logic system 315, coarse counter 320, and fine counter 325. Voltage reduction circuit 305 receives V SOURCE sense signal 330, which carries the voltage V SOURCE 105 of FIG. 1B. Comparator 310 receives an output signal from voltage reduction circuit 305 and external pin sense signal 335, which carries the voltage present at external pin 110 of FIG. 1B. State logic system 315 receives an output signal from comparator 310, an output signal from coarse counter 320 and an output signal from fine counter 325. Coarse counter 320 and fine counter 325 receive output signals from state logic system 315. The output signals of coarse counter 320 and fine counter 325 are combined to create control signal 340, which can be used to increment or decrement the value of variable impedance 140 of FIG. 1B. An embodiment of an algorithm that defines the operation state logic system 315, coarse counter 320, and fine counter 325 is shown in FIG. 4A and FIG. 4B.

[0054] Referring again to FIG. 1B, in operation control system 150 is capable of sensing V SOURCE voltage 105 and the pin voltage at external pin 110 and of driving variable impedance 140 to a value that maintains the pin voltage at external pin 110 at a value equal to one-half the value of V SOURCE voltage 105. When control system 150 achieves this result, the pin circuit impedance at external pin 110 matches signal source impedance 130.

[0055] Referring again to FIG. 3, in operation state logic system 315 generates count up and count down signals that are coupled to the input port of coarse counter 320 and the input port of fine counter 325 in order to generate control signal 340, which, when connected to variable impedance 140 of FIG. 1B is capable of increasing and decreasing variable impedance 140 of FIG. 1B. State logic system 315 responds to the outputs of coarse counter 320, fine counter 325, and the output of comparator 310 to count up or count down coarse counter 320 and to count up or count down fine counter 325. In one embodiment, comparator 310 generates an output signal that indicates to state logic system 315 whether the output signal from voltage reduction circuit 305 is greater than or less than external pin sense signal 345. The speed of comparator 310 is not critical to the practice of the present invention. Voltage reduction circuit 305, which in one embodiment can be a non-inverting amplifier, scales V SOURCE sense signal 330 by a factor of one-half. The output signal of voltage reduction circuit 305 is coupled to an input port of comparator 310.

[0056] Those skilled in the art will recognize that, in another embodiment of the present invention, a microprocessor can be substituted for state logic system 315, coarse counter 320, and fine counter 325. The flow diagram of FIG. 4A and FIG. 4B defines the operation of state logic system 315 in combination with coarse counter 320 and fine counter 325. This flow diagram can be reduced to a computer program, which can be executed on a microprocessor. Since the flow diagram is composed of a small number of simple comparisons and assignments arranged in tight loops, a microprocessor having small instruction set is suitable for use in the present invention.

AN EMBODIMENT OF THE GENERAL ALGORITHM USING COUNTERS

[0057] Referring to FIG. 4A and FIG. 4B, in one embodiment of the present invention, an impedance matching algorithm 400 defines the logical operation of state logic system 315, coarse counter 320, and fine counter 325 of FIG. 3 or a microprocessor.

[0058] The operation of the flow diagram of FIG. 4A and FIG. 4B is best understood by assuming values for the external pin voltage of FIG. 1B, V PIN and the voltage source of FIG. 1B, V SOURCE 105, which is designated as V CC in FIG. 4A and FIG. 4B, and tracing a path through the flow diagram. Impedance matching algorithm 400 shown in FIG. 4A and FIG. 4B begins at decision block 410.

[0059] At decision block 410, V PIN is compared to V CC/2. If the pin voltage is greater than V CC/2, then fine counter 325 is set to zero. If V PIN is not greater than V CC/2, then fine counter 325 is set to its maximum value.

[0060] Assuming that V PIN is greater than V CC/2, the algorithm is prepared to consider executing branch 415 and branch 420. For V greater than V CC/2, the strategy of the algorithm in branch 415 and branch 420 is to decrement coarse counter 320 until V PIN is less than V CC/2, and to then increment fine counter 325 until V PIN equals V CC/2. When V PIN equals V CC/2, the pin circuit impedance matches the signal source impedance. However, if after zeroing fine counter 325, V PIN is not greater than V CC/2, then coarse counter 320 need not be adjusted and only fine counter 325 is adjusted, incremented until it reaches its maximum value or until V PIN equals V CC/2.
Assuming that $V_{PIN}$ is not greater than $V_{CC}/2$, the algorithm is prepared to consider executing branch 425 and branch 430. For $V_{PIN}$ not greater than $V_{CC}/2$, the strategy of the algorithm in branch 425 and branch 430 is to increment coarse counter 320 until $V_{PIN}$ is greater than $V_{CC}/2$ and to then decrement fine counter 325 until $V_{PIN}$ equals $V_{CC}/2$. When $V_{PIN}$ equals $V_{CC}/2$, the pin circuit impedance matches the signal source impedance. However, if after setting fine counter 325 to all ones, $V_{PIN}$ is greater than $V_{CC}/2$, then coarse counter 320 need not be adjusted and only fine counter 325 is adjusted, decremented until it reaches its minimum value or until $V_{PIN}$ equals $V_{CC}/2$.

CONCLUSION

The present invention has practical applications in many types of electronic systems. In one application, the present invention may be embodied in memory devices such as static random access memories (SRAM’s), as part of a memory package such as single in line memory modules (SIMM’s) or dual in line memory modules (DIMM’s). As additional SIMM’s or DIMM’s are added to motherboards of computer systems, the characteristic impedance of the memory bus may change. The present invention allows for the adaptation to changes in the characteristic impedance on a memory bus when new memory is added to or removed from the bus by dynamically matching the bus driver impedance with the resulting bus impedance.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A method comprising:
   selecting a search value having a plurality of subranges;
   selecting a target value; and
   repeatedly altering at least one of the plurality of subranges until the search value matches the target value and storing the search value.

2. The method of claim 1, further comprising:
   repeatedly comparing the search value to the target value.

3. The method of claim 2, wherein repeatedly altering at least one of the plurality of subranges until the search value matches the target value comprises:
   incrementing and decrementing the plurality of subranges in a counter until the search value matches the target value.

4. A method comprising:
   selecting a search value having a plurality of subranges;
   selecting a target value; and
   repeatedly altering at least one of the plurality of subranges until an underflow condition is detected and recording the underflow condition.

5. A method comprising:
   selecting a search value having a plurality of subranges;
   selecting a target value; and
   repeatedly altering at least one of the plurality of subranges until an overflow condition is detected and recording the overflow condition.

6. A system comprising:
   a counter unit representing a search value having a plurality of subranges;
   a register unit containing a target value; and
   a control unit operably coupled to the counter unit and the register unit and capable of repeatedly altering at least one of the plurality of subranges until a physically recordable condition selected from the group consisting of a match, an overflow, and an underflow occurs.

7. The system of claim 6, further comprising:
   a comparison unit operably coupled to the counter unit and the register unit and the comparison unit capable of repeatedly comparing the counter unit to the register unit.

8. An impedance matching circuit, comprising:
   a first signal line;
   a second signal line having a characteristic impedance and connected to the first signal line; and
   a controllable impedance connected to the first signal line and the second signal line and operable for dynamically matching the characteristic impedance on the second signal line.

9. The impedance matching circuit of claim 8, wherein the controllable impedance comprises a plurality of parallel resistors arranged to provide discrete steps of impedance on the second signal line.

10. The impedance matching circuit of claim 8, wherein the controllable impedance is a controlled transistor connected between the second signal line and a source of voltage.

11. The impedance matching circuit of claim 10, wherein the source of voltage is positive.

12. The impedance matching circuit of claim 10, wherein the source of voltage is negative.

13. The impedance matching circuit of claim 8, wherein the controllable impedance includes a circuit connected to the second signal line for sensing the characteristic impedance looking into the second signal line and for adjusting the controllable impedance in response thereto.

14. An impedance matching circuit, comprising:
   an internal signal line;
   an external signal line having an impedance and connected to the internal signal line; and
   a controllable impedance connected between the external signal line and a power source and operable for dynamically matching the impedance on the external signal line.

15. The impedance matching circuit of claim 14, wherein the controllable impedance comprises:
   a plurality of switched resistors connected between the power source and the external signal line; and
a state machine operable for switching selected ones of the plurality of switched resistors.

16. The impedance matching circuit of claim 14, wherein the controllable impedance comprises:

a controlled transistor connected between the external signal line and a source of voltage; and

a control circuit connected to the controlled transistor and operable for controlling the impedance on the external signal line.

17. The impedance matching circuit of claim 16, wherein the control circuit is connected to the external signal line for sensing a first impedance looking into the external signal line and dynamically changing the impedance looking out of the external signal line.

18. A dynamic impedance matching circuit, comprising:

an internal signal line;

an external pin connected to the internal signal line;

a controllable impedance device connected between a voltage source and the external pin; and

a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.

19. An impedance matching system for an external pin on a integrated circuit, comprising:

an internal signal line connected to the external pin;

a controllable impedance circuit device connected between a voltage source and the external pin; and

a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.

20. A variable resistance circuit for matching a reflection from an external signal connected to a pin, comprising:

an internal signal connected to the pin;

a controllable resistance connected between the pin and a voltage source; and

a sense circuit connected to the controllable resistance and the pin and operable for changing the controllable resistance to minimize the reflection.

21. An impedance matching system, comprising:

a variable impedance capable of coupling a source voltage to an external pin having a pin voltage and a pin circuit impedance, and the external pin coupled to a signal source having a signal source impedance, the variable impedance is capable of matching a pin circuit impedance to a signal source impedance; and

a control system coupled to the variable impedance, to the source voltage, and to the external pin, the control system is capable of sensing the pin voltage, capable of sensing the source voltage, and capable of continuously controlling the variable impedance in response to changes in the source voltage and the pin voltage in order to control the pin voltage to one-half the source voltage.

22. The impedance matching system of claim 21, wherein the variable impedance is a metal-oxide semiconductor field effect transistor (MOSFET) having a gate, a drain, and a source.

23. The impedance matching system of claim 21, wherein the variable impedance is a resistor-transistor pair.

24. The impedance matching system of claim 21, wherein the signal source is a memory cell.

25. The impedance matching system of claim 24, wherein the memory cell is included in a memory device.

26. The impedance matching system of claim 25, wherein the memory device is included in a system.

27. An impedance matching system, comprising:

a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a signal source having a signal source impedance coupled to the external pin, the variable impedance is capable of matching the pin circuit impedance to the signal source impedance;

a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;

a comparator coupled to the pin voltage and the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage; and

a microprocessor capable of continuously controlling the impedance of the variable impedance in order to control the pin voltage to one-half the source voltage, the microprocessor is coupled to the comparator and the variable impedance.

28. The impedance matching system of claim 27, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

29. The impedance matching system of claim 27, wherein the variable impedance is a resistor-transistor pair.

30. The impedance matching system of claim 27, wherein the signal source is a memory cell.

31. The impedance matching system of claim 30, wherein the memory cell is included in a memory device.

32. The impedance matching system of claim 31, wherein the memory device is included in a system.

33. An impedance matching system, comprising:

a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a signal source coupled to the external pin and the signal source having a signal source impedance, the variable impedance is capable of matching the pin circuit impedance to the signal source impedance;

a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;

a comparator coupled to the pin voltage and the voltage reduction circuit to receive the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage;

a coarse counter having a coarse counter input port and a coarse counter output port, the coarse counter output signal is coupled to the variable impedance, and the coarse counter is capable of increasing or decreasing the variable impedance;
a fine counter having a fine counter input port and a fine counter output signal, the fine counter output signal is coupled to the variable impedance, and the fine counter is capable of increasing or decreasing the variable impedance; and

a state logic system coupled to the comparator, the coarse counter output signal the fine counter output signal, the coarse counter input port, and the fine counter input port, the state logic system is capable of continuously controlling the variable impedance in order to control the pin voltage to one-half the source voltage.

34. The impedance matching system of claim 33, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

35. The impedance matching system of claim 33, wherein the variable impedance is a resistor-transistor pair.

36. The impedance matching system of claim 33, wherein the signal source is a memory cell.

37. The impedance matching system of claim 36, wherein the memory cell is included in a memory device.

38. The impedance matching system of claim 37, wherein the memory device is included in a system.

39. An impedance matching circuit, comprising:

a circuit;

a first signal line connected to the circuit;

a second signal line having a characteristic impedance and connected to the first signal line; and

a controllable impedance connected to the first signal line and the second signal line and operable for dynamically matching the characteristic impedance on the second signal line.

40. The impedance matching circuit of claim 39, wherein the controllable impedance comprises a plurality of parallel resistors arranged to provide discrete steps of impedance on the second signal line.

41. The impedance matching circuit of claim 39, wherein the controllable impedance is a controlled transistor connected between the second signal line and a source of voltage.

42. The impedance matching circuit of claim 41, wherein the source of voltage is positive.

43. The impedance matching circuit of claim 41, wherein the source of voltage is negative.

44. The impedance matching circuit of claim 39, wherein the controllable impedance includes a circuit connected to the second signal line for sensing the characteristic impedance looking into the second signal line and for adjusting the controllable impedance in response thereto.

45. An impedance matching circuit, comprising:

a circuit;

a internal signal line connected to the circuit;

an external signal line having an impedance and connected to the internal signal line; and

a controllable impedance connected between the external signal line and a power source and operable for dynamically matching the impedance on the external signal line.

46. The impedance matching circuit of claim 45, wherein the controllable impedance comprises:

a plurality of switched resistors connected between the power source and the external signal line; and

a state machine operable for switching selected ones of the plurality of switched resistors.

47. The impedance matching circuit of claim 45, wherein the controllable impedance comprises:

a controlled transistor connected between the external signal line and a source of voltage; and

a control circuit connected to the controlled transistor and operable for controlling the impedance on the external signal line.

48. The impedance matching circuit of claim 47, wherein the control circuit is connected to the external signal line for sensing a first impedance looking into the external signal line and dynamically changing the impedance looking out of the external signal line.

49. A dynamic impedance matching circuit, comprising:

a circuit;

an internal signal line connected to the circuit;

an external pin connected to the internal signal line;

a controllable impedance device connected between a voltage source and the external pin; and

a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.

50. An impedance matching system for an external pin on an integrated circuit, comprising:

a circuit;

an internal signal line connected to the external pin and to the circuit;

an controllable impedance circuit device connected between a voltage source and the external pin; and

a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.

51. An impedance matching circuit, comprising:

a memory device;

a first signal line connected to the memory device;

a second signal line having a characteristic impedance and connected to the first signal line; and

a controllable impedance connected to the first signal line and the second signal line and operable for dynamically matching the characteristic impedance on the second signal line.

52. The impedance matching circuit of claim 51, wherein the controllable impedance comprises a plurality of parallel resistors arranged to provide discrete steps of impedance on the second signal line.

53. The impedance matching circuit of claim 51, wherein the controllable impedance is a controlled transistor connected between the second signal line and a source of voltage.
54. The impedance matching circuit of claim 53, wherein the source of voltage is positive.
55. The impedance matching circuit of claim 53, wherein the source of voltage is negative.
56. The impedance matching circuit of claim 51, wherein the controllable impedance includes a circuit connected to the second signal line for sensing the characteristic impedance looking into the second signal line and for adjusting the controllable impedance in response thereto.
57. An impedance matching circuit, comprising:
   a memory device;
   an internal signal line connected to the memory device;
   an external signal line having an impedance and connected to the internal signal line; and
   a controllable impedance connected between the external signal line and a power source and operable for dynamically matching the impedance on the external signal line.
58. The impedance matching circuit of claim 57, wherein the controllable impedance comprises:
   a plurality of switched resistors connected between the power source and the external signal line; and
   a state machine operable for switching selected ones of the plurality of switched resistors.
59. The impedance matching circuit of claim 57, wherein the controllable impedance comprises:
   a controlled transistor connected between the external signal line and a source of voltage; and
   a control circuit connected to the controlled transistor and operable for controlling the impedance on the external signal line.
60. The impedance matching circuit of claim 59, wherein the control circuit is connected to the external signal line for sensing a first impedance looking into the external signal line and dynamically changing the impedance looking out of the external signal line.
61. A dynamic impedance matching circuit, comprising:
   a memory device;
   an internal signal line connected to the memory device;
   an external pin connected to the internal signal line;
   a controllable impedance device connected between a voltage source and the external pin; and
   a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.
62. An impedance matching system for an external pin on a integrated circuit, comprising:
   a memory device;
   an internal signal line connected to the external pin and to the memory device;
   an controllable impedance circuit device connected between a voltage source and the external pin; and
   a control circuit connected to the external pin and operable for sensing an impedance looking out of the
63. An impedance matching circuit, comprising:
   an SRAM;
   a first signal line connected to the SRAM;
   a second signal line having a characteristic impedance and connected to the first signal line; and
   a controllable impedance connected to the first signal line and the second signal line and operable for dynamically matching the characteristic impedance on the second signal line.
64. The impedance matching circuit of claim 63, wherein the controllable impedance comprises a plurality of parallel resistors arranged to provide discrete steps of impedance on the second signal line.
65. The impedance matching circuit of claim 63, wherein the controllable impedance is a controlled transistor connected between the second signal line and a source of voltage.
66. The impedance matching circuit of claim 65, wherein the source of voltage is positive.
67. The impedance matching circuit of claim 65, wherein the source of voltage is negative.
68. The impedance matching circuit of claim 63, wherein the controllable impedance includes a circuit connected to the second signal line for sensing the characteristic impedance looking into the second signal line and for adjusting the controllable impedance in response thereto.
69. An impedance matching circuit, comprising:
   an SRAM;
   a internal signal line connected to the SRAM;
   an external signal line having an impedance and connected to the internal signal line; and
   a controllable impedance connected between the external signal line and a power source and operable for dynamically matching the impedance on the external signal line.
70. The impedance matching circuit of claim 69, wherein the controllable impedance comprises:
   a plurality of switched resistors connected between the power source and the external signal line; and
   a state machine operable for switching selected ones of the plurality of switched resistors.
71. The impedance matching circuit of claim 69, wherein the controllable impedance comprises:
   a controlled transistor connected between the external signal line and a source of voltage; and
   a control circuit connected to the controlled transistor and operable for controlling the impedance on the external signal line.
72. The impedance matching circuit of claim 71, wherein the control circuit is connected to the external signal line for sensing a first impedance looking into the external signal line and dynamically changing the impedance looking out of the external signal line.
73. A dynamic impedance matching circuit, comprising:
   an SRAM;
an internal signal line connected to the SRAM;
an external signal line connected to the internal signal line;
a controllable impedance device connected between a voltage source and the external pin; and
a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.
74. An impedance matching system for an external pin on an integrated circuit, comprising:
an SRAM;
an internal signal line connected to the external pin and to the SRAM;
an controllable impedance circuit device connected between a voltage source and the external pin; and
a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.
75. An impedance matching circuit, comprising:
a motherboard;
a first signal line connected to the motherboard;
a second signal line having a characteristic impedance and connected to the first signal line; and
a controllable impedance connected to the first signal line and the second signal line and operable for dynamically matching the characteristic impedance on the second signal line.
76. The impedance matching circuit of claim 75, wherein the controllable impedance comprises a plurality of parallel resistors arranged to provide discrete steps of impedance on the second signal line.
77. The impedance matching circuit of claim 75, wherein the controllable impedance is a controlled transistor connected between the second signal line and a source of voltage.
78. The impedance matching circuit of claim 77, wherein the source of voltage is positive.
79. The impedance matching circuit of claim 77, wherein the source of voltage is negative.
80. The impedance matching circuit of claim 75, wherein the controllable impedance includes a circuit connected to the second signal line for sensing the characteristic impedance looking into the second signal line and for adjusting the controllable impedance in response thereto.
81. An impedance matching circuit, comprising:
a motherboard;
an internal signal line coupled to the motherboard;
an external signal line having an impedance and connected to the internal signal line; and
a controllable impedance connected between the external signal line and a power source and operable for dynamically matching the impedance on the external signal line.
82. The impedance matching circuit of claim 81, wherein the controllable impedance comprises:
a plurality of switched resistors connected between the power source and the external signal line; and
a state machine operable for switching selected ones of the plurality of switched resistors.
83. The impedance matching circuit of claim 81 wherein the controllable impedance comprises:
a controlled transistor connected between the external signal line and a source of voltage; and
a control circuit connected to the controlled transistor and operable for controlling the impedance on the external signal line.
84. The impedance matching circuit of claim 83, wherein the control circuit is connected to the external signal line for sensing a first impedance looking into the external signal line and dynamically changing the impedance looking out of the external signal line.
85. A dynamic impedance matching circuit, comprising:
a motherboard;
an internal signal line coupled to the motherboard;
an external pin connected to the internal signal line;
an controllable impedance device connected between a voltage source and the external pin; and
a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.
86. An impedance matching system for an external pin on an integrated circuit, comprising:
a motherboard;
an internal signal line connected to the external pin and to the motherboard;
an controllable impedance circuit device connected between a voltage source and the external pin; and
a control circuit connected to the external pin and operable for sensing an impedance looking out of the external pin and for controlling the controllable impedance device to match the impedance.
87. An impedance matching system, comprising:
a variable impedance capable of coupling a source voltage to an external pin having a pin voltage and a pin circuit impedance, and the external pin coupled to a circuit signal source having a circuit signal source impedance, the variable impedance is capable of matching a pin circuit impedance to a signal source impedance; and
a control system coupled to the variable impedance, to the source voltage, and to the external pin, the control system is capable of sensing the pin voltage, capable of sensing the source voltage, and capable of continuously controlling the variable impedance in response to changes in the source voltage and the pin voltage in order to control the pin voltage to one-half the source voltage.
88. The impedance matching system of claim 87, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.
89. The impedance matching system of claim 87, wherein the variable impedance is a resistor-transistor pair.

90. An impedance matching system, comprising:
   a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a circuit signal source having a circuit signal source impedance coupled to the external pin, the variable impedance is capable of matching the pin circuit impedance to the signal source impedance;
   a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;
   a comparator coupled to the pin voltage and the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage; and
   a microprocessor capable of continuously controlling the impedance of the variable impedance in order to control the pin voltage to one-half the source voltage, the microprocessor is coupled to the comparator and the variable impedance.

91. The impedance matching system of claim 90, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

92. The impedance matching system of claim 90, wherein the variable impedance is a resistor-transistor pair.

93. An impedance matching system, comprising:
   a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a circuit signal source coupled to the external pin and the circuit signal source having a circuit signal source impedance, the variable impedance is capable of matching the pin circuit impedance to the circuit signal source impedance;
   a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;
   a comparator coupled to the pin voltage and the voltage reduction circuit to receive the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage;
   a coarse counter having a coarse counter input port and a coarse counter output signal, the coarse counter output signal is coupled to the variable impedance, and the coarse counter is capable of increasing or decreasing the variable impedance;
   a fine counter having a fine counter input port and a fine counter output signal, the fine counter output signal is coupled to the variable impedance, and the fine counter is capable of increasing or decreasing the variable impedance; and
   a state logic system coupled to the comparator, the coarse counter output signal the fine counter output signal, the coarse counter input port, and the fine counter input port, the state logic system is capable of continuously controlling the variable impedance in order to control the pin voltage to one-half the source voltage.

94. The impedance matching system of claim 93, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

95. The impedance matching system of claim 93, wherein the variable impedance is a resistor-transistor pair.

96. An impedance matching system, comprising:
   a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a circuit signal source having a circuit signal source impedance coupled to the external pin, the variable impedance is capable of matching the pin circuit impedance to the memory signal source impedance; and
   a control system coupled to the variable impedance, to the source voltage, and to the external pin, the control system is capable of sensing the pin voltage, capable of sensing the source voltage, and capable of continuously controlling the variable impedance in response to changes in the source voltage and the pin voltage in order to control the pin voltage to one-half the source voltage.

97. The impedance matching system of claim 96, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

98. The impedance matching system of claim 96, wherein the variable impedance is a resistor-transistor pair.

99. An impedance matching system, comprising:
   a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a memory signal source having a memory signal source impedance coupled to the external pin, the variable impedance is capable of matching the pin circuit impedance to the memory signal source impedance;
   a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;
   a comparator coupled to the pin voltage and the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage; and
   a microprocessor capable of continuously controlling the impedance of the variable impedance in order to control the pin voltage to one-half the source voltage, the microprocessor is coupled to the comparator and the variable impedance.

100. The impedance matching system of claim 99, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

101. The impedance matching system of claim 99, wherein the variable impedance is a resistor-transistor pair.

102. An impedance matching system, comprising:
   a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and a memory signal source coupled to the external pin and the memory signal source having a memory signal source impedance, the variable impedance is capable of matching the pin circuit impedance to the memory signal source impedance;
   a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;
   a comparator coupled to the pin voltage and the voltage reduction circuit to receive the one-half source voltage,
the comparator is capable of comparing the pin voltage to the one-half source voltage;
a coarse counter having a coarse counter input port and a coarse counter output signal, the coarse counter output signal is coupled to the variable impedance, and the coarse counter is capable of increasing or decreasing the variable impedance;
a fine counter having a fine counter input port and a fine counter output signal, the fine counter output signal is coupled to the variable impedance, and the fine counter is capable of increasing or decreasing the variable impedance;
a state logic system coupled to the comparator, the coarse counter output signal the fine counter output signal, the coarse counter input port, and the fine counter input port, the state logic system is capable of continuously controlling the variable impedance in order to control the pin voltage to one-half the source voltage.

103. The impedance matching system of claim 102, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

104. The impedance matching system of claim 102, wherein the variable impedance is a resistor-transistor pair.

105. An impedance matching system, comprising:
a variable impedance capable of coupling a source voltage to an external pin having a pin voltage and a pin circuit impedance, and the external pin coupled to an SRAM signal source having an SRAM signal source impedance, the variable impedance is capable of matching a pin circuit impedance to the SRAM signal source impedance; and
a control system coupled to the variable impedance, to the source voltage, and to the external pin, the control system is capable of sensing the pin voltage, capable of sensing the source voltage, and capable of continuously controlling the variable impedance in response to changes in the source voltage and the pin voltage in order to control the pin voltage to one-half the source voltage.

106. The impedance matching system of claim 105, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

107. The impedance matching system of claim 105, wherein the variable impedance is a resistor-transistor pair.

108. An impedance matching system, comprising:
a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and an SRAM signal source having a SRAM signal source impedance, the external pin coupled to the external pin, the variable impedance is capable of matching the pin circuit impedance to the SRAM signal source impedance;
a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;
a comparator coupled to the pin voltage and the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage; and
a microprocessor capable of continuously controlling the impedance of the variable impedance in order to control the pin voltage to one-half the source voltage, the microprocessor is coupled to the comparator and the variable impedance.

109. The impedance matching system of claim 108, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

110. The impedance matching system of claim 108, wherein the variable impedance is a resistor-transistor pair.

111. An impedance matching system, comprising:
a variable impedance capable of coupling a source voltage to an external pin having a pin circuit impedance and an SRAM signal source coupled to the external pin and the SRAM signal source having an SRAM signal source impedance, the variable impedance is capable of matching the pin circuit impedance to the SRAM signal source impedance;
a voltage reduction circuit coupled to the source voltage, the voltage reduction circuit is capable of generating a one-half source voltage;
a comparator coupled to the pin voltage and the voltage reduction circuit to receive the one-half source voltage, the comparator is capable of comparing the pin voltage to the one-half source voltage;
a coarse counter having a coarse counter input port and a coarse counter output signal, the coarse counter output signal is coupled to the variable impedance, and the coarse counter is capable of increasing or decreasing the variable impedance;
a fine counter having a fine counter input port and a fine counter output signal, the fine counter output signal is coupled to the variable impedance, and the fine counter is capable of increasing or decreasing the variable impedance; and
a state logic system coupled to the comparator, the coarse counter output signal the fine counter output signal, the coarse counter input port, and the fine counter input port, the state logic system is capable of continuously controlling the variable impedance in order to control the pin voltage to one-half the source voltage.

112. The impedance matching system of claim 111, wherein the variable impedance is a MOSFET having a gate, a drain, and a source.

113. The impedance matching system of claim 111, wherein the variable impedance is a resistor-transistor pair.

114. A method comprising:
sensing a source voltage and a pin circuit voltage at an external pin; and
continuously controlling a variable impedance, connected to the source voltage and the external pin, in response to the source voltage and the pin circuit voltage to maintain the pin circuit voltage at one-half the source voltage.

115. The method of claim 114, wherein sensing a source voltage and a pin circuit voltage at an external pin comprises:
sensing the source voltage with a voltage reduction circuit; and
sensing the pin circuit voltage with a comparator.

116. The method of claim 114, wherein continuously controlling a variable impedance, connected to the source voltage and the external pin, in response to the source voltage and the pin circuit voltage to maintain the pin circuit voltage at one-half the source voltage comprises:
receiving a digital comparison signal; and
digitally generating a control signal for continuously controlling the variable impedance.

117. A method comprising:
comparing a pin circuit voltage at an external pin to one-half of a source voltage to generate a comparison signal; and
continuously controlling a variable impedance, connected to the source voltage and the external pin, in response to the comparison signal to maintain the pin circuit voltage at one-half the source voltage.

118. The method of claim 117, continuously controlling a variable impedance, connected to the source voltage and the external pin, in response to the comparison signal to maintain the pin circuit voltage at one-half the source voltage comprises:

receiving a digital comparison signal; and
digitally generating a control signal for continuously controlling the variable impedance.

119. A method comprising:
sensing a source voltage;
generating a voltage signal that is one-half the source voltage;
comparing a pin circuit voltage signal to the voltage signal to generate a comparison signal;
adjusting a coarse counter having an output signal in response to the comparison signal;
adjusting a fine counter having an output signal in response to the comparison signal; and
controlling a variable impedance with the output signal of the coarse counter and the output signal of the fine counter to drive the pin circuit voltage signal to the generated voltage signal.

120. A method comprising:
sensing a source voltage;
generating a voltage signal that is one-half the source voltage;
comparing a pin circuit voltage signal to the voltage signal to generate a comparison signal;
adjusting a coarse counter variable having a value in response to the comparison signal;
adjusting a fine counter variable having a value in response to the comparison signal; and
controlling a variable impedance with the value of the coarse counter variable and the value of the fine counter variable to drive the pin circuit voltage signal to the generated voltage signal.

121. A method comprising:
comparing a pin circuit voltage to one-half of a source voltage to determine whether the pin circuit voltage is initially less than one-half of the source voltage;
incrementing a coarse counter to a value less than the pin circuit voltage, when the pin circuit voltage is initially greater than one-half of the source voltage; and
incrementing the fine counter until the value of the coarse counter and the fine counter equals one-half of the source voltage, when the pin circuit voltage is initially less than one-half of the source voltage.

decrementing a fine counter until the value of the coarse counter and the fine counter equals one-half of the source voltage, when the pin circuit voltage is initially less than one-half of the source voltage; and
incrementing the coarse counter to a value less than the pin circuit voltage, when the pin circuit voltage is initially greater than one-half of the source voltage; and
incrementing the fine counter until the value of the coarse counter and the fine counter equals one-half of the source voltage, when the pin circuit voltage is initially greater than one-half of the source voltage.

122. A method comprising:
comparing a pin circuit voltage to one-half of a source voltage to determine whether the pin circuit voltage is initially less than one-half of the source voltage;
incrementing a coarse counter variable to a value greater than one-half of the source voltage, when the pin circuit voltage is initially less than one-half of the source voltage;

123. A method for matching a search value to a target value in a range of values having a maximum value and a minimum value, in a system having a coarse counter and a fine counter representing the search value, the method comprising:
comparing the search value to the target value to determine whether the search value is initially less than the target value;
incrementing the coarse counter to a value greater than the target value, when the search value is initially less than the target value;

124. A method for matching a search value to a target value in a range of values having a maximum value and a minimum value, in a system having a coarse counter and a fine counter representing the search value, the method comprising:
comparing the search value to the target value to determine whether the search value is initially less than the target value;
incrementing the coarse counter to a value greater than the target value, when the search value is initially less than the target value; and