SEMICONDUCTOR INTEGRATED CIRCUIT HAVING TRANSISTORS FOR CUTTING-OFF SUBTHRESHOLD CURRENT

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ABSTRACT
A semiconductor integrated circuit which enables a sub-threshold current to be suppressed when a logic gate circuit group is nonactivated and enables the logic gate circuit group to be activated at a high speed is provided. The semiconductor integrated circuit has at least one logic gate circuit connected to a feed line, a first transistor serially connected to the feed line in order to suppress the subthreshold current flowing in the logic gate circuit upon nonactivation of the logic gate circuit and a second transistor which is connected in parallel to the first transistor. The second transistor is activated prior to activation of the logic gate circuit and the first transistor.
Fig. 2
Fig. 5

Diagram showing connections and components labeled with numbers and symbols.
SEMICONDUCTOR INTEGRATED CIRCUIT
HAVING TRANSISTORS FOR CUTTING-OFF
SUBTHRESHOLD CURRENT

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor integrated circuit, more particularly, to a semiconductor integrated circuit in which transistors for cutting-off a subthreshold current are added to feed lines and/or grounding lines which supply electrical potential to a logic gate circuit group in driving circuits of a semiconductor memory device.

[0003] 2. Description of the Related Art

[0004] In the conventional semiconductor integrated circuit, in accordance with forming a minute semiconductor element, a subthreshold current flowing when the element is turned off is a problem. The subthreshold current is a current which flows even when the element is turned off. If the subthreshold current is left as it is, an erroneous operation of the circuit or the like is caused.

[0005] For example, in a word driver of a semiconductor memory devices, a gate circuit having a large driving power is used to drive a word line, and an influence of the subthreshold current is large so that a problem such that a consumption of a current is increased is caused.

[0006] In order to solve the problem caused by the subthreshold current, as disclosed in IEEEJ Solid-State Circuit, vol. 28, No. 11, p.1105, November 1993, for instance, it is proposed that a transistor for cutting-off the subthreshold current is serially inserted to a feed line for applying a voltage to the semiconductor device element.

[0007] The conventional semiconductor integrated circuit to which the transistor for cutting-off the subthreshold current is added will now be described with reference to FIG. 5.

[0008] A semiconductor integrated circuit as shown in FIG. 5 is a selecting circuit of a word line in a dynamic random access memory (DRAM) and is constructed by: a word driver 600; a decoder 500; and transistors 511, 512, . . . , and 51n for cutting-off the subthreshold current (in the following, abbreviated to cut-off transistors). The word driver 600 is divided into n blocks 531, 532, . . . , and 53n. Each of the blocks is constructed of m driving circuits 5411 to 541m, 5421 to 542m, . . . , and 54n1 to 54nm each constructed of arbitrary logic circuits. Each of the outputs of the driving circuits 5411 to 541m, 5421 to 542m, . . . , and 54n1 to 54nm is connected to each word line of the DRAM. By activating one driving circuit in accordance with input address signals, one word line is selected. Each of the cut-off transistors 511, 512, . . . , and 51n is serially connected between a power source Vcc and each of feed lines 1.50, 1.51, . . . , and 1.5n of the blocks 531, 532, . . . , and 53n of the word driver. The decoder 500 decodes a part of input address signals, sets one of signals 01, 02, and φn to the low level, and sets one of the cut-off transistors 511, 512, . . . , and 51n into a driving state. Thus, a current is supplied to the feed line to which the driving circuit selected in accordance with the input address is connected.

[0009] According to the construction, when word driver 600 is inactivated, all of the cut-off transistors 511, 512, . . . , and 51n are turned off, so that no current flows through the feed lines 1.50, 1.51, . . . , and 1.5n. When the word driver 600 is activated, no current is supplied to non-selected blocks 5311, 5321, . . . , and 53n. Consequently, damage by the subthreshold current can be avoided.

[0010] However, in the conventional semiconductor integrated circuit as shown in FIG. 5, in a state where the cut-off transistors 511 to 51n are turned off and the word driver 600 is disconnected from the power source Vcc, there is a case where the subthreshold current flows in the word driver 600 and electric potentials of the feed lines 1.51 to 1.5n drop. In such a case, a problem such that the word driver 600 is activated slowly is caused. That is, for instance, in case when the inputted address signals are decoded and the driving circuit 5411 in the word driver 600 is selected, the level of an output φ1 of the decoder 500 becomes low. The cut-off transistor 511 is then turned on and, first, the feed line 1.50 is charged. After that, the driving circuit 5411 is operated. As mentioned above, a problem such that even if the decoding signal of the address signal is inputted to the word driver 600, the driving circuit cannot be operated promptly is caused.

SUMMARY OF THE INVENTION

[0011] It is an object of the invention to provide a semiconductor integrated circuit which can suppress a subthreshold current upon inactivation of a logic gate circuit group in a word driver or the like and can activate the logic gate circuit group at high speed.

[0012] A semiconductor integrated circuit of the present invention comprises:

[0013] a first feed line;
[0014] a second feed line;
[0015] a first power source line for applying a first electric potential to the first feed line;
[0016] at least one logic circuit connected between the first feed line and the second feed line and outputting a signal of a predetermined logic level in accordance with a logic level of an input signal;
[0017] a first transistor having a first conductivity and having a current path between the first power source line and the first feed line; and
[0018] a second transistor having the first conductivity and connected in parallel to the first transistor.

[0019] The first transistor is conductive state when the logic circuit is in an operation state and is non-conductive state when the logic circuit is in a standby state.

[0020] The second transistor is changed from a non-conductive state to a conductive state before the first transistor is changed from a non-conductive state to a conductive state.

[0021] A driving power of the first transistor is larger than that of the second transistor.

[0022] Further, a semiconductor integrated circuit of the present invention comprises:

[0023] a semiconductor integrated circuit comprising:
[0024] a memory cell array having a plurality of word lines;

[0025] a first decoder decoding address signals in response to a RAS signal to output first decoding signals;

[0026] a plurality of feed lines;

[0027] a word driver having a plurality of blocks, each of which has at least one driving circuit, each of the driving circuits being connected with an associated one of the plurality of feed lines, each input terminal of the driving circuits receiving an associated one of the first decode signals and each output terminal of the driving circuits being connected to an associated one of the word lines, and

[0028] a cut-off circuit having a second decoder which decodes a part of the address signals to output second decoding signals, a plurality of first transistors, each of which is serially connected to associated one of the plurality of feed lines, each control electrode of the plurality of first transistors receiving an associated one of the second decoding signals, a plurality of second transistors, each of which is connected in parallel to each of the plurality of first transistors associated with it.

[0029] Control electrodes of the plurality of second transistors receive the RAS signal.

[0030] Driving powers of the plurality of first transistors are larger than those of the plurality of second transistors.

[0031] According to this construction, when an electric potential of a feed line drops upon standby of a logic circuit by a subthreshold leakage current of the logic circuit, the feed line is charged prior to activation of the logic circuit, so that the activation of the logic circuit can be executed at a high speed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The above and other objects, advantages and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

[0033] FIG. 1 is a block diagram of the first embodiment of a semiconductor integrated circuit according to the invention;

[0034] FIG. 2 is a timing chart showing an operation of the semiconductor integrated circuit as shown in FIG. 1;

[0035] FIG. 3 is a block diagram of the second embodiment of the semiconductor integrated circuit according to the invention;

[0036] FIG. 4 is a timing chart showing an operation of the semiconductor integrated circuit as shown in FIG. 3;

[0037] FIG. 5 is a block diagram of a conventional semiconductor integrated circuit; and

[0038] FIG. 6 is a block diagram of a DRAM to which the semiconductor integrated circuit according to the invention is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039] A semiconductor integrated circuit according to the first embodiment of the present invention is applied as a selecting circuit of a word line of a dynamic random access memory (DRAM) and, as shown in FIG. 1, has a word driver 10 and a cut-off circuit 30. FIG. 6 shows a block diagram of the DRAM to which a circuit shown in FIG. 1 is applied. A RAS signal, a CAS signal, and address signals A0 to Ai are inputted to a row and column decoder 40. In response to the RAS signal, signals which are obtained by decoding the address signals A0 to Ai are outputted to the word driver 10. In response to the CAS signal, the decoding signals are outputted to a YSW selector 70. A cut-off circuit 30 decodes a part (here, corresponding to signals Aj to Ai) of the address signals AO to Ai, so that a current is supplied to one of blocks 101 to 10n of the word driver 10. A memory cell array 50 outputs data stored in a selected memory cell to input/output terminals DQ0 to DQi via a DIO 60, or stores inputted data to the selected memory cell.

[0040] The word driver 10 is divided into n blocks 101, 102, and 10n. Each of the blocks is constructed by each of m driving circuits 1211 to 121m, 1221 to 122m, . . . , and 12n1 to 12nm which comprise an arbitrary logic circuit. Each of the outputs of the driving circuits 1211 to 121m, 1221 to 122m, . . . , and 12n1 to 12nm is connected to a plurality of word lines in the memory cell array 50. Activation of one of driving circuits in accordance with the input addresses A0 to Ai results in selecting one of the word lines. The driving circuits 1211 to 121m, 1221 to 122m, . . . , and 12n1 to 12nm comprise, for example, an NCT circuit, NAND circuit, or the like, respectively.

[0041] The cut-off circuit 30 comprises by: a decoder 100; n cut-off PMOS transistors 11, 12, . . . , and 1n, each of which is driven by each of decoding signals Q1, Q2, . . . , and Qn of the decoder 100, and one end of each of which is connected to a power source and the other ends of which are connected to the word driver 10; and n pMOS transistors 21, 22, . . . , and 2n, each of which is connected in parallel to each of the cut-off PMOS transistors 11, 12, . . . , and 1n, and are driven by a signal φ.

[0042] An operation of the semiconductor integrated circuit of this embodiment will now be described with reference to FIGS. 1, 6, and 2 in the following.

[0043] First, when the word driver 10 as shown in FIG. 1 does not output, that is, in case of standby of the operation of the word driver 10, all of the driving circuits in the word driver 10 and cut-off pMOS transistors 11, 12, . . . , and 1n and pMOS transistors 21, 22, . . . , and 2n are turned off. Therefore, increase in consumption of an electric power by the subthreshold current upon standby of the operation can be prevented.

[0044] Subsequently, operation time of the word driver 10 will be described.

[0045] FIG. 2 shows a timing chart in case where the address signals A0 to Ai are decoded, so that the driving circuit 1211 in the block 101 of the word driver 10 is selected.

[0046] Since, on standby of the operation, the cut-off pMOS transistors 11 to 1n are turned off as mentioned above
and the word driver 10 is disconnected from a power source Vcc, there is a chance that electric potentials of feed lines L₁ to Lₙ drop by a subthreshold current of the word driver 10. FIG. 2 shows such a case and the electric potential of the feed line L₁ is decreased upon standby of the operation. When the /RAS signal is activated from such a state, in response to that, the signal Φ is set to the low level. Thus, the transistors 21 to 2n as shown in FIG. 1 are turned on and the feed lines Lₙ to L₁ are charged. That is, the electric potentials of the feed lines L₁ to Lₙ are preliminarily increased. In FIG. 2, the electric potentials of the feed lines L₂ to Lₙ are omitted.

[0047] After that, a part (A) to (A) of the input addresses are decoded by the decoder 100 and the decoding signal Φ₁ is set to the low level. The input addresses A₀ to Aₙ are decoded by a decoder 40 and an input signal 121₁ₒᵣₐ, of the driving circuit 121₁ is set to the high level. Thus, an output signal 121₁ₒᵣₐ is outputted and one of the word lines in the memory cell array 50 is selected. In this instance, according to the embodiment, since the feed lines L₁ to Lₙ are preliminarily charged before the decoding signal from the decoder 40 is inputted to the word driver 10, the driving circuit 121₁ can output the output signal 121₁ₒᵣₐ promptly after the decoding signal 121₁ₒᵣₐ was inputted.

[0048] Timings of transition of the decoding signal Φ₁ and transition of the signal 121₁ₒᵣₐ are delayed from transition of the /RAS signal for a predetermined period by delay of the cut-off circuit 30 and decoder 40. Consequently, the signal Φ to drive the transistors 21 to 2n is set to a signal which synchronizes with the transition of the /RAS, so that, as mentioned above, the feed lines L₁ to Lₙ can be preliminarily charged.

[0049] Since the pMOS transistors 2₁, 2₂, . . . , and 2ₙ shown in FIG. 1 function in order to charge the feed lines L₁ to Lₙ, it is preferable that transistors having a small driving power are used. By such transistors, consumption of the electric power is suppressed as much as possible and an operation at a high speed can be realized.

[0050] It is preferable that the cut-off pMOS transistors 1₁, 1₂, . . . , and 1ₙ have a large driving power so as to drive the word driver 10.

[0051] As mentioned above, in the first embodiment of the semiconductor integrated circuit according to the invention as shown in FIG. 1, even if the electric potentials of the feed lines L₁, L₂, . . . , and Lₙ decrease by the subthreshold current of the word driver 10, prior to inputting of the decoding signal, the pMOS transistors 2₁, 2₂, . . . , and 2ₙ are turned on, so that the feed lines L₁, L₂, . . . , and Lₙ can be pre-charged (those electric potentials can be increased) and the operation after that can be performed at a high speed.

[0052] Next, the second embodiment of the semiconductor integrated circuit of the invention will be now described with reference to FIGS. 3, 4 and 6.

[0053] The semiconductor integrated circuit according to the second embodiment is applied as a selecting circuit of a word line of a dynamic random access memory (DRAM) similarly with the first embodiment. As shown in FIG. 3, the semiconductor integrated circuit has the word driver 10 and cut-off circuit 30. In the embodiment, different from the first embodiment, the cut-off circuit 30 further has cut-off nMOS transistors 3₈₁, 3₈₂, and 3₈ₙ for cutting off the subthreshold current which are provided for n grounding lines S₁, S₂, . . . , and Sₙ of the word driver 10. Each of the cut-off nMOS transistors 3₈₁, 3₈₂, and 3₈ₙ is controlled by each of the signals Φ₁, Φ₂, . . . , and Φₙ which is obtained by inverting each of the decoding signals Φ₁, Φ₂, . . . , and Φₙ outputted from the decoder 100 by an NOT (inverter) 3₆₅.

[0054] Further, the cut-off circuit 30 has nMOS transistors 3₇₁, 3₇₂, . . . , and 3₇ₙ, each of which is connected in parallel to each of the cut-off nMOS transistors 3₈₁, 3₈₂, . . . , and 3₈ₙ. Those transistors can be driven by the signal Φᵣ.

[0055] Similarly with the first embodiment, the word driver 10 is divided into n blocks 1₀₁, 1₀₂, . . . , and 1₀ₙ. Each of the blocks is constructed of m driving circuits 3₂₁₁ to 3₂₁ₘ, 3₂₂₁ to 3₂₂ₙ, . . . , and 3₂₁ to 3₂ₙ each constructed by an arbitrary logic circuit. Each of the outputs of the driving circuits 3₂₁₁ to 3₂₁ₘ, 3₂₂₁ to 3₂₂ₙ, . . . , and 3₂₁ to 3₂ₙ is connected to a plurality of word lines in the memory cell array 50, respectively. In response to the input address signals A₀ to Aₙ, one of the driving circuits is activated, so that one of the plurality of word lines is selected. Each of the driving circuits 3₂₁₁ to 3₂₁ₘ, 3₂₂₁ to 3₂₂ₙ, . . . , and 3₂₁ to 3₂ₙ according to the embodiment is constructed by two inverters 3₅₁ and 3₆₁ as shown in FIG. 3.

[0056] An operation of the semiconductor integrated circuit of the embodiment will now be described in the following.

[0057] First, if the word driver 10 as shown in FIG. 3 does not output, that is, in case of standby of the operation of the word driver 10, all of the driving circuits in the word driver 10 and cut-off nMOS transistors 1₁, 1₂, . . . , and 1ₙ and pMOS transistors 2₁, 2₂, . . . , and 2ₙ and cut-off nMOS transistors 3₈₁, 3₈₂, and 3₈ₙ and nMOS transistors 3₇₁, 3₇₂, . . . , and 3₇ₙ are turned off. Therefore, increase in consumption of an electric power by the subthreshold current upon standby of the operation can be prevented.

[0058] Next, operation timing of the word driver 10 will be described.

[0059] FIG. 4 shows a timing chart in case where the address signals A₀ to Aₙ are decoded, so that the driving circuit 3₂₁₁ in the block 1₀₁ of the word driver 10 is selected.

[0060] Since, on standby of the operation, the cut-off pMOS transistors 1₁ to 1ₙ are turned off as mentioned above and the word driver 10 is disconnected from the power source Vcc, there is a chance that electric potentials of the feed lines L₁ to Lₙ drop by the subthreshold current of the word driver 10. Since the cut-off nMOS transistors 3₈₁, 3₈₂, . . . , and 3₈ₙ are also turned off and the word driver 10 is disconnected from the grounding power source as well, there is a chance that the electric potentials of the grounding lines S₁ to Sₙ are increased by the subthreshold current.

[0061] FIG. 4 shows such a state and the electric potential of the feed line L₁ drops upon standby of the operation and the electric potential of the grounding line S₁ increases. When the /RAS signal is active from such a state, in response to this state, the signal Φ is set to the low level. Thus, the transistors 2₁ to 2n as shown in FIG. 3 are turned on and the feed lines L₁ to Lₙ are charged. That is, the electric potentials of the feed lines L₁ to Lₙ are preliminarily
increased and, in response to the signal \( \Phi \). Further, in response to the signal \( \Phi \), the transistors 371 to 37\( n \) are turned on and the grounding lines S1 to Sn are discharged. That is, the electric potentials of the grounding lines are preliminarily decreased.

In FIG. 4, the electric potentials of the feed lines L2 to Ln and the grounding lines S2 to Sn are omitted.

[0062] After that, the decoder 100 decodes a part (Aj to Ai) of the input address signals and the decoding signal \( \Phi \) is set to the low level. The input address signals \( \text{Ai} \) to \( \text{Ai} \) are decoded by the decoder 40 and an input \( 3211 \_\text{out} \) of the driving circuit 3211 is set to the high level. Thus, a signal \( 3211 \_\text{out} \) is outputted and one of the word lines in the memory cell array 50 are selected. In this instance, according to this embodiment, since the feed lines L1 to Ln are preliminarily charged before the decoding signal from the decoder 40 is inputted to the word driver 10 and the grounding lines S1 to Sn are discharged, the driving circuit 3211 can output the output signal \( 3211 \_\text{out} \) promptly in response to the input of the decoding signal \( 3211 \_\text{out} \).

[0063] As mentioned above, in the second embodiment of the semiconductor integrated circuit according to the invention as shown in FIG. 3 as well, an effect similar to that of the first embodiment as shown in FIG. 1 can be obtained. Further, each of the nMOS transistors 371 to 37\( n \) is connected in parallel to each of the cut-off nMOS transistors 381 to 38\( n \) serving as transistors for cutting-off the sub-threshold current, respectively, which is serially connected to each of the grounding lines of the word driver 10. Therefore, if the word driver 10 is operated, prior to start of the operation, the electric potentials of the grounding lines S1, S2, \ldots, and Sn can be decreased, so that the word driver 10 can be activated more promptly.

[0064] In the first embodiment, a case where each of the pMOS transistors 21 to 2\( n \) is connected in parallel to each of the cut-off pMOS transistors 11 to 1\( n \) which is serially connected to each of the feed lines of the word driver 10 has been described. In the second embodiment, a case where each of the pMOS transistors 21 to 2\( n \) is connected in parallel to each of the cut-off pMOS transistors 11 to 1\( n \) which is serially connected to each of the feed lines of the word driver 10. Each of the nMOS transistors 371 to 37\( n \) is connected in parallel to each of the cut-off nMOS transistors 381 to 38\( n \) which is serially connected to each of the grounding lines of a logic gate circuit group 41 has been described. This invention, however, is not limited to the foregoing embodiments and various modifications can be embodied without departing from the scope of the invention.

[0065] For example, as shown in the second embodiment, transistors can be provided for the grounding lines of the word driver 10, thus providing transistors for both of the feed lines and the grounding lines of the word driver 10. That is, an embodiment such that each of the nMOS transistors is connected in parallel to only each of the cut-off nMOS transistors which is serially connected to each of the grounding lines of the word driver 10 is possible.

[0066] The logic circuit comprising the word driver 10, which is provided by the foregoing first and second embodiments, can be constructed by properly combining not only the NOT or NAND but also NOR, AND, OR, or the like.

[0067] In the foregoing first and second embodiments, signals as signals \( \Phi \) and \( \Phi' \) inputted to gates of the PMOS transistors 21 to 2\( n \) and nMOS transistors 371 to 37\( n \) are not especially limited. However, as a signal \( \Phi \), the RAS signal can be directly used and, as a signal \( \Phi' \), an inverting signal of the RAS signal can be used. Further, inversely, that is, as a signal \( \Phi \), an inverting signal of the address signal RAS can be used and, as a signal \( \Phi' \), the RAS signal can be directly used. In those cases, timings when the pMOS transistors 21 to 2\( n \) and nMOS transistors 371 to 37\( n \) are turned on become further rapid and the word driver 10 can be activated further rapidly.

[0068] Moreover, the invention is not limited to a case where it is applied to a word driver serving as a selecting circuit of a word line in a dynamic random access memory (DRAM) and can be applied to other various circuits.

[0069] As will be obviously understood, according to the present invention, in a semiconductor integrated circuit having a logic gate circuit group comprising a plurality of logic gate circuits, when the feed lines (grounding lines) to supply electric potentials to the plurality of logic gate circuits are voltage-decreased (increased) by a subthreshold leakage current, transistors such that prior to activating the circuit, the feed lines are preliminarily charged (discharged) and the electric potentials are decreased (increased) are added, so that a semiconductor integrated circuit which enables the logic gate circuit group to be activated at a high speed can be provided.

[0070] It is apparent that the present invention is not limited to the above embodiments, but may be modified and changed without departing from the scope and spirit of the invention.

What is claimed is:

1. A semiconductor integrated circuit comprising:
   a first feed line;
   a second feed line;
   a first power source line for applying a first electric potential to said first feed line;
   at least one logic circuit connected between said first feed line and said second feed line and outputting a signal of a predetermined logic level in accordance with a logic level of an input signal;
   a first transistor having a first conductivity type and having a current path between said first power source line and said first feed line; and
   a second transistor having said first conductivity type and connected in parallel to said first transistor.

2. The semiconductor integrated circuit according to claim 1, wherein said first transistor is in a conductive state when said logic circuit is in an operation state and is in a non-conductive state when said logic circuit is in a standby state.

3. The semiconductor integrated circuit according to claim 2, wherein said second transistor is changed from a non-conductive state to a conductive state before said first transistor is changed from a non-conductive state to a conductive state.

4. The semiconductor integrated circuit according to claim 1, wherein a driving power of said first transistor is larger than that of said second transistor.
5. The semiconductor integrated circuit according to claim 1, further comprising:

a second power source line for applying a second electric potential to said second feed line;

a third transistor having a second conductivity type and having a current path between said second power source line and said second feed line; and

a fourth transistor having said second conductivity type and connected in parallel to said third transistor.

6. The semiconductor integrated circuit according to claim 5, wherein said third transistor is in a conductive state when said logic circuit is in said operation state and is in a non-conductive state when said logic circuit is in said standby state.

7. The semiconductor integrated circuit according to claim 6, wherein said fourth transistor is changed from a non-conductive state to a conductive state before said third transistor is changed from said non-conductive state to said conductive state.

8. The semiconductor integrated circuit according to claim 5, wherein a driving power of said third transistor is larger than that of said fourth transistor.

9. The semiconductor integrated circuit according to claim 5, wherein said first and second transistors are p-channel type MOS transistors and said third and fourth transistors are n-channel type MOS transistors.

10. A semiconductor integrated circuit comprising:

a memory cell array having a plurality of word lines;

a first decoder decoding address signals in response to a /RAS signal to output first decoding signals;

a plurality of feed lines;

a word driver having a plurality of blocks, each of which has at least one driving circuit, each of said driving circuits being connected with associated one of said plurality of feed lines, input terminal of said driving circuits receiving one of said first decode signals and output terminal of said driving circuits being connected to associated one of said word lines, and

a cut-off circuit having a second decoder which decodes a part of said address signals to output second decoding signals, a plurality of first transistors, each of which is serially connected to associated one of said plurality of feed lines, each control electrode of said plurality of first transistors receiving associated one of said second decoding signals, a plurality of second transistors, each of which being connected in parallel to each of said plurality of first transistors.

11. The semiconductor integrated circuit according to claim 10, wherein control electrodes of said plurality of second transistors receive said /RAS signal.

12. The semiconductor integrated circuit according to claim 10, wherein driving powers of said plurality of first transistors are larger than those of said plurality of second transistors.

13. The semiconductor integrated circuit according to claim 10, further comprising a plurality of ground lines, each of which is connected to associated one of said driving circuits, a plurality of third transistors, each of which is serially connected to associated one of said plurality of ground lines, and each control electrode of which receiving associated one of inverted signals of said second decoding signals, a plurality of fourth transistors, each of which being connected in parallel to each of said plurality of third transistors.

14. The semiconductor integrated circuit according to claim 13, wherein control electrodes of said plurality of fourth transistors receive inverted signal of said /RAS signal.

15. The semiconductor integrated circuit according to claim 13, wherein driving powers of said plurality of third transistors are larger than those of said plurality of fourth transistors.

16. The semiconductor integrated circuit according to claim 13, said plurality of first transistors and said plurality of second transistors are p-channel type MOS and said plurality of third transistors and said plurality of fourth transistors are n-channel type MOS transistors.