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ASYNCHRONOUS TRANSMISSION FOR NFC CARD EMULATION MODE

ASYNCHRONE ÜBERTRAGUNG FÜR NFC-Kartenemulationsmodus

ÉMISSION ASYNCHRONE POUR UN MODE D'ÉMULATION DE CARTE NFC

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This invention relates to a method and system for asynchronous communication technique in Near Field Communication (NFC) system. Particularly, this invention relates to a method and system for generating a clock frequency that is close to the clock frequency received from the NFC reader for use in asynchronous communication technique in NFC system.

Summary of the Prior Art

Near Field Communication (NFC) enables contactless short range communication between two devices, typically requiring distance of 4 cm or less to initiate a connection. The connection can be done much faster than other communication technologies like Bluetooth or WiFi. The user only needs to bring two NFC supported devices closer and data will be transferred automatically. Some of its applications include credit card payment, ticketing, content sharing, quick pairing, and etc. Some of its applications include credit card payment, ticketing, content sharing, quick pairing, and etc.

In general, NFC device requires very low power or no power for transmission when it operates in tag or card emulation mode. NFC tag/card device will first detect RF magnetic field from NFC reader device. The magnetic field energy is used to power the load component in the NFC tag/card device and transfer the data using passive load modulation (PLM). The term "passive" here is because there is no need for the NFC tag/card device to use its own energy for the transmission. Thus, when implemented in any mobile phones or tablet PCs, it still works when the battery dies and it does not affect device battery consumption.

Having good advantages, passive load modulation has its drawbacks. The amount of magnetic field that can be absorbed by the NFC tag/card device is limited to the antenna coupling between two NFC devices. Antenna coupling performance can deteriorate, for example, when smaller antenna is used or when two NFC devices are further apart.

Other NFC tag/card emulation technique is Active Load Modulation (ALM). This technique is getting popular as there is a strong interest in integrating NFC technology into mobile phones or tablet PCs. Mobile phones or tablet PCs have their own battery power, and thus, the NFC tag/card devices will be able to utilize their own battery power to generate the magnetic field during load modulation. ALM mode is also more suitable for smaller antenna implementation in the device and has better performance than the PLM mode. However, for both PLM and ALM modes, normal clock recovery is required to ensure synchronous transmission between NFC devices.

A known NFC using analog phase-locked loop (PLL) to control ALM is disclosed in US 8934836 B2. Figure 1 shows the circuitry design of the NFC between two devices disclosed in US 8934836 B2.

The above advantages are provided by the subject matter of independent claims 1 and 4. Further imple-
In accordance with embodiments of this invention, a method for an NFC card for use in asynchronous NFC card emulation mode transmission is provided. The method comprises estimating a carrier frequency offset between a carrier frequency of a NFC reader and a carrier frequency of the NFC card, adjusting digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset to obtain an adjusted baseband sample output, and modulating a RF transmitter based on the adjusted baseband sample output.

In accordance with embodiments of this invention, the step of estimating carrier frequency offset is triggered upon detecting a radio frequency (RF) magnetic field from the NFC reader.

In accordance with embodiments of this invention, the step of estimating carrier frequency offset is provided in the following manner. The method obtains an in-phase component (I) and a quadrature phase component (Q) for a number of samples of an input signal from an Analogue to Digital Converter (ADC) of the NFC card. The phase for each sample is then computed with the following expression: \( \tan^{-1}(Q/I) \). Subsequently, the method obtains the set of inphase component (I) and quadrature phase component (Q), wherein \( fc \) is the carrier frequency, \( fs \) is the ADC sampling frequency, and \( n \) is the sample number.

In accordance with embodiments of this invention, the step of obtaining the set of inphase component (I) and quadrature phase component (Q) for the signal from the Analogue to Digital Converter (ADC) of the NFC card is provided in the following manner. The input signal at intermediate frequency is down-converted into a complex signal centered at zero frequency. Subsequently, a low pass filter is applied to filter harmonics components from the complex signal. The input signal at intermediate frequency into a complex signal centered at zero frequency is down-converted by multiplying the input signal with \( \cos(2\pi fc/fs \cdot n) \) to obtain inphase component (I) and multiplying the input signal with \( \sin(2\pi fc/fs \cdot n) \) to obtain quadrature phase component (Q), where \( fc \) is the carrier frequency, \( fs \) is the ADC sampling frequency, and \( n \) is the sample number.

In accordance with embodiments of this invention, the step of adjusting digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset may be provided in the following manner. The method obtains the input sample stream with reference to \( k \), input\([n]\) is the input sample with reference to \( n \). If there is any more input sample stream, the method increments \( n \) and \( k \) by 1 and repeats from the step of adding the absolute of the estimated CFO to Acc. If the Acc is more than the input sampling frequency of the NFC card, the method determines if the estimated CFO is greater than zero. If the estimated CFO is greater than zero, the method adds one sample and deducts the Acc by input sampling frequency. The method adds one sample by incrementing \( n \) by 1 and outputting the input sample with the following expression output\([k]=\text{input}\([n]\)\). If the estimated CFO is less than zero, the method skips one sample and deducts the Acc by input sampling frequency. The method skips one sample by incrementing \( n \) by 1 and outputting the input sample with the following expression output\([k]=\text{input}\([n]\)\).

In accordance with embodiments of this invention, the step of adjusting digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset may be provided in the following manner. Input sample stream is received from an encoder. In response to receiving the input sample stream from an encoder, the method sets Acc to zero and retrieves the estimated CFO from the memory. The absolute of the estimated CFO is added to Acc. If the Acc is less than the data-rate, the method establishes the number of samples for each encoded bit, \( N \), is equal to number of samples per information bit, Bit_Len, where data-rate is equal to sampling frequency divided by Bit_Len. If the Acc is more than the data-rate, the method deducts the Acc by data-rate and determines if the estimated CFO is greater than zero. If the estimated CFO is greater than zero, the method establishes that \( N \) is equal to Bit_Len+1. If the estimated CFO is less than zero, the method establishes that \( N \) is equal to Bit_Len-1. The digital baseband sample for 1 bit duration is then generated based on value of \( N \). If there is any more input sample stream, repeating from the step of adding the absolute of the estimated CFO to Acc.

In accordance with embodiments of this invention, a NFC card having a clock frequency offset (CFO) estimation module, a sample adjustment module and an analogue transmission module is provided to perform the method as described above.

**Brief Description of the Drawings**

- Figure 1 illustrating a known circuitry design of the NFC between two devices;
- Figure 2 illustrating an overview of an asynchronous transmission between two NFC devices in accordance with an embodiment of this invention;
Figure 3 illustrating an overview of a process flow performed by an NFC Device in card emulation mode upon detecting a carrier signal from another NFC Device in accordance with an embodiment of this invention;

Figure 4 illustrating a block diagram of the digital baseband of an NFC Device in asynchronous transmission in accordance with an embodiment of this invention;

Figure 5 illustrating a receiver processing timeline at the NFC Device in asynchronous card emulation mode in accordance with an embodiment of this invention;

Figure 6 illustrating a process flow performed by a CFO estimation module in accordance with an embodiment of this invention;

Figure 7 illustrating a block diagram of digital receiving module in accordance with an embodiment of this invention;

Figure 8 illustrating an embodiment of the CFO correction module in accordance with an embodiment of this invention;

Figure 9 illustrating a block diagram of digital transmission module for DBB controlled sample adjustment in accordance with an embodiment of this invention;

Figure 10 illustrating a process on the algorithm of DBB controlled sample adjustment at transmission mode shown in figure 9 in accordance with an embodiment of this invention;

Figure 11 illustrating a process on the algorithm of MAC controlled sample adjustment at transmission mode shown in figure 12 in accordance with an embodiment of this invention; and

Figure 12 illustrating a block diagram of digital transmission module for MAC controlled sample adjustment in accordance with an embodiment of this invention.

Detailed Description

[0021] This invention relates to a method and system for asynchronous communication technique in Near Field Communication (NFC) system. Particularly, this invention relates to a method and system for generating a clock frequency that is close to the clock frequency received from the NFC reader for use in asynchronous communication technique in NFC system.

[0022] A clock offset adjustment is introduced in NFC tag/card device for NFC transmission. This is different from conventional communication systems, such as cellular communications, WiFi or Bluetooth communications, where no clock offset adjustment is carried out at the transmission and the clock offset is typically taken care at the receiver.

[0023] In conventional NFC PLM communication, the NFC tag/card device recovers the clock from the NFC Reader/Poll Device magnetic field and uses this recovered clock to transmit the response frames back to the NFC Reader/Poll Device. So by nature of equal clock frequency, the NFC reader/poll device does not carry out any clock adjustment at the response frame reception.

[0024] With local power supply, NFC tag/card device may adopt ALM communication. However, the NFC reader/poll device has no idea whether the NFC tag/card device is in PLM or ALM mode. Further, the NFC reader/poll device may not carry out any clock adjustment at the response frame reception. Hence, NFC Tag/Card Device transmission at ALM mode should guarantee the clock of transmitted signal to be synchronized (both frequency and phase) with NFC reader/poll device clock.

[0025] In US 8934836 B2, the NFC tag/card device transmission employs the clock recovery process in Analog module to guarantee the clock of transmitted signal matches with NFC reader/poll device clock. In this invention, we introduce a sample-based low complexity method to compensate carrier frequency offset between NFC tag/card device and NFC reader/poll device, without the analog clock recovery process.

[0026] The required processes for asynchronous communication of NFC tag/card emulation mode will be described below.

[0027] Figure 2 illustrates the overview of an asynchronous transmission between two NFC devices. NFC Device 1 100 is a typical reader or poll device in NFC protocol with a clock frequency of \( f_{R1} \). This means that the magnetic field generated by NFC device 1 100 is \( f_{R1} \). NFC Device 2 120 is an NFC tag/card or listen device in ALM mode. The NFC Device 2 120 employs a local clock generator 123 to generate the clock frequency of \( f_{R2} \) and supplies this clock to both digital receiver module 121 and digital transmission module 122, where \( f_{R2} \) may not be the same as \( f_{R1} \). The local clock generator 123 is used as reference clock in all NFC card digital modules including Digital RX module and TX module.

[0028] Since \( f_{R2} \) is unlikely to be the same as \( f_{R1} \), the digital receiver module 121 of NFC Device 2 120 is required to adjust the clock offset between \( f_{R1} \) and \( f_{R2} \) at the demodulation and decoding. Further details in this regard will be described below with reference to figure 5.

[0029] The digital transmission module 122 of NFC Device 2 120 employs a sample-based low complexity method to compensate carrier frequency offset between \( f_{R1} \) and \( f_{R2} \). Further details pertaining to the sample-based low complexity method will be described below with reference to figure 5. As a result, the transmitted signal from NFC Device 2 120 is at the clock frequency of \( f_{R2} \), which is approximated to \( f_{R1} \) but not exactly the same as \( f_{R1} \). Thus, this is an asynchronous transmission to NFC Device 1 100.

[0030] For purposes of this discussion, an NFC tag/card device means the NFC device is in card emulation mode. The term 'tag' and 'card' can be used interchangeably.

[0031] Figure 3 illustrate an overview of a process flow performed by NFC Device 2 120 upon detecting a
carrier signal, \( f_{R1} \), from NFC Device 1 100. The process
flow 300 begins with step 305 where NFC Device 2 120 de-
tects a RF magnetic field from NFC Device 1 100. The
signal received is processed in the analogue receiving
module 124 in a conventional manner. Particularly, the
signal is converted to digital signal by an Analogue to
Digital Converter (ADC). For brevity, specific details per-
taining to the analogue receiving module 124 are omitted. [0034] In step 310, NFC Device 2 120 estimates the
clock frequency offset (CFO), \( \Delta f = f_{R1} \cdot f_{R2} \), and stores
the CFO information to a memory in the digital baseband.
NFC Device 2 then continues to demodulate the received
signal from NFC Device 1 in step 315. In step 320, pro-
cess 300 determines whether NFC Device 2 120 is being
switched to transmission state. If NFC Device 2 120 is
still in receiving state, process 300 repeats step 315. In
brief, the step 315 repeats until the NFC Device 2 is ready
to receive NFC Device 1. If the NFC Device 2 120 is being
switched to transmission state, process 300 proceeds to step 325. Further details regarding demod-
ulating of the received signal will be described below with
reference to figures 7 and 8.

[0035] In step 325, NFC Device 2 performs encoding
and subcarrier generation of the information bit stream.
In step 330, NFC Device 2 adjusts the digital baseband
output samples based on the CFO estimation information
stored on the memory. Further details regarding the ad-
justment of digital transmission sample will be described
below with reference to figures 9-12. After the adjust-
ment, the frequency of RF transmitted signal will be very
close to \( f_{R1} \) and process 300 proceeds to step 335 to
perform RF modulation by the analogue transmission
module 125 in a conventional manner. For brevity, spe-
cific details pertaining to the analogue receiving module 124 are omitted. Process 300 ends after step 335.
[0036] Advantageously, NFC Device 1, which could be
from a different manufacturer, does not need to perform
any additional processing to receive the signal from NFC
Device 2 since the \( f_{R2} \) is almost equal to \( f_{R1} \).

[0037] Figure 4 illustrates the overall block diagram of
the digital baseband 400 of NFC Device 2 120 in asyn-
chronous transmission. The digital baseband 400 of a
NFC card emulation receiver comprises CFO estimation
module 410, memory 420, digital receiving module 121 and
the digital transmission module 122. The digital rece-
iving module 121 converts the received signal into de-
coded bit stream using the carrier frequency offset from
the memory 420. The digital transmission module 122
converts the input bit stream into baseband sampling out-
put for RF modulation.

[0038] Figure 5 illustrates the receiver processing
timeline at NFC Device 2 in asynchronous card emulation
mode. AGC adjustment may be included before CFO es-
timation to ensure a stable receiving signal at the receiv-
er. CFO estimation is performed during carrier wave
(CW) period, which is available before receiving NFC De-
vice 1 packet.

[0039] Further details regarding the CFO estimation
module 410 will be described below with reference to
figure 6. Further details regarding digital receiving mod-
ule 121 and digital transmission module 122 will be de-
scribed below with reference to figures 7-8 and 9-12 re-
spectively.

[0040] Figure 6 illustrates a process flow 600 being
performed by the CFO estimation module 410. The pro-
cess 600 begins with step 605 by obtaining an in-phase
component (I) and a quadrature phase component (Q)
for a number of samples from the ADC output. The set
of in-phase component (I) and quadrature phase com-
ponent (Q) can be obtained in the following manner. First,
the input signal (i.e. the ADC output) is down-converted
at intermediate frequency into a complex signal centered
at zero frequency. Particularly, the down-converting is
by multiplying the input signal by locally generated down
conversion sample of \( \cos(2\pi fc/fs n) \) and \( \sin(2\pi fc/fs n) \) to
obtain the in-phase component (I) and quadrature com-
ponent (Q) respectively, where \( fc \) is the carrier frequency,
fs is the ADC sampling frequency, and \( n \) is the sample
number. In this exemplary embodiment of invention, fs
is equal to 4 times of \( fc \). For \( fs = 4fc \), the down conversion
becomes very simple as the \( \cos(2\pi fc/fs n) \) and \( \sin(2\pi fc/fs n) \) can
be replaced by the sequence of \((1,0,1,0)\) and
\((0,1,0,1)\), respectively. Particularly, when \( fs = 4fc \),
\( \cos(2\pi fc/fs n) \) would be equal to \( \cos(\pi n/2) \). Substituting
the sample number \( n = 0,1,2,3,4,5,... \) into \( \cos(\pi n/2) \), we
get \( \cos(0), \cos(\pi/2), \cos(\pi), \cos(3\pi/2), \cos(2\pi), \cos(2.5\pi),... \) which would result in
\( 1,0,-1,0,1,0,-1,0,... \). This is a repeated sequence of
\((1,0,-1,0)\).

[0041] Similarly for the sin function, when \( fs = 4fc \),
\( \sin(2\pi fc/fs n) = \sin(\pi n/2) \). Substituting the sample
number \( n = 0,1,2,3,4,5,... \), we get \( \sin(0), \sin(\pi/2), \sin(\pi), \sin(3\pi/2), \sin(2\pi), \sin(2.5\pi),... \) which would result in
\( 0,1,0,-1,0,1,0,-1,... \). This is a repeated sequence of
\((0,1,0,-1)\).

[0042] After down-converting the input signal, a low
pass filtering is applied to filter away harmonics compo-
nents from the input signal. Alternatively, Coordinate Ro-
tation Digital Computer (CORDIC) algorithm may be
used to obtain the in-phase component (I) and quadra-
ture phase component (Q) without departing from the
In step 615, the phase of the vector from the complex signal output which consists of in-phase component (I) and quadrature phase component (Q) is computed using the following expression, phase = \( \tan^{-1}(Q/I) \) for each sample. Essentially, the arctan of Q/I provides the phase shift of the vector of Q/I.

In step 620, the process 600 computes the phase differences between two adjacent samples, i.e. at \( t = i \) and \( t = (i+1) \) where \( i = 1, 2, 3, \ldots \). In step 625, the CFO estimate is then obtained from the average of the phase differences between two adjacent samples. The estimated CFO is then stored on the memory in step 630. Process 600 ends after step 630.

Figure 7 illustrates a block diagram of digital receiving module 121. The digital receiving module 121 comprises a CFO correction module 710 to compensate the asynchronous frequency component, an envelope/phase detector 720 to detect the envelope/phase component of complex baseband signal, and a DEC module 730 to obtain the decoded bit stream. The envelope/phase detector 720 or SYNC process may include DC cancellation to remove the DC component of the signal. Further, the envelope detector can be implemented by using simple approximation of the square root function. When high precision envelope/phase detector is used, CFO correction module 710 may not be required and can be replaced by a simple down conversion based on zero frequency offset.

Figure 8 illustrates an exemplary embodiment of the CFO correction module 710. The CFO correction module 710 may consist of phase rotation module 712, a low pass filter 714 and a decimate module 716. The phase rotation is based on frequency offset information. The rotation is equivalent to multiplying the input with locally generated down conversion sample of \( \cos(2\pi \frac{(fc + \Delta f)}{fs} n) \) and \( \sin(2\pi \frac{(fc + \Delta f)}{fs} n) \) where \( \Delta f \) is carrier frequency offset. The LPF 714 filters the phase rotation output. The decimate module 716 decimates the CFO filter output to lower sampling rate.

Figure 9 illustrates a block diagram of digital transmission module 122. The digital transmission module 122 comprises an encoder 910, a subcarrier generator 920 and a sample adjustment module 930. The information bit stream is fed to the encoder 910 and subcarrier generator 920. The output of subcarrier generator is the digital baseband output of NFC Device 2 in synchronous card emulation mode. A digital transmission sample adjustment module 930 is provided to adjust the digital baseband output to compensate the carrier frequency offset. The sample adjustment module 930 can be based on either digital baseband (DBB) or medium access control (MAC). The block diagram shown in figure 9 is based on DBB controlled sample adjustment. Further details for sample adjustment module in accordance with MAC will be described below with reference to figures 11 and 12. The estimated CFO is retrieved back from the memory 420 during transmission process. The output of digital transmission sample adjustment module 930 is sent to RF module for RF modulation.

For purposes of this discussion, the Digital transmission sample adjustment module 930 is applicable for all NFC specifications, e.g. ISO14443A, ISO14443B, FeliCa, and ISO15693, with any data rates.

DBB controlled sample adjustment

Figure 10 illustrates a process 1000 on the algorithm of DBB controlled sample adjustment at transmission mode shown in figure 9.

The "input sample" is the output from subcarrier generator 920 in Figure 9. In brief, the samples are adjusted whenever the accumulation of the absolute value of estimated CFO (i.e. Acc) is greater than or equal to the input sampling frequency (i.e. Sampling_freq). Input sampling frequency could be 13.56MHz. 1 sample is added if the value of estimated CFO is positive, and 1 sample is skipped if the value of the estimated CFO is negative.

Process 1000 begins with step 1005 by receiving input sample stream from the output of subcarrier generator 920 in Figure 9. In step 1010, process 1000 resets n, k and Acc to zero where n, k and Acc are variables. Variables n and k are used to indicate the input sample number and output sample number respectively while variable Acc refers to the accumulated estimated CFO.

In step 1015, process 1000 adds the absolute of estimated CFO to Acc. If the Acc is determined to be more than the input sampling frequency in step 1020, process 1000 proceeds to step 1030. If the Acc is determined to be less than the input sampling frequency in step 1020, process 1000 proceeds to step 1025.

In step 1025, the input sample stream is directly output since the accumulated estimated CFO is not more than the input sampling frequency.

In step 1030, process 1000 determines whether the estimated CFO is greater than zero, i.e. whether the estimated CFO is positive or negative. If the estimated CFO is positive, process 1000 proceeds to step 1040. If the estimated CFO is negative, process 1000 proceeds to step 1034. A positive estimated CFO means that \( f_{R1} \) is greater than the input sampling frequency and an additional sample is added. A negative estimated CFO means that \( f_{R1} \) is smaller than the input sampling frequency and one input sample is skipped.

In step 1034, process 1000 increases n by 1 and subsequently outputs the next input sample with the following expression \( output[k]=input[n] \) in step 1036. This is so that the current input sample is skipped and the next input sample is being outputted.

In step 1040, process 1000 outputs the input sample with the following expression \( output[k]=input[n] \). In step 1044, process 1000 increase k by 1 and subsequently outputs the input sample with the following expression \( output[k]=input[n] \) in step 1046. This is so that the same sample is outputted twice.
[0057] For purpose of this discussion, the expression output[k]=input[n] is used to illustrate which input sample is being outputted by the sample adjustment module 930.

[0058] In step 1050, process 1000 deducts the Acc by estimated CFO. Figure 12 illustrates the block diagram for sample adjustment module in accordance with MAC. The sample adjustment module 940 receives the encoded bit stream from the encoder 910 and implements transmission sample adjustment to subcarrier generator 920. The subcarrier generator 920 then generates DBB samples for RF modulation.

[0059] As an example, for data rate = 106kbps, the default value of N is 128, which is obtained from the sampling rate of 13.56MHz and data rate of 106kbps under synchronous condition. The sample adjustment module 940 outputs the value of N for each encoded bit. The value of N is adjusted based on the estimated CFO. Figure 12 illustrates the block diagram for sample adjustment module in accordance with MAC. The sample adjustment module 940 receives the encoded bit stream from the encoder 910 and implements transmission sample adjustment to determine the value of N for each encoded bit. The value of N together with the encoded bit stream is then forwarded to subcarrier generator 920. The subcarrier generator 920 then generates DBB samples for RF modulation.

[0060] As an example, for data rate = 106kbps, the default value of N is 128, which is obtained from the ratio between sampling rate of 13.56MHz and data rate of 106kbps under synchronous condition. The sample adjustment module 940 outputs the value of N for each encoded bit back to the subcarrier generator 920. For data rate = 106kbps, the value of N is 128 if 1 more sample is added, 127 if 1 sample is removed, or 128 if the default value is chosen.

[0061] Similar to DBB sample adjustment, Acc is the accumulation of estimated CFO which is obtained from memory 420. Bit_len is the number of samples per information bit. For example, if data-rate = 106kbps, Bit_len = 128; if data-rate = 212kbps, Bit_len = 64; etc. The value of N will be equal to Bit_len if Acc ≤ data-rate. When Acc > data-rate, N will be equal to Bit_len+1 or Bit_len-1 depending on the sign of estimated CFO. DBB samples for 1 bit duration are generated based on the value of N. The relationship between data-rate, Bit_len and sampling frequency is shown in Table 1 below.

<table>
<thead>
<tr>
<th>Data-rate (kbps)</th>
<th>Sampling frequency</th>
<th>Bit_len</th>
</tr>
</thead>
<tbody>
<tr>
<td>106</td>
<td>13.568MHz</td>
<td>128</td>
</tr>
<tr>
<td>212</td>
<td></td>
<td>64</td>
</tr>
<tr>
<td>424</td>
<td></td>
<td>32</td>
</tr>
<tr>
<td>848</td>
<td></td>
<td>16</td>
</tr>
</tbody>
</table>

[0062] Figure 11 illustrates a process 1100 on the algorithm of MAC controlled sample adjustment at transmission mode shown in figure 12. Process 1100 begins with step 1105 by receiving encoded bit stream from the encoder 910 in Figure 12. In step 1110, process 1100 resets Acc to zero.

[0063] In step 1115, process 1100 adds the absolute of CFO estimated offset frequency to Acc. If the Acc is determined to be more than the data-rate in step 1120, process 1100 proceeds to step 1125. If the Acc is determined to be less than the data-rate in step 1120, process 1100 proceeds to step 1140.

[0064] In step 1140, the number of samples for each encoded bit is equal to Bit_len since the accumulated estimated CFO is not more than the data-rate. The value of N is transmitted to the subcarrier generator 920.

[0065] In step 1125, process 1100 deducts the Acc by the relevant data-rate.

[0066] In step 1130, process 1100 determines whether the estimated CFO is greater than zero, i.e. whether the estimated CFO is positive or negative. If the estimated CFO is positive, process 1100 proceeds to step 1135. If the estimated CFO is negative, process 1100 proceeds to step 1145. A positive estimated CFO means that FR1 is greater than the input sampling frequency and an additional sample is added in step 1135. A negative estimated CFO means that FR1 is smaller than the input sampling frequency and one sample is removed in step 1145. The value of N is then transmitted to the subcarrier generator 920.

[0067] In step 1150, the digital baseband sample for 1 bit duration based on value of N is generated by the subcarrier generator 920.

[0068] In step 1155, process 1100 determines whether there is any more input sample stream. If there is more input sample stream, process 1100 repeats from step 1115. If there is no more input sample stream, process 1100 ends.

[0069] A wireless communication device may include both NFC in ALM and PLM modes. During the ALM mode, the asynchronous card emulation mode as illustrated above will be implemented. During the PLM mode, it will use conventional system to recover the clock from the magnetic field. Hence, the asynchronous card emulation mode as illustrated above can be implemented to existing wireless communication device including both NFC in ALM and PLM modes.

[0070] The above is a description of embodiments of an NFC device in accordance with the present invention. It is foreseeable that those skilled in the art can and will design alternative NFC devices based on this disclosure that infringe upon this invention as set forth in the following claims.

Claims

1. A method performed by a Near Field Communication...
A Near Field Communication, NFC, card configured to perform any of the methods according to claims 1-3.

Patentansprüche

1. Verfahren, das von einer Nahfeldkommunikations(NFC)-Karte durchgeführt wird, die einen Speicher (420), ein Trägerfrequenz-Offset(CFO)-Schätzmodul (410), ein Abtastverstärkungsmodul (930) und einen Hochfrequenz(HF)-Sender umfasst, wobei das Verfahren...

2. The method according to claim 1, wherein the step of estimating the carrier frequency offset is triggered upon detecting a RF magnetic field from the NFC reader.

3. The method according to claim 1 or 2, wherein the step of estimating the carrier frequency offset comprises:

   obtaining an in-phase component (I) and a quadrature phase component (Q) for a plurality of samples of an input signal, received by the NFC card from the NFC reader, from an Analogue to Digital Converter, ADC, of the NFC card; computing a phase for each sample; computing phase differences between a plurality of adjacent samples from the input signal; averaging the phase differences to obtain the estimated carrier frequency offset; and storing the estimated carrier frequency offset in the memory of the NFC card.

4. A Near Field Communication, NFC, card configured to perform any of the methods according to claims 1-3.

5. The method comprising:

   a.) estimating, by the CFO estimation module (410), a CFO, between a carrier frequency of a NFC reader and a carrier frequency of the NFC card (step 310), wherein a positive estimated CFO indicates that the carrier frequency of the NFC reader is larger than the carrier frequency of the NFC card and a negative estimated CFO indicates that the carrier frequency of the NFC reader is smaller than the carrier frequency of the NFC card,

   b.) receiving, by the sample adjustment module (930), an input baseband sample stream and setting, by the sample adjustment module (930), n, k and Acc to zero, wherein n is an input sample number of a sample input to the sample adjustment module (930) and input sample [n] indicates an (n + 1) - th input sample, k is an output sample number of a sample output from the sample adjustment module (930) and output sample [k] indicates an (k + 1) - th output sample, wherein Acc indicates an accumulation of estimated CFOs (steps 1005, 1010),

   c.) retrieving, by the sample adjustment module (930), the estimated CFO from the memory (420),

   d.) adding, by the sample adjustment module (930), an absolute value of the estimated CFO to Acc (step 1015),

   e.) determining, by the sample adjustment module (930), whether the estimated CFO is greater than zero (step 1030),

   f.) in case of no in step e.), outputting, by the sample adjustment module (930), output sample [k] with output sample [k] = input sample [n] (step 1025),

   g.) in case of yes in step e.), determining, by the sample adjustment module (930), whether the estimated CFO is greater than zero (step 1030),

   h.) in case of no in step g.), incrementing, by the sample adjustment module (930), n by one (step 1034),

   i.) after step h.), outputting, by the sample adjustment module (930), output sample [k] with output sample [k] = input sample [n] (step 1036),

   j.) after step i.), determining, by the sample adjustment module (930), Acc as Acc = Acc - sampling frequency (step 1050),

   k.) after step j.) or after step f.), determining, by the sample adjustment module (930), whether there is a further input sample after input sample [n] (step 1055),

   l.) in case of yes in step k.), incrementing, by the sample adjustment module (30), n and k by one and returning to step d.) (step 1060),

   m.) in case of yes in step g.), outputting, by the sample adjustment module (930), output sample [k] = input sample [n] and subsequently incrementing k by one (step 1040, step 1044),

   n.) after step m.), outputting, by the sample adjustment module (930), output sample [k] = input sample [n] and going to step j.) (step 1046),

   o.) in case of no in step k.) going, by the sample adjustment module (930), to step p.),

   p.) modulating the radio frequency, RF, transmitter based on the output samples of the sample adjustment module (930).
CFO anzeigt, dass die Trägerfrequenz des NFC-Lesers kleiner als die Trägerfrequenz der NFC-Karte ist.

1. Verfahren, das für die Dämpfung von Eingangs-Basisband-Abtastwertestroms durch das Abtastwertanpassungsmodul (930) und Einstellen durch das Abtastwertanpassungsmodul (930) von n, k und Acc auf Null, wobei n eine Eingangsabtastwertnummer eines in das Abtastwertanpassungsmodul (930) eingegebenen Abtastwertes ist und Eingangsabtastwert \([n]\) einen \((n + 1)\)-ten Eingangsabtastwert angibt, k eine Ausgangsabtastwertnummer eines vom Abtastwertanpassungsmodul (930) ausgegebenen Abtastwertes ist und Ausgangsabtastwert \([k]\) einen \((k + 1)\)-ten Ausgangsabtastwert angibt, wobei Acc eine Ansammlung von geschätzten CFOs angibt (Schritte 1005, 1010).

2. Abfragen des geschätzten CFO durch das Abtastwertanpassungsmodul (930) aus dem Speicher (420),

3. Addieren eines Absolutwertes des geschätzten CFO zu Acc durch das Abtastwertanpassungsmodul (930) (Schritt 1015),

4. Bestimmen, das Abtastwertanpassungsmodul (930), ob die Acc größer als eine Abtastfrequenz der NFC-Karte ist (Schritt 1020),

5. Falls nein in Schritt e.), Ausgeben, durch das Abtastwertanpassungsmodul (930), von Ausgangsabtastwert \([k]\) mit Ausgangsabtastwert \([k]\) = Eingangsabtastwert \([n]\) (Schritt 1025),

6. Falls ja in Schritt e.), Bestimmen, durch das Abtastwertanpassungsmodul (930), ob der geschätzte CFO größer als Null ist (Schritt 1030),

7. Falls nein in Schritt g.), Inkrementieren, durch das Abtastwertanpassungsmodul (930), von n um eins (Schritt 1034),

8. Ausgeben, durch das Abtastwertanpassungsmodul (930), von Ausgangsabtastwert \([k]\) mit Ausgangsabtastwert \([k]\) = Eingangsabtastwert \([n]\) (Schritt 1036),

9. Mit dem Schritt h.) Ausgeben, durch das Abtastwertanpassungsmodul (930), von Acc als Acc = Acc - Abtastfrequenz (Schritt 1050),

10. Nach Schritt j.) oder nach Schritt f.) Bestimmen, durch das Abtastwertanpassungsmodul (930), ob es einen weiteren Eingangsabtastwert nach Eingangsabtastwert \([n]\) gibt (Schritt 1055),

11. Falls ja in Schritt k.), Inkrementieren, durch das Abtastwertanpassungsmodul (30), von n und k um eins und Zurückkehren zu Schritt d.) (Schritt 1060),

12. Falls ja in Schritt g.), Ausgeben, durch das Abtastwertanpassungsmodul (930), von Ausgangsabtastwert \([k]\) = Eingangsabtastwert \([n]\) und anschließendes Inkrementieren von k um eins (Schritt 1040, Schritt 1044),

13. Ausgeben, durch das Abtastwertanpassungsmodul (930), von Ausgangsabtastwert \([k]\) = Eingangsabtastwert \([n]\) und Übergehen zu Schritt j.) (Schritt 1046).

Revendications

1. Procédé, réalisé par une carte de communication en champ proche (NFC) comprenant une mémoire (420), un module d’estimation de décalage de fréquence porteuse (410), un module de réglage d’échantillon (930) et un émetteur radiofréquence (RF), le procédé consistant :

   a.) à estimer, au moyen du module d’estimation de décalage de fréquence porteuse (CFO) (410), un décalage CFO, entre une fréquence porteuse d’un lecteur de communication NFC et une fréquence porteuse de la carte de communication NFC (étape 310), dans lequel un décalage CFO estimé positif indique que la fréquence porteuse du lecteur de communication NFC est plus importante que la fréquence porteuse de la
carte de communication NFC et un décalage CFO estimé négatif indique que la fréquence porteuse du lecteur de communication NFC est plus petite que la fréquence porteuse de la carte de communication NFC.

b.) à recevoir, au moyen du module de réglage d'échantillon (930), un flux d'échantillon de bande de base d'entrée et à régler, au moyen du module de réglage d'échantillon (930), n, k et Acc à zéro, dans lequel n est le nombre d'échantillons d'entrée d'une entrée d'échantillon dans le module de réglage d'échantillon (930) et l'échantillon d'entrée [n] indique un (n + 1)ème échantillon d'entrée, k est un nombre d'échantillons de sortie d'une sortie d'échantillon du module de réglage d'échantillon (930) et l'échantillon de sortie [k] indique un (k + 1)ème échantillon de sortie, dans lequel Acc indique une accumulation de décalages CFO estimés (étapes 1005, 1010).

c.) à récupérer, au moyen du module de réglage d'échantillon (930), le décalage CFO estimé à partir de la mémoire (420).

d.) à ajouter, au moyen du module de réglage d'échantillon (930), une valeur absolue du décalage CFO estimé à Acc (étape 1015).

e.) à déterminer, au moyen du module de réglage d'échantillon (930), si Acc est supérieur à une fréquence d'échantillonnage de la carte de communication NFC (étape 1020).

f.) dans le cas d’un non à l’étape e.), à fournir en sortie, au moyen du module de réglage d’échantillon (930), l’échantillon de sortie de [k] avec l’échantillon de sortie [k] = l’échantillon d’entrée [n] (étape 1025).

g.) dans le cas d’un oui à l’étape e.), à déterminer, au moyen du module de réglage d’échantillon (930), si le décalage CFO estimé est supérieur à zéro (étape 1030).

h.) dans le cas d’un non à l’étape g.), à incrémenter, au moyen du module de réglage d’échantillon (930), n de un (étape 1034).

i.) après l’étape h.), à fournir en sortie, au moyen du module de réglage d’échantillon (930), l’échantillon de sortie de [k] avec l’échantillon de sortie [k] = l’échantillon d’entrée [n] (étape 1036).

j.) après l’étape i.), à déterminer, au moyen du module de réglage d’échantillon (930), Acc en tant que Acc = Acc - fréquence d’échantillonnage (étape 1050).

k.) après l’étape j.) ou après l’étape f.), à déterminer, au moyen du module de réglage d’échantillon (930), s’il y a un autre échantillon d’entrée après l’échantillon d’entrée [n] (étape 1055).

l.) dans le cas d’un oui à l’étape k.), à incrémenter, au moyen du module de réglage d’échantillon (30), n et k de un et à retourner à l’étape d.) (étape 1060).

m.) dans le cas d’un oui à l’étape g.), à fournir en sortie, au moyen du module de réglage d’échantillon (930), l’échantillon de sortie [k] = l’échantillon d’entrée [n] et, par la suite, à incrémenter k de un (étape 1040, étape 1044).

n.) après l’étape m.), à fournir en sortie, au moyen du module de réglage d’échantillon (930), l’échantillon de sortie [k] = l’échantillon d’entrée [n] et à aller à l’étape j.) (étape 1046).

o.) dans le cas d’un non à l’étape k.), à aller, au moyen du module de réglage d’échantillon (930), à l’étape p.).

p.) à moduler l’émetteur radiofréquence (RF) en se basant sur les échantillons de sortie du module de réglage d’échantillon (930).

2. Procédé selon la revendication 1, dans lequel l’étape d’estimation du décalage de fréquence porteuse est déclenchée lors de la détection d’un champ magnétique RF à partir du lecteur de communication NFC.

3. Procédé selon la revendication 1 ou 2, dans lequel l’étape d’estimation du décalage de fréquence porteuse consiste :

à obtenir une composante en phase (I) et une composante de phase en quadrature (Q) pour une pluralité d’échantillons d’un signal d’entrée, reçu par la carte de communication NFC en provenance du lecteur de communication NFC, en provenance d’un convertisseur analogique-numérique (ADC) de la carte de communication NFC ;
à calculer une phase pour chaque échantillon ;
à calculer des différences de phase entre une pluralité d’échantillons adjacents à partir du signal d’entrée ;
à faire la moyenne des différences de phase pour obtenir le décalage de fréquence porteuse estimé ; et
à stocker le décalage de fréquence porteuse estimé dans la mémoire dans la carte de communication NFC.

4. Carte de communication en champ proche (NFC) configurée pour réaliser l’un quelconque des procédés selon les revendications 1 à 3.
Figure 1 (Prior art)
Figure 2
Start

Detect RF magnetic field

Estimate carrier frequency offset

Demodulate received signal

TX mode?

No

Yes

Encode input bit stream and generate subcarrier sample

Adjust digital transmission sample

RF modulation

End

Figure 3
Figure 4

Figure 5
Figure 6

Start

605

Obtaining I and Q components

615

Compute the phase of the complex signal

620

Compute difference between phase at t=i and t=(i+1)

625

Average the difference

630

Save in memory

End
1. Start
2. Input sample stream
3. Set n, k and Acc to zero
4. Acc = Acc + |offset freq|
5. Check if Acc > sampling frequency?
   a. Yes: Output[k] = input sample[n]
   b. No: Check if Offset freq > 0?
      c. Yes: Output[k] = input sample[n]
      d. No: n = n+1
6. Output[k] = input sample[n]
7. Acc = Acc - sampling freq
8. Check if last input sample stream?
   a. Yes: End
   b. No: k = k+1
9. Repeat steps 3-8 until all samples are processed.
Start

Input sample stream

Set Acc to zero

Acc = Acc + |offset freq|

Acc > data rate?

Yes → N = Bit_Len

No → Acc = Acc – data rate

Offset freq > 0?

Yes → N = Bit_Len + 1

No → N = Bit_Len - 1

Generate DBB sample for 1 bit duration based on value of N

Last input sample stream?

Yes → End

No
Figure 12
REFERENCES CITED IN THE DESCRIPTION

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