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(54) START-UP CIRCUIT

ANLAUSCHALTUNG

CIRCUIT DE DÉMARRAGE

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Description

[0001] Start-up circuits are an essential building block for the construction of many integrated circuits, in particular circuits that have a number of possible stable states such as bandgap voltage reference circuits, oscillators, and flip-flops.

[0002] As an example, bandgap voltage reference circuits are used to provide a temperature-stable voltage reference. Such a bandgap reference circuit operates using a voltage difference between two transistors operated at different current densities to produce an output voltage with low temperature dependence. A silicon-based bandgap circuit will usually produce an output voltage of around 1.25 V, close to the voltage required for a charge carrier (i.e. an electron or a hole) to overcome the 1.22 eV bandgap associated with silicon at absolute zero.

[0003] There are two operating points at which the two transistors draw an identical drain current when the same gate-source voltage is applied to each. When operated at either of these points, the bandgap reference circuit is stable over a wide range of temperatures. The first is what is known as the "zero operating point", in which the voltage applied and the drain currents are all zero - a situation which is of little interest for producing a reference voltage. The "non-zero operating point" exists at a finite, non-zero voltage which when applied across the gate-source interface of the two transistors, causes the same current to flow through each transistor.

[0004] Such a bandgap reference is stable at each of these operating points and will converge towards one or the other whenever possible. It is clear therefore that while there are two possible operating points, only the normal operating point is of interest with a view to creating a stable, non-zero reference voltage. When such a bandgap reference circuit is powered on with no external voltages applied, more often than not it will tend to stabilise at the zero operating point. A start-up circuit is therefore used in order to give the bandgap reference circuit a "kick" (i.e. an "impulse" or a "transient event") in order to force it towards the non-zero operating point as required. An example for a band-gap reference voltage generating circuit is given in US2007/0200616.

[0005] One conventional solution is to sense the zero operating point and inject a current into a transistor of the bandgap reference circuit. This can be used to force the bandgap reference circuit to a desired operating point with relative ease, but can lead to large currents on the output of the circuit which, if connected to external circuits, may cause damage. This start-up circuitry will also draw small amounts of current, which will cause an error in the output voltage. This is particularly an issue for smaller device fabrication sizes such as 16 nm and 28 nm.

[0006] When viewed from a first aspect, the present invention provides a start-up circuit arranged to initialise a circuit portion with a zero stable point and a non-zero stable point, the start-up circuit comprising:

- a capacitive voltage divider including a first capacitor in series with a second capacitor that generates a divider bias voltage between said first and second capacitors at a divider node;
- a differential amplifier including a first amplifier input, a second amplifier input, and an amplifier output connected to the divider node;
- a first driver transistor arranged such that a gate terminal of the first driver transistor is connected to the divider node, and a drain terminal of the first driver transistor is connected to both a first start-up output and the first amplifier input; and
- a second driver transistor arranged such that a gate terminal of the second driver transistor is connected to the divider node, and a drain terminal of the second driver transistor is connected to both a second start-up output and the second amplifier input;

wherein the start-up circuit is arranged such that the differential amplifier controls the divider bias voltage and drives the circuit portion to the non-zero stable point.

[0007] Thus it will be seen by those skilled in the art that the present invention provides a start-up circuit that can be used to initialise a circuit portion such as a bandgap voltage reference circuit to a desired state. The capacitive voltage divider provides the initial kick to the system on power-up. Due to the voltage divider, a small divider bias voltage causes the driver transistors to open, allowing a small current to flow through each, which in turn increases the voltage applied to the amplifier inputs. The amplifier then permits a greater current to flow through itself, reducing the bias voltage (i.e. the amplifier pulls down the bias voltage), which causes the driver transistors to permit more current to flow therethrough. By initialising the circuit in this manner, the currents generated within the bandgap circuit are kept to a minimum. Should the currents from the bandgap reference circuit be mirrored for use in other external circuits, the risk of damaging said external circuits with excessive current is reduced.

[0008] The Applicant has appreciated that conventional start-up circuits often have a capacitor connected between the power supply or ground and the driver transistors for stability and so implementing the invention requires only one additional capacitor. Conventional start-up circuits use this capacitor to stabilise an amplifier within the start-up circuit. The second capacitor can be chosen to create the desired capacitance ratio as discussed later.

[0009] While there are a number of differential amplifier arrangements suited to the invention, in a set of embodiments the differential amplifier comprises a long tailed pair arrangement including first and second mirror transistors, and first and second differential pair transistors. In a set of embodiments, the mirror transistors are p-channel metal-oxide-semiconductor (PMOS) field-effect
In a set of embodiments, the first and second mirror transistors are n-channel metal-oxide-semiconductor (NMOS) field-effect transistors. This choice of PMOS and NMOS transistors is particularly suitable for use between a positive supply rail and ground as conventional in integrated circuit design, but the invention could be implemented by reversing the transistor types and swapping the polarity of the voltage supply.

[0010] In a set of embodiments, the first and second mirror transistors are arranged such that their respective source terminals are connected to a supply voltage and their respective gate terminals are connected together. In a set of embodiments, the first mirror transistor is diode-connected (i.e. its drain terminal is connected to its gate terminal).

[0011] In a set of embodiments, the drain terminal of the first mirror transistor is connected to the drain terminal of the first differential pair transistor and the drain terminal of the second mirror transistor is connected to the drain terminal of the second differential pair transistor. This ensures that the same current flows through each "leg" of the differential amplifier.

[0012] In a set of embodiments, the source terminals of the first and second differential pair transistors are connected to each other. In a set of embodiments, the source terminals of the first and second differential pair transistors are connected to a current source. In a set of embodiments, the current source is a current mirror.

[0013] In a set of embodiments, the circuit comprises a current mirror output transistor arranged such that its gate terminal is connected to the divider node. In a set of embodiments, the drain terminal of the current mirror output transistor is connected to an external current mirror. This external current mirror provides an output current for external circuitry and mirrors the current flowing through the circuit portion.

[0014] An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 shows the stable points of a typical bandgap reference voltage circuit;
Fig. 2 is a circuit diagram of a start-up circuit in accordance with an embodiment of the invention; and Fig. 3 is a timing diagram showing the typical operation of the start-up circuit of Fig. 2.

[0015] Fig. 1 shows the stable points of a typical bandgap reference voltage circuit with two reference transistors. There are two points at which the current-voltage plots for each reference transistor meet, i.e. where for a given current density, the voltage across the transistors is the same. These are the desirable operating points where the reference voltage taken as the output has a flat temperature response.

[0016] There is a zero stable point 200 at the origin, which is of little practical interest as no currents flow at this point. There is also a non-zero stable point 202, at which the reference circuit functions as desired. The purpose of the start-up circuit described herein is therefore to drive the bandgap circuit to the non-zero operating stable point 202 rather than the zero one 200.

[0017] Fig. 2 is a circuit diagram of a start-up circuit 2 in accordance with an embodiment of the invention. The start-up circuit is configured to initialise a bandgap reference circuit 4 with the stable points illustrated in Fig. 1. The bandgap reference circuit 4 comprises a pair of n-channel metal-oxide-semiconductor ("NMOS") field-effect transistors ("FET"s or "MOSFET"s) 6, 8 - one transistor 8 of which is connected in series with a fixed resistor 10 via its drain terminal.

[0018] The two bandgap transistors 6, 8 are each driven by respective p-channel metal-oxide-semiconductor ("PMOS") field-effect transistors 12, 14. The PMOS driver transistors 12, 14 are arranged such that their source terminals are connected to the supply voltage 40. One of the driver transistors 12 has its drain terminal connected to the drain terminal of one of the bandgap transistors 6, while the drain terminal of the other driver transistor 14 is connected to the drain terminal of the other bandgap transistor 8 via the fixed resistor 10. Both bandgap transistors 6, 8 are diode-connected (i.e. their respective gate and drain terminals are connected to one another). For increased temperature sensitivity, the bandgap transistors 6, 8 may be implemented using NPN bipolar junction transistors (BJTs) instead of NMOSFETs.

[0019] The driver transistors 12, 14 and bandgap reference circuit 4 form two distinct "paths". The first is defined as the path from supply voltage 40 to ground 44 through driver transistor 12 and bandgap transistor 6, while the second is defined as the path from supply voltage 40 to ground 44 through driver transistor 14, fixed resistor 10 and bandgap transistor 8.

[0020] The drain terminals of the driver transistors 12, 14 are each connected to the respective gate terminals of NMOS differential pair transistors 20, 22. Along with two PMOS current mirror transistors 24, 26, these differential pair transistors 20, 22 form a single-sided differential amplifier.

[0021] The PMOS current mirror transistors 24, 26 are arranged such that their source terminals are connected to the supply voltage 40, while their drain terminals are each connected to the respective drain terminals of the differential pair transistors 20, 22. The gate terminals of the current mirror transistors 24, 26 are connected to one another, and the drain and gate terminals of one current mirror transistor 26 are connected in order to place it in a diode-connected configuration.

[0022] A capacitive voltage divider is formed by two capacitors 16, 18 which are connected between the positive supply rail 40 and ground 44. This arrangement leads to a non-zero voltage located at the node 48 between the two capacitors.

[0023] The drain terminals of one of the current mirror transistors 24 and its associated differential pair transistor 20 are connected directly to the node 48 between the...
two capacitors 16, 18. The node 48 is further connected to the gate terminals of the two divider transistors and of a PMOS output current mirror transistor 36, which feeds current to a current mirror 38, which in turn produces an output current 46.

[0024] The source terminals of the differential pair transistors 20, 22 are both connected to an NMOS current source transistor 28, which acts as a current source for the differential amplifier. It is arranged to mirror the current passing through an NMOS transistor 30, which itself is connected to an input current 42.

[0025] A voltage difference between the two transistors 6, 8 when operated at different current densities due to the fixed resistor 10 is used as a reference voltage by external circuits. The bandgap circuit 4 is stable when operated at a point at which the two transistors 6, 8 draw an identical drain current when the same gate-source voltage is applied to each.

[0026] Fig. 3 is a timing diagram showing the typical operation of the start-up circuit 2 of Fig. 2.

[0027] When the circuit 2 is switched on at initial time 100, there is a time-varying component on the supply voltage 40 and thus the input current 42 due to the transient response of the circuit. While the capacitors 16, 18 are effectively open circuit to DC (i.e. non-time-varying) signals, they provide charge injection due to the resulting time-varying voltage. The voltage at the node 48 is determined - at least initially when the transistors connected thereto are "off" - by the magnitude of the time-varying voltage present on the supply rail, multiplied by the ratio of the capacitance of capacitor 16 to the total capacitance of both capacitors 16, 18 combined. Since the voltage at the node 48 is necessarily smaller than the supply voltage 40, there is a negative gate-source voltage applied across the two driver transistors 12, 14. This causes each of the driver transistors 12, 14 to switch "on" and conduct a small current 52, 54 respectively (only the current 52 through driver transistor 12 is shown for illustrative purposes).

[0028] As the driver transistors 12, 14 conduct more current, their drain terminals are driven to increasingly higher voltages, which drives the voltage applied at the gate terminals of the differential pair transistors 20, 22 to higher voltages accordingly. This increases the gate-source voltage of each of the differential pair transistors 20, 22, causing them to switch on and also begin conducting current 50, 56.

[0029] At time 102, once sufficient current 50 begins flowing through the differential pair transistor 20, the voltage at node 48 is pulled down accordingly.

[0030] Since the voltage at the node 48 is then reduced, the driver transistors 12, 14 have a yet higher negative gate-source voltage applied to them, and thus conduct yet more current.

[0031] This cyclical arrangement drives the bandgap reference circuit 4 away from its zero operating point 200 and towards its non-zero operating point 202 (see Fig. 1). Eventually at time 104, the current through each of these paths will reach an equilibrium point wherein the voltages applied to the gates of the differential pair transistors 20, 22 is equal, and the node 48 remains stable at the resulting differential voltage. At this stage, the bandgap circuit 4 has been stabilised to its non-zero operating point and the start-up circuit is now effectively "switched off" (in practice, drawing a minimal amount of current).

[0032] Throughout the operation of the circuit, the output current 46 remains within reasonable levels, with the initial spike at time 100 being substantially the same magnitude as its value during normal operation from time 104 onwards.

[0033] Thus it will be seen that a start-up circuit with a controlled output current has been described herein. Although a particular embodiment has been described in detail, it will be appreciated by those skilled in the art that many variations and modifications are possible using the principles of the invention set out herein.

Claims

1. A start-up circuit (2) arranged to initialise a circuit portion (4) with a zero stable point (200) and a non-zero stable point (202), the start-up circuit (2) comprising:

   a capacitive voltage divider including a first capacitor (16) in series with a second capacitor (18) that generates a divider bias voltage between said first and second capacitors (16, 18) at a divider node (48);
   a differential amplifier including a first amplifier input (20), a second amplifier input (22), and an amplifier output connected to the divider node (48);
   a first driver transistor (12) arranged such that a gate terminal of the first driver transistor (12) is connected to the divider node (48), and a drain terminal of the first driver transistor (12) is connected to both a first start-up output and the first amplifier input; and
   a second driver transistor (14) arranged such that a gate terminal of the second driver transistor (14) is connected to the divider node (48), and a drain terminal of the second driver transistor (14) is connected to both a second start-up output and the second amplifier input;

   wherein the start-up circuit (2) is arranged such that the differential amplifier controls the divider bias voltage and drives the circuit portion to the non-zero stable point (202).

2. The start-up circuit (2) as claimed in claim 1, wherein the differential amplifier comprises a long tailed pair arrangement including first and second mirror tran-
3. The start-up circuit (2) as claimed in claim 2, wherein the mirror transistors (24, 26) are p-channel metal-oxide-semiconductor (PMOS) field-effect transistors.

4. The start-up circuit (2) as claimed in claim 2 or 3, wherein the differential pair transistors (20, 22) are n-channel metal-oxide-semiconductor (NMOS) field-effect transistors.

5. The start-up circuit (2) as claimed in any of claims 2 to 4, wherein the first and second mirror transistors (24, 26) are arranged such that their respective source terminals are connected to a supply voltage and their respective gate terminals are connected together.

6. The start-up circuit (2) as claimed in any of claims 2 to 5, wherein the first mirror transistor (26) is diode-connected.

7. The start-up circuit (2) as claimed in any of claims 2 to 6, wherein the drain terminal of the first mirror transistor (26) is connected to the drain terminal of the first differential pair transistor (22) and the drain terminal of the second mirror transistor (24) is connected to the drain terminal of the second differential pair transistor (20).

8. The start-up circuit (2) as claimed in any of claims 2 to 7, wherein the source terminals of the first and second differential pair transistors (20, 22) are connected to each other.

9. The start-up circuit (2) as claimed in any of claims 2 to 8, wherein the source terminals of the first and second differential pair transistors (20, 22) are connected to a current source.

10. The start-up circuit (2) as claimed in claim 9, wherein the current source is a current mirror (28, 30).

11. The start-up circuit (2) as claimed in any preceding claim, wherein the circuit comprises a current mirror output transistor (36) arranged such that its gate terminal is connected to the divider node.

12. The start-up circuit (2) as claimed in claim 11, wherein the drain terminal of the current mirror output transistor (36) is connected to an external current mirror (38).

Patentansprüche

1. Anlaufschaltung (2), die angeordnet ist, um einen Schaltungsabschnitt (4) mit einem stabilen Nullpunkt (200) und einem stabilen Nicht-Nullpunkt (202) zu initialisieren, wobei die Anlaufschaltung (2) umfasst:
   
   - einen kapazitiven Spannungsteiler einschließlich eines ersten Kondensators (16) in Reihe mit einem zweiten Kondensator (18), der an einem Teilknoten (48) eine Teillervorspannung zwischen dem ersten und zweiten Kondensator (16, 18) erzeugt;
   - einen Differenzverstärker einschließlich eines ersten Verstärkereingangs (20), eines zweiten Verstärkereingangs (22) und eines Verstärkerausgangs, der mit dem Teilknoten (48) verbunden ist;
   - einen ersten Treibertransistor (12), der so angeordnet ist, dass ein Gate-Anschluss des ersten Treibertransistors (12) mit dem Teilknoten (48) verbunden ist, und ein Drain-Anschluss des ersten Treibertransistors (12) sowohl mit dem ersten Anlaufausgang als auch mit dem ersten Verstärkereingang verbunden ist; und
   - einen zweiten Treibertransistor (14), der so angeordnet ist, dass ein Gate-Anschluss des zweiten Treibertransistors (14) mit dem Teilknoten (48) verbunden ist, und ein Drain-Anschluss des zweiten Treibertransistors (14) sowohl mit einem zweiten Anlaufausgang als auch mit dem zweiten Verstärkereingang verbunden ist; wobei die Anlaufschaltung (2) so angeordnet ist, dass der Differenzverstärker die Teillervorspannung steuert und den Schaltungsabschnitt zu dem stabilen Nicht-Nullpunkt (202) treibt.

2. Anlaufschaltung (2) nach Anspruch 1, wobei der Differenzverstärker eine langschwänzige Paaranordnung einschließlich eines ersten und zweiten Spiegeltransistors (24, 26) und eines ersten und zweiten Differenzpaartransistors (20, 22) umfasst.

3. Anlaufschaltung (2) nach Anspruch 2, wobei die Spiegeltransistoren (24, 26) p-Kanal-Metalloxidhalbleiter (PMOS)-Feldeffecttransistoren sind.

4. Anlaufschaltung (2) nach Anspruch 2 oder 3, wobei die Differenzpaartransistoren (20, 22) n-Kanal-Metalloxidhalbleiter (NMOS)-Feldeffecttransistoren sind.

5. Anlaufschaltung (2) nach einem der Ansprüche 2 bis 4, wobei der erste und zweite Spiegeltransistor (24, 26) so angeordnet sind, dass ihre jeweiligen Source-Anschlüsse mit einer Versorgungsspannung verbunden sind und ihre jeweiligen Gate-Anschlüsse miteinander verbunden sind.
6. Anlaufschaltung (2) nach einem der Ansprüche 2 bis 5, wobei der erste Spiegeltransistor (26) als Diode geschaltet ist.

7. Anlaufschaltung (2) nach einem der Ansprüche 2 bis 6, wobei der Drain-Anschluss des ersten Spiegeltransistors (26) mit dem Drain-Anschluss des ersten Differenzpaartransistors (22) verbunden ist und der Drain-Anschluss des zweiten Spiegeltransistors (24) mit dem Drain-Anschluss des zweiten Differenzpaartransistors (20) verbunden ist.

8. Anlaufschaltung (2) nach einem der Ansprüche 2 bis 7, wobei die Source-Anschlüsse des ersten und zweiten Differenzpaartransistors (20, 22) miteinander verbunden sind.

9. Anlaufschaltung (2) nach einem der Ansprüche 2 bis 8, wobei die Source-Anschlüsse des ersten und zweiten Differenzpaartransistors (20, 22) mit einer Stromquelle verbunden sind.

10. Anlaufschaltung (2) nach Anspruch 9, wobei die Stromquelle ein Stromspiegel (28, 30) ist.

11. Anlaufschaltung (2) nach einem der vorstehenden Ansprüche, wobei die Schaltung einen Stromspiegel-Ausgangstransistor (36) umfasst, der so angeordnet ist, dass sein Gate-Anschluss mit dem Teilerknoten verbunden ist.

12. Anlaufschaltung (2) nach Anspruch 11, wobei der Drain-Anschluss des Stromspiegel-Ausgangstransistors (36) mit einem externen Stromspiegel (38) verbunden ist.

Re Vendications

1. Circuit de démarrage (2) conçu pour initialiser une portion de circuit (4) avec un point stable nul (200) et un point stable non nul (202), le circuit de démarrage (2) comprenant :
   un diviseur de tension capacitif comportant un premier condensateur (16) en série avec un second condensateur (18) qui génère une tension de polarisation de diviseur entre les dits premier et second condensateurs (16, 18) au niveau d’un noeud de diviseur (48) ;
   un amplificateur différentiel comportant une première entrée d’amplificateur (20), une seconde entrée d’amplificateur (22), et une sortie d’amplificateur connectées au noeud de diviseur (48) ;
   un premier transistor pilote (12) conçu de sorte qu’une borne de grille du premier transistor pilote (12) soit connectée au noeud de diviseur (48), et une borne de drain du premier transistor pilote (14) conçu de sorte qu’une borne de grille du second transistor pilote (14) soit connectée au noeud de diviseur (48), et une borne de drain du second transistor pilote (14) soit connectée à la fois à une seconde sortie de démarrage et à une première sortie de démarrage et à la première entrée d’amplificateur ; et
   un second transistor pilote (16) conçu de sorte qu’une borne de grille du second transistor pilote (16) soit connectée au noeud de diviseur (48), et une borne de drain du second transistor pilote (16) soit connectée à la fois à une seconde sortie de démarrage et à la première entrée d’amplificateur ;
   dans lequel le circuit de démarrage (2) est conçu de sorte que l’amplificateur différentiel commande la tension de polarisation de diviseur et pilote la portion de circuit au point stable non nul (202).

2. Circuit de démarrage (2) selon la revendication 1, dans lequel l’amplificateur différentiel comprend un agencement de paire à longue queue comportant des premier et second transistors miroirs (24, 26) et des premier et second transistors à paire différentielle (20, 22).

3. Circuit de démarrage (2) selon la revendication 2, dans lequel les transistors miroirs (24, 26) sont des transistors à effet de champ à semi-conducteur à oxyde de métal à canal p (PMOS).

4. Circuit de démarrage (2) selon la revendication 2 ou 3, dans lequel les transistors à paire différentielle (20, 22) sont des transistors à effet de champ à semi-conducteur à oxyde de métal à canal n (NMOS).

5. Circuit de démarrage (2) selon l’une quelconque des revendications 2 à 4, dans lequel les premier et second transistors miroirs (24, 26) sont conçus de sorte que leurs bornes de source respectives soient connectées à une tension d’alimentation et leurs bornes de grille respectives soient connectées ensemble.

6. Circuit de démarrage (2) selon l’une quelconque des revendications 2 à 5, dans lequel le premier transistor miroir (26) est connecté par diode.

7. Circuit de démarrage (2) selon l’une quelconque des revendications 2 à 6, dans lequel la borne de drain du premier transistor miroir (26) est connectée à la borne de drain du premier transistor à paire différentielle (22) et la borne de drain du second transistor miroir (24) est connectée à la borne de drain du second transistor à paire différentielle (20).

8. Circuit de démarrage (2) selon l’une quelconque des revendications 2 à 7, dans lequel les bornes de source des premier et second transistors à paire différentielle (20, 22) sont connectées l’une à l’autre.

9. Circuit de démarrage (2) selon l’une quelconque des revendications 2 à 8, dans lequel les bornes de source des premier et second transistors à paire différentielle (20, 22) sont connectées l’une à l’autre.
revendications 2 à 8, dans lequel les bornes de source des premier et second transistors à paire différentielle (20, 22) sont connectées à une source de courant.

10. Circuit de démarrage (2) selon la revendication 9, dans lequel la source de courant est un miroir de courant (28, 30).

11. Circuit de démarrage (2) selon une quelconque revendication précédente, dans lequel le circuit comprend un transistor de sortie de miroir de courant (36) conçu de sorte que sa borne de grille soit connectée au noyau de diviseur.

12. Circuit de démarrage (2) selon la revendication 11, dans lequel la borne de drain du transistor de sortie de miroir de courant (36) est connectée à un miroir de courant externe (38).
REFERENCES CITED IN THE DESCRIPTION

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