DATA WRITE CONTROL APPARATUS AND METHOD

A data write control apparatus and method are disclosed. The method includes: when the write control apparatus is in write-back mode, detecting, by a processor, a quantity of dirty blocks in a first memory; when the quantity of dirty blocks reaches a first preset threshold, separately predicting execution progress of a program run by the processor within a danger time period in the two write modes; when it is predicted that the execution progress of the program run by the processor within the danger time period in write-through mode is faster than the execution progress of the program run by the processor within the danger time period in write-back mode, switching a current data write mode to the write-through mode; and when the write control apparatus is in write-through mode, detecting the quantity of dirty blocks, and when the quantity of dirty blocks decreases to a second preset threshold, switching the current data write mode to the write-back mode.
Description

TECHNICAL FIELD

[0001] The present invention relates to the field of data write control technologies, and in particular, to a data write control apparatus and method.

BACKGROUND

[0002] A nonvolatile SRAM (NV-SRAM) is a storage structure including both an SRAM and an NVM. In a working mode, an electronic apparatus stores data by using an SRAM. After the electronic apparatus encounters a power failure, an NV-SRAM can back up data to an NVM unit. However, after the electronic apparatus encounters a power failure, the nonvolatile SRAM needs to be powered by a relatively large on-chip energy storage capacitor, so as to perform data backup. The capacitor may cause relatively high overheads of a chip area and costs. If a relative small on-chip energy storage capacitor is used, backup may fail due to insufficient electric energy. After the backup fails, a previous successful backup point needs to be rolled back. Rolling back to the previous backup point causes some performance overheads, thereby affecting execution progress of a program.

SUMMARY

[0003] Embodiments of the present invention provide a data write control apparatus and method, so that the program execution efficiency of the write apparatus and method is improved by switching between two different write modes.

[0004] A first aspect of the embodiments of the present invention provides a data write control apparatus, including a level 1 memory, a level 2 memory, and a processor, where the level 1 memory includes a volatile storage unit, the level 2 memory is a nonvolatile storage unit, and a data write mode of the data write control apparatus includes a write-back mode and a write-through mode; and in write-back mode, the processor writes received data to the level 1 memory, and in write-through mode, the processor writes received data to the level 1 memory and the level 2 memory; when the write control apparatus is in write-back mode, the processor detects a quantity of dirty blocks in the first memory; when the quantity of dirty blocks reaches a first preset threshold, separately predicts execution progress of a program run by the processor within a danger time period in the two write modes; and when it is predicted that the execution progress of the program run by the processor within the danger time period in write-through mode is faster than the execution progress of the program run by the processor within the danger time period in write-back mode, switches a current data write mode to the write-through mode; and when the write control apparatus is in write-through mode, the processor detects the quantity of dirty blocks; and when the quantity of dirty blocks decreases to a second preset threshold, switches the current data write mode to the write-back mode.

[0005] Further, according to the first aspect of the embodiments of the present invention, the level 1 memory further includes a nonvolatile storage unit; after the data write control apparatus encounters a power failure, data in the volatile storage unit is backed up to the nonvolatile storage unit; and the first preset threshold is a maximum quantity of dirty blocks that can be backed up by the first memory.

[0006] Further, according to the first aspect of the embodiments of the present invention, a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-back mode is used is:

$$E(G - R) = k(L - \frac{1}{\lambda} - t_s) + ke^{-\lambda(L + \frac{1}{\lambda} - t_s)}$$

where $k$ is the execution progress of the program run by the processor within a unit time in write-back mode; $L$ is a length of the preset danger time period; if a time when the quantity of dirty blocks reaches the first preset threshold is used as a zero time, $t_s$ is a time of latest power supply before the zero time; and $1/\lambda$ is an average power supply time of the data write control apparatus that is pre-obtained by means of statistics collection; and a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-through mode is used is:

$$E(G') = k'L$$
where \( k' \) is the execution progress of the program run by the processor within a unit time in write-through mode.

[0007] Further, according to the first aspect of the embodiments of the present invention, the second preset threshold equals the first preset threshold minus 1.

[0008] A second aspect of the embodiments of the present invention provides a data write control method applied in the data write control apparatus, where the data write control apparatus includes a level 1 memory, a level 2 memory, and a processor, the level 1 memory includes a volatile storage unit, the level 2 memory is a nonvolatile storage unit, and a data write mode of the data write control apparatus includes a write-back mode and a write-through mode; and in write-back mode, the processor writes received data to the level 1 memory, in write-through mode, the processor writes received data to the level 1 memory and the level 2 memory; and the method includes:

- when the write control apparatus is in write-back mode, detecting, by the processor, a quantity of dirty blocks in the first memory;
- when the quantity of dirty blocks reaches a first preset threshold, separately predicting execution progress of a program run by the processor within a danger time period in the two write modes;
- when it is predicted that the execution progress of the program run by the processor within the danger time period in write-through mode is faster than the execution progress of the program run by the processor within the danger time period in write-back mode, switching a current data write mode to the write-through mode; and
- when the write control apparatus is in write-through mode, detecting the quantity of dirty blocks; and when the quantity of dirty blocks decreases to a second preset threshold, switching the current data write mode to the write-back mode.

[0009] Further, according to the second aspect of the embodiments of the present invention, the level 1 memory further includes a nonvolatile storage unit; after the data write control apparatus encounters a power failure, data in the volatile storage unit is backed up to the nonvolatile storage unit; and the first preset threshold is a maximum quantity of dirty blocks that can be backed up by the first memory.

[0010] Further, according to the second aspect of the embodiments of the present invention, a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-back mode is used is:

\[
E(G - R) = k(L - \frac{1}{\lambda} - t_s) + k e^{-\lambda t_s} (L + \frac{1}{\lambda} - t_s)
\]

where \( k \) is the execution progress of the program run by the processor within a unit time in write-back mode; \( L \) is a length of the preset danger time period; if a time when the quantity of dirty blocks reaches the first preset threshold is used as a zero time, \( t_s \) is a time when power is supplied to the data write control apparatus within the danger time period; and \( 1/\lambda \) is an average power supply time of the data write control apparatus that is pre-obtained by means of statistics collection; and a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-through mode is used is:

\[
E(G') = k'L
\]

[0011] where \( k' \) is the execution progress of the program run by the processor within a unit time in write-through mode.

[0012] Further, according to the second aspect of the embodiments of the present invention, the second preset threshold equals the first preset threshold minus 1.

[0013] As can be seen, according to the data write control apparatus and method in the embodiments of the present invention, when a data write mode of the data write control apparatus is a write-back mode, a quantity of dirty blocks in a volatile storage unit is detected. When the quantity of dirty blocks reaches a preset threshold, it is determined according to a preset condition whether to switch the data write mode of the data write control apparatus to a write-through mode. When the preset condition is satisfied and the data write mode the data write control apparatus is switched to the write-through mode, the quantity of dirty blocks continues to be detected. When the quantity of dirty blocks is less than a second preset threshold, the data write mode of the data write control apparatus is switched to the write-back mode. In this way, execution performance of a program of the data write control apparatus can be improved.
BRIEF DESCRIPTION OF DRAWINGS

[0014] To describe the technical solutions in the embodiments of the present invention or in the prior art more clearly, the following briefly describes the accompanying drawings required for describing the embodiments or the prior art. Apparently, the accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

FIG. 1 is a structural diagram of a data write apparatus according to a first embodiment of the present invention; FIG. 2 is a schematic diagram of switching between two data write modes of the data write apparatus; and FIG. 3 is a flowchart of a data write method according to a second embodiment.

DESCRIPTION OF EMBODIMENTS

[0015] The following clearly and completely describes the technical solutions in the embodiments of the present invention with reference to the accompanying drawings in the embodiments of the present invention. Apparently, the described embodiments are merely some but not all of the embodiments of the present invention. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

[0016] Technical solutions provided in the embodiments of the present invention are mainly applied in a memory that has both a nonvolatile storage unit and a volatile storage unit, for example, a nonvolatile static random access memory (Nonvolatile Static Random Access Memory, NV-SRAM). When an electronic apparatus using a memory of this structure as an internal memory encounters a power failure, power may be supplied to the memory by using a backup power source on the memory, so that data in the volatile storage unit is backed up to the nonvolatile storage unit. For ease of description, the present invention is described by using the NV-SRAM as an example in the following embodiments. It should be noted that the memory applied in the present invention is not limited to the NV-SRAM, and another memory having the same structure is also within the scope disclosed in the present invention.

[0017] The volatile storage unit in NV-SRAM is a static random access memory (Static Random Access Memory, SRAM), the nonvolatile storage unit is a phase-change random access memory (Phase-change Random Access memory, PCM), and the backup power source is an on-chip energy storage capacitor.

[0018] The technical solutions provided in the present invention are described from different perspectives by using different embodiments below.

First Embodiment

[0019] The first embodiment provides a data write control apparatus 10. The data write control apparatus 10 includes a level 1 memory 11, a level 2 memory 12, and a processor 13. The level 1 memory 11 includes a volatile storage unit 111 and a nonvolatile storage unit 112. The level 2 memory 12 is a nonvolatile storage unit.

[0020] The write control apparatus 10 includes two data write modes, that is, a write-back mode and a write-through mode. In write-back (write-back) mode, data in a received data write request is written to the level 1 memory. In write-through (through-write) mode, data in a received data write request is written to both the level 1 memory 11 and the level 2 memory 12.

[0021] In this embodiment, the level 1 memory 11 is a nonvolatile static random access memory (Nonvolatile Static Random Access Memory, NV-SRAM); the volatile storage unit 111 is a static random access memory (Static Random Access Memory, SRAM); and the nonvolatile storage unit 112 is a phase-change random access memory (Phase-change Random Access memory, PCM). After the data write control apparatus 10 encounters a power failure, power may be supplied to the level 1 memory 11 by using a backup power source 113 on the level 1 memory 11, so that data in the volatile storage unit 111 is backed up to the nonvolatile storage unit 112.

[0022] In write-back mode, when receiving a data write instruction, the processor 13 directly writes data to a storage block 113 in the volatile storage unit 111. The data written to the volatile storage unit 111 is written to the level 2 memory 12 only when the data needs to be replaced in the volatile storage unit 111. A storage block 113 that is written to the volatile storage unit 111 but is not written to the level 2 memory 12 is a dirty block. Each storage block 113 has a dirty block tag, which is used to identify whether the storage block 113 is a dirty block. The volatile storage unit 111 has relatively high data read and write speeds. Therefore, in write-back mode, the data write control apparatus 10 has faster program processing progress. When the data write control apparatus 10 encounters a power failure, data in all dirty blocks in the volatile storage unit 111 needs to be backed up to the nonvolatile storage unit 112. However, because electric energy of the backup power source 113 is limited, when a quantity of dirty blocks exceeds a quantity of dirty blocks whose backup is supported by the backup power source 113, the backup fails. When the backup fails, a program...
needs to be rolled back to a previous successful backup point. This causes high performance overheads, thereby affecting execution progress of the program.

[0023] In write-through mode, when receiving a data write instruction, the processor 13 also writes data to the level 2 memory 12 when writing the data to the storage block 113 of the volatile storage unit 111. In this way, no dirty block is generated. Therefore, no backup failure occurs. However, speeds of reading and writing data by the nonvolatile storage unit 112 are relatively low. Therefore, compared with the write-back mode, in write-through mode, the data write control apparatus 10 has relatively slow program processing progress.

[0024] Therefore, to improve performance of the data write control apparatus 10, the data write control apparatus 10 provided in this embodiment may be switched between the two data write modes, thereby improving the overall program processing progress.

[0025] When the write control apparatus 10 is in write-back mode, the processor 13 detects a quantity of dirty blocks in the first memory 11; when the quantity of dirty blocks reaches a first preset threshold, or the quantity of dirty blocks reaches a first preset threshold, predicts execution progress of a program in the two write modes; and when it is predicted that the execution progress in write-through mode is faster than the execution progress in write-back mode, switches a current data write mode to the write-through mode.

[0026] When the write control apparatus 10 is in write-through mode, the processor 13 detects the quantity of dirty blocks, and when the quantity of dirty blocks reaches a second preset threshold, switches the current data write mode to the write-back mode.

[0027] The first preset threshold is a maximum quantity of dirty blocks that can be backed up by the first memory 11.

[0028] In this embodiment, in an implementation manner, when the quantity of dirty blocks detected by the processor 13 reaches the first preset threshold, the current data write mode is switched to the write-through mode.

[0029] In another implementation manner, when the quantity of dirty blocks detected by the processor 13 reaches the first preset threshold, the execution progress of the program in the two write modes is predicted. In this case, the predicted execution progress of the program is execution progress of the program within a danger time period L that is from a time when the quantity of dirty blocks reaches the first preset threshold to a time when the quantity of dirty blocks is less than the first preset threshold.

[0030] The data write control apparatus 10 in this embodiment is usually a particular detection apparatus, for example, a sensor used for detecting a health status of a human body in a wearable device. Therefore, only one particular program is usually run. The danger time period L in which a quantity of dirty blocks of the running program reaches and is greater than the first preset threshold is basically the same. Therefore, for the particular program, the danger time period L may be obtained in advance.

[0031] In this embodiment, execution progress of a program may be represented by using a percentage. The data write control apparatus 10 runs the particular program. Therefore, a total quantity of instructions of the program is definite. The execution progress of the program may be calculated according to Formula (1):

\[
G(t) = \frac{N_{\text{executed}}(t)}{N_{\text{total}}} \tag{1}
\]

where \(N_{\text{executed}}(t)\) is a quantity of instructions that have been executed, and \(N_{\text{total}}\) is the total quantity of instructions; and if time overheads caused by pipeline stall are ignored, it may be approximately considered that \(G(t)\) linearly increases.

[0032] First, the progress of the program is calculated when the write-back mode is used within the danger time period L.

[0033] As shown in FIG. 2, a curve C1 is a progress curve of the program when the write-back mode is used, and a curve C2 is a progress curve of the program when the write-through mode is used.

[0034] After the program starts running, the data write control apparatus 10 writes data in write-back mode, starts detecting the quantity of dirty blocks; and when the quantity of dirty blocks reaches the first preset threshold, obtains the preset danger time period L, and predicts processing progress of the program in the two write modes in the time period L.

[0035] When the quantity of dirty blocks reaches the first preset threshold, and the write-back mode is not switched to the write-through mode, a process for calculating the processing progress of the executed program is as follows:

[0036] First, a power failure probability of the data write control apparatus 10 is calculated. In actual application, a power failure may occur in different situations. For example, if the data write control apparatus 10 uses a solar power system, a passive power failure occurs when sun is blocked, the sun angle changes, the weather changes, or the like. This feature is represented as memorylessness of a power supply time in terms of a power supply feature, that is, power supply time lengths are not directly associated with one another. Therefore, modeling may be performed on a power supply time by means of exponential distribution:
where \( f(t_{on}) \) is a probability density of the power supply time length, and \( \frac{1}{\lambda} \) is an expectation of the power supply time length.

Then, a formula for calculating a probability that a power failure occurs within the danger time period \( L \) is:

\[
P(F) = P(t_{on} < L) = \int_0^L f(t_{on}) dt_{on} = 1 - e^{-\lambda L}
\]

For a continuous power supply time \( t \), formulas for calculating progress percentages when the two strategies are used are respectively:

\[
G(t) = kt
\]

\[
G'(t) = k't
\]

where \( k \) is a program progress within a unit time when the write-back mode is used, and \( k' \) is a program progress within a unit time when the write-through mode is used.

If a power failure occurs within the danger time period \( L \), a backup failure occurs, and after backup fails, backup rollback occurs. As shown in FIG. 2, if a power failure occurs at a time \( T_e \), a backup failure occurs, and the program needs to be rolled back to a program progress at a time \( T_s \) when this power supply starts. If a start point of the danger time period \( L \), that is, a switching point \( P \), is used as a zero time, progress of the rolled-back program is:

\[
R(t_s) = \begin{cases} 
G(t_s + t_e) & \text{if } t_s < L \\
0 & \text{if } t_s > L 
\end{cases}
\]

where \( T_e < L \) represents that a power failure occurs within the danger time period \( L \); and \( T_e > L \) represents that no power failure occurs within the danger time period \( L \), and the program does not need to be rolled back.

Therefore, if the write-back policy is not switched to the write-through policy at the switching point within the danger time period \( L \), a formula for calculating an expectation of an actual progress percentage \( G-R \) is:

\[
E(G-R) = G(L) - \int_0^L k(t_s + t_e) f(t_e) dt_e = k(L - \frac{1}{\lambda} t_e) + ke^{-\lambda t_e}(L + \frac{1}{\lambda} - t_e)
\]

If the quantity of dirty blocks reaches the first preset value, the data write mode is switched to the write-through mode at the switching point, and

a formula for calculating an expectation of the actual progress percentage \( G-R \) is:

\[
E(G') = kL
\]

The data write mode is switched to the write-through policy only when \( E(G-R) < E(G') \), that is:

\[
E(G-R) - E(G') = k(L - \frac{1}{\lambda^2} - \frac{t_e}{\lambda}) + \frac{ke^{-\lambda t_e}}{\lambda}(L + \frac{1}{\lambda} + t_e) - k'L < 0
\]
It may be obtained by transforming Formula (8) that:

\[ \frac{k}{k'} < \frac{\lambda^3L}{\lambda^3L - 1 - \lambda t_s + e^{-\lambda t_s} (1 + \lambda L + \lambda t_s)} \]

That is, when the foregoing formula is satisfied, the data write mode of the data write control apparatus 10 is switched to the write-through mode.

After the write-through mode is entered, the quantity of dirty blocks no longer increases. However, because new data is written, data in original dirty blocks are replaced and written to the second memory 12. In this way, the quantity of dirty blocks decreases. When the quantity of dirty blocks decreases to the second preset value, the processor 13 switches the data write mode of the data write control apparatus 10 to the write-through mode.

Program execution performance in write-back mode is relatively high. Therefore, the second preset threshold preferably equals the first preset threshold minus 1. In this way, the data write control apparatus 10 may quickly enter the write-back mode. Certainly, in another embodiment, different second preset thresholds may be set according to a specific situation.

Second Embodiment

The second embodiment provides a data write method applied in the data write apparatus provided in the first embodiment. As shown in FIG. 3, FIG. 3 is a flowchart of the data write method.

Step S301: When the write control apparatus is in write-back mode, the processor detects a quantity of dirty blocks in the first memory.

Step S302: When the quantity of dirty blocks reaches a first preset threshold, separately predict execution progress of a program run by the processor within a danger time period in two write modes.

Step S303: When it is predicted that the execution progress of the program run by the processor within the danger time period in write-through mode is faster than the execution progress of the program run by the processor within the danger time period in write-back mode, switch the current data write mode to the write-through mode.

Step S304: When the write control apparatus is in write-through mode, detect the quantity of dirty blocks; and when the quantity of dirty blocks reaches a second preset threshold, switch the current data write mode to the write-back mode.

In this embodiment, the level 1 memory further includes the nonvolatile storage unit. After the data write control apparatus encounters a power failure, data in the volatile storage unit is backed up to the nonvolatile storage unit, and the first preset threshold is a maximum quantity of dirty blocks that can be backed up by the first memory.

In this embodiment, a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-back mode is used is:

\[ E(G - R) = k(L - \frac{1}{\lambda} - t_s) + ke^{-\lambda t_s} (L + \frac{1}{\lambda} - t_s) \]

where \( k \) is the execution progress of the program run by the processor within a unit time in write-back mode; \( L \) is a length of the preset danger time period; if a time when the quantity of dirty blocks reaches the first preset threshold is used as a zero time, \( t_s \) is a time when the data write control apparatus encounters a power failure within the danger time period; and \( 1/\lambda \) is an average power supply time of the data write control apparatus that is pre-obtained by means of statistics collection.

A calculation formula for predicting the execution progress of the program of the write control apparatus when the write-through mode is used is:

\[ E(G') = k'L \]

where \( k' \) is the execution progress of the program run by the processor within a unit time in write-through mode.

In this embodiment, the second preset threshold equals the first preset threshold minus 1.

A person of ordinary skill in the art may understand that all or a part of the steps of the methods in the embodiments may be implemented by a program instructing relevant hardware. The program may be stored in a computer readable storage medium. The storage medium may include: a ROM, a RAM, a magnetic disk, or an optical disc.
The data write apparatus and method provided in the embodiments of the present invention are described in
detail above. In this specification, specific examples are used to describe the principle and implementation manners of
the present invention, and the description of the embodiments is only intended to help understand the method and core
idea of the present invention. In addition, a person of ordinary skill in the art may, based on the idea of the present
invention, make modifications with respect to the specific implementation manners and the application scope. Therefore,
the content of this specification shall not be construed as a limitation to the present invention.

Claims

1. A data write control apparatus, comprising a level 1 memory, a level 2 memory, and a processor, wherein the level
1 memory comprises a volatile storage unit, the level 2 memory is a nonvolatile storage unit, and a data write mode
of the data write control apparatus comprises a write-back mode and a write-through mode; and in the write-back
mode, the processor writes received data to the level 1 memory, and in the write-through mode, the processor writes
received data to the level 1 memory and the level 2 memory;
when the write control apparatus is in write-back mode, the processor detects a quantity of dirty blocks in the first
memory; when the quantity of dirty blocks reaches a first preset threshold, separately predicts execution progress
of a program run by the processor within a danger time period in the two write modes; and when it is predicted that
the execution progress of the program run by the processor within the danger time period in the write-through mode
is faster than the execution progress of the program run by the processor within the danger time period in the write-
back mode, switches a current data write mode to the write-through mode; and
when the write control apparatus is in write-through mode, the processor detects the quantity of dirty blocks; and
when the quantity of dirty blocks decreases to a second preset threshold, switches the current data write mode to
the write-back mode.

2. The data write control apparatus according to claim 1, wherein the level 1 memory further comprises a nonvolatile
storage unit; after the data write control apparatus encounters a power failure, data in the volatile storage unit is
backed up to the nonvolatile storage unit; and the first preset threshold is a maximum quantity of dirty blocks that
can be backed up by the first memory.

3. The data write control apparatus according to claim 1, wherein a calculation formula for predicting the execution
progress of the program of the write control apparatus when the write-back mode is used is:

\[
E(G-R) = k(L - \frac{1}{\lambda} - t_s) + ke^{-\lambda L}(L + \frac{1}{\lambda} - t_s)
\]

wherein \(k\) is the execution progress of the program run by the processor within a unit time in write-back mode; \(L\)
is a length of the preset danger time period; if a time when the quantity of dirty blocks reaches the first preset threshold
is used as a zero time, \(t_s\) is a time of latest power supply before the zero time, and \(1/\lambda\) is an average power supply
time of the data write control apparatus that is pre-obtained by means of statistics collection; and
a calculation formula for predicting the execution progress of the program of the write control apparatus when the
write-through mode is used is:

\[
E(G')=k'L
\]

wherein \(k'\) is the execution progress of the program run by the processor within a unit time in write-through mode.

4. The data write control apparatus according to claim 1, wherein the second preset threshold equals the first preset
threshold minus 1.

5. A data write control method applied in the data write control apparatus, wherein the data write control apparatus
comprises a level 1 memory, a level 2 memory, and a processor, the level 1 memory comprises a volatile storage
unit, and the level 2 memory is a nonvolatile storage unit, and a data write mode of the data write control apparatus
comprises a write-back mode and a write-through mode; and in write-back mode, the processor writes received
data to the level 1 memory, and in write-through mode, the processor writes received data to the level 1 memory
and the level 2 memory; and the method comprises:

when the write control apparatus is in write-back mode, detecting, by the processor, a quantity of dirty blocks in the first memory;

when the quantity of dirty blocks reaches a first preset threshold, separately predicting execution progress of a program run by the processor within a danger time period in the two write modes;

when it is predicted that the execution progress of the program run by the processor within the danger time period in write-through mode is faster than the execution progress of the program run by the processor within the danger time period in write-back mode, switching a current data write mode to the write-through mode; and

when the write control apparatus is in write-through mode, detecting the quantity of dirty blocks; and when the quantity of dirty blocks decreases to a second preset threshold, switching the current data write mode to the write-back mode.

6. The data write control method according to claim 5, wherein the level 1 memory further comprises a nonvolatile storage unit; after the data write control apparatus encounters a power failure, data in the volatile storage unit is backed up to the nonvolatile storage unit; and the first preset threshold is a maximum quantity of dirty blocks that can be backed up by the first memory.

7. The data write control method according to claim 5, wherein a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-back mode is used is:

\[ E(G-R) = k(L - \frac{1}{\lambda} - t_s) + ke^{-\lambda t_s}(L + \frac{1}{\lambda} - t_s) \]

wherein \( k \) is the execution progress of the program run by the processor within a unit time in write-back mode; \( L \) is a length of the preset danger time period; if a time when the quantity of dirty blocks reaches the first preset threshold is used as a zero time, \( t_s \) is a time when power is supplied before the data write control apparatus encounters a power failure within the danger time period; and \( 1/\lambda \) is an average power supply time of the data write control apparatus that is pre-obtained by means of statistics collection; and

a calculation formula for predicting the execution progress of the program of the write control apparatus when the write-through mode is used is:

\[ E(G') = k'L \]

wherein \( k' \) is the execution progress of the program run by the processor within a unit time in write-through mode.

8. The data write control method according to claim 5, wherein the second preset threshold equals the first preset threshold minus 1.
**FIG. 1**

- **Level 1 memory**
  - **Volatile storage unit**
  - **Nonvolatile storage unit**
  - **Backup power source**

- **Processor**

- **Level 2 memory**

Connectors and arrows indicate data flow and connections between components.
FIG. 2
When a write control apparatus is in write-back mode, a processor detects a quantity of dirty blocks in a first memory

When the quantity of dirty blocks reaches a first preset threshold, separately predict execution progress of a program run by the processor within a danger time period in two write modes

When it is predicted that the execution progress of the program run by the processor within the danger time period in write-through mode is faster than the execution progress of the program run by the processor within the danger time period in write-back mode, switch a current data write mode to the write-through mode

When the write control apparatus is in write-through mode, detect the quantity of dirty blocks, and when the quantity of dirty blocks reaches a second preset threshold, switch the current data write mode to the write-back mode

FIG. 3
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

G06F 3/06 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPDOC, CNPAT, CNKI, IEEE, GOOGLE, WANFANG; data, read, write, SRAM, NV-SRAM, NVRAM, nonvolatile, write-back, write-through, mode, state, switch+, PCM, dirty, block, time, dead-block, threshold?, direct writing, transition, LI Hehe, LIU Yongpan, time, schedule, changing-over

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
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<td>A</td>
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