A switching circuit (100) includes first and second MOS transistors (M1, M2) of the same conductive type. The second MOS transistor (M2) has a drain connected to a first terminal (T1), a source connected to a load connecting terminal (Tout), a gate connected to a gate of the first MOS transistor (M1), and a back gate connected to a source of the first MOS transistor (M1). The switching circuit (100) includes a potential control circuit (Vc) that controls a current flowing between the source of the first MOS transistor (M1) and a resistor connecting terminal (TR) so that the potential of the source of the first MOS transistor (M1) and the potential of the source of the second MOS transistor (M2) are equal. This switching circuit (100) further includes a switching control circuit (CON) that outputs a control signal (Sg) to the gate of the first MOS transistor (M1) and the gate of the second MOS transistor (M2) and controls the operations of the first MOS transistor (M1) and the second MOS transistor (M2).
Description

FIELD

[0001] Embodiments described herein relate to a switching circuit and a power supply device.

BACKGROUND

[0002] In conventional switching circuits, the potential of a back gate of a power MOSFET is set to the potential of a source. For this reason, the back gate and the source of the power MOSFET is short-circuited. In other words, a parasitic diode between the back gate and the source of the power MOSFET is short-circuited. Therefore, if a power supply is reversely connected, a large current can flow to a load via the parasitic diode between the back gate and a drain of the power MOSFET.

DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a circuit diagram of a power supply device according to a first embodiment.
   FIG. 2 is a circuit diagram showing a second MOS transistor shown in FIG. 1.
   FIG. 3 is a cross-section of the second MOS transistor shown in FIG. 2.
   FIG. 4 is a circuit diagram of a power supply device according to a second embodiment.
   FIG. 5 is a cross-section of a MOS transistor shown in FIG. 4.

DETAILED DESCRIPTION

[0004] Embodiments disclosed herein provide a switching circuit, which can suppress a current flowing in an output MOS transistor when a power supply is reversely connected, and a power supply device.

[0005] The switching circuit according to an embodiment is provided with first and second MOS transistors of the same conductive type. The second MOS transistor has a drain connected to a first terminal, a source connected to a load connecting terminal, a gate connected to a gate of the first MOS transistor, and a back gate connected to the source. This switching circuit includes a potential control circuit that controls a current flowing between the source of the first MOS transistor and a resistor connecting terminal so that the potential of the source of the first MOS transistor and the potential of the source of the second MOS transistor are equal. This switching circuit further includes a switching control circuit that outputs a control signal to the gate of the first MOS transistor and the gate of the second MOS transistor and turns off the first MOS transistor and the second MOS transistor if the power supply is reversely connected.

[0006] FIG. 1 is a circuit diagram of a power supply device 1000 according to a first embodiment.

[0007] As shown in FIG. 1, the power supply device 1000 is provided with a switching circuit 100 and a resistor R.

[0008] The resistor R is connected between a resistor connecting terminal TR and a second potential line L2.

[0009] The switching circuit 100 supplies a voltage from a connected power supply to a load 101.

[0010] This switching circuit 100, as shown in FIG. 1, is provided with a first terminal (power supply terminal) T1, a second terminal (ground terminal) T2, a load connecting terminal Tout, a resistor connecting terminal TR, a signal input terminal Tin, first MOSFET (nMOS transistor) M1, a second MOS transistor (nMOS transistor) M2 as an output MOS transistor, potential control circuit VC, and a switching control circuit CON.

[0011] The first terminal (power supply terminal) T1 is connected to the first potential line L1.

[0012] The second terminal (ground terminal) T2 is connected to the second potential line L2.

[0013] A load 101 may be connected between the load connecting terminal Tout and the second potential line L2.

[0014] The resistor R is connected between the resistor connecting terminal TR and the second potential line L2.

[0015] An instruction signal Sc is input to the device at the signal input terminal Tin. Instruction signal Sc may be provided by external circuitry not shown in FIG. 1.

[0016] In the first MOS transistor M1, the drain is connected to the first terminal T1, and the source and back gate are electrically connected.

[0017] The second MOS transistor M2 is a MOS transistor of the same conductive type as that of the first MOS transistor M1. In the second MOS transistor M2, the drain is connected to the first terminal T1, the source is connected to the load connecting terminal Tout, the gate is connected to the gate of the first MOS transistor M1, and the back gate is connected to the source of the first MOS transistor M1.

[0018] Here, the size of the second MOS transistor M2 (i.e., the number of cells in the second MOS transistor M2) is set so that it is greater than the size of the first MOS transistor M1 (i.e., the number of cells in the first MOS transistor M1).

[0019] In addition, the potential control circuit VC controls a current flowing between the source of the first MOS transistor M1 and the resistor connecting terminal TR so that the potential of the source of the first MOS transistor M1 and the potential of the source of the second MOS transistor M2 are equal.

[0020] This potential control circuit VC, for example, has a bipolar transistor (PNP type bipolar transistor) Tr and an amplifier A as shown in FIG. 1.

[0021] The bipolar transistor Tr is connected between
the source of the first MOS transistor M1 and the resistor connecting terminal TR.

[0022] The amplifier A compares the potential at the source of the first MOS transistor M1 with the potential at the source of the second MOS transistor M2 and outputs a signal to the base of the bipolar transistor Tr. The output signal corresponds to the comparison result and serves to control a current flowing in the bipolar transistor Tr.

[0023] The instruction signal Sc, which is provided by external circuitry, is inputted into the switching control circuit CON via the signal input terminal Tin.

[0024] In addition, the switching control circuit CON is connected between the first terminal T1 and the second terminal T2 to be able to detect the potential of the first terminal T1 and the potential of the second terminal T2.

[0025] Moreover, the switching control circuit CON outputs a control signal Sg in response to the instruction signal Sc at the signal input terminal Tin or the detected difference in voltages at the first terminal T1 and the second terminal T2.

[0026] In other words, the switching control circuit CON outputs the control signal Sg to the gate of the first MOS transistor M1 and the gate of the second MOS transistor M2, thereby controlling the operations of the first MOS transistor M1 and the second MOS transistor M2.

[0027] Here, in case a power supply is normally connected, in this embodiment (also similarly in the following embodiments), it is assumed that the power supply is connected to the first potential line L1 and the ground is connected to the second potential line L2.

[0028] On the other hand, in case a power supply is reversely connected, in this embodiment (also similarly in the following embodiments), it is assumed that the ground is connected to the first potential line L1 and the power supply is connected to the second potential line L2. In this case, the potential of the second terminal T2 is higher than the potential of the first terminal T1.

[0029] For example, in case the power supply is reversely connected, the switching control circuit CON turns off the first MOS transistor M1 and the second MOS transistor M2 by the control signal Sg.

[0030] In other words, if the potential of the second terminal T2 is higher than the potential of the first terminal T1, the switching control circuit CON turns off the first MOS transistor M1 and the second MOS transistor M2 by the control signal Sg.

[0031] Here, FIG. 2 is a circuit diagram showing the second MOS transistor M2 shown in FIG. 1. In addition, FIG. 3 is a cross-section of the second MOS transistor M2 shown in FIG. 2.

[0032] As shown in FIG. 3, the second MOS transistor M2 has semiconductor substrate 1, first conductive type (n+ type) first semiconductor layer 2 with a high impurity concentration, first conductive type (n-type) second semiconductor layer 3 with a low impurity concentration, second conductive type (p type) third semiconductor layer 4, first gate insulating film 6ag, first gate electrode 7a, second gate insulating film 6bg, second gate electrode 7b, first conductive type (n+ type) first diffusion layer 8a with a high impurity concentration, first conductive type (n+ type) second diffusion layer 8b with a high impurity concentration, source electrode 9, second insulating layer 10a, third insulating layer 10b, and interlayer dielectric film 11.

[0033] The semiconductor substrate 1, for example, is composed of a semiconductor material such as silicon.

[0034] The first semiconductor layer 2 is formed on the semiconductor substrate 1. This first semiconductor layer 2 functions as the drain D (FIG. 2) of the second MOS transistor M2.

[0035] The second semiconductor layer 3 is formed on the first semiconductor layer 2.

[0036] The third semiconductor layer 4 is formed on the second semiconductor layer 3. This third semiconductor layer 4 functions as the back gate (FIG. 2) of the second MOS transistor M2.

[0037] The first gate insulating film 6ag is formed on the inner surface of a first trench 6a which extends from the upper surface of the third semiconductor layer 4 to the upper surface of the second semiconductor layer 3.

[0038] The first gate electrode 7a is formed in the first trench 6a which has the first gate insulating film 6ag also formed therein. This first gate electrode 7a functions as the gate of the second MOS transistor M2 (FIG. 2).

[0039] The second gate insulating film 6bg is formed on the inner surface of a second trench 6b which extends from the upper surface of the third semiconductor layer 4 to the upper surface of the second semiconductor layer 3.

[0040] The second gate electrode 7b is formed in the second trench 6b which has the second gate insulating film 6bg also formed therein. This second gate electrode 7b functions as the gate of the second MOS transistor M2 (FIG. 2).

[0041] The first diffusion layer 8a is formed on the upper surface of the third semiconductor layer 4 and laid out so that it and the first gate electrode 7a each make contact with opposing sides of the first gate insulating film 6ag.

[0042] The second diffusion layer 8b is formed on the upper surface of the third semiconductor layer 4 and laid out so that it and the second gate electrode 7b each make contact with opposing sides of the second gate insulating film 6bg.

[0043] The first insulating layer 5 is formed in a third trench 5a formed on the upper surface of the third semiconductor layer 4 and applies insulation between the first diffusion layer 8a and the second diffusion layer 8b.

[0044] The source electrode 9 is formed on the first diffusion layer 8a, first insulating film 5, and second diffusion layer 8b. The source electrode 9 functions as the source of the second MOS transistor M2 (FIG. 2).

[0045] The second insulating film 10a covers the aperture (at which the upper surface of the first gate electrode 7a is disposed) of the first trench 6a.
The third insulating film 10b covers an aperture (at which the upper surface of the second gate electrode 7b is disposed) of the second trench 6b.

The interlayer dielectric film 11 is formed on the source electrode 9, second insulating layer 10a, and third insulating layer 10b.

Here, parasitic diodes DP1 (FIG. 2) are formed by the first conductive type second semiconductor layer 3 and the second conductive type third semiconductor layer 4.

In addition, parasitic diodes DP2 (FIG. 2) are formed by the first conductive type first and second diffusion layers 8a and 8b and the second conductive type third semiconductor layer 4.

Here, the operational characteristics of the switching circuit 100 of this embodiment with the above described configuration will be explained.

For example, when a power supply is normally connected, the switching control circuit CON outputs the control signal Sg to the gate of the first MOS transistor M1 and the gate of the second MOS transistor M2 in response to the instruction signal Sc inputted, by external circuitry, at the signal input terminal Tin. In this way, the switching control circuit CON controls the operations of the first MOS transistor M1 and the second MOS transistor M2.

In other words, in a normal operation, the switching circuit 100 can set the potential of the power source, the potential of the sense source, and the potential of the back gate to the same potential, thus being able to realize operations similar to those of a general high side IPD (Intelligent Power Device).

On the other hand, in case the power supply is reversely connected, turns off the first MOS transistor M1 and the second MOS transistor M2 by the control signal Sg.

In other words, if the potential at the second terminal T2 is higher than the potential at the first terminal T1, the switching control circuit CON turns off the first MOS transistor M1 and the second MOS transistor M2 by the control signal Sg.

At that time, when the power supply is reversely connected, the parasitic diode DP2 between the back gate and the source of the second MOS transistor M2 prevents a backward current from flowing to the second MOS transistor M2.

As mentioned above, according to the switching circuit of this embodiment, in case the power supply is reversely connected, a current flow to the output MOS transistor M2 can be suppressed.

(Embodiment 2)

In this second embodiment, there will be an explanation of an example configuration in which the parasitic diode DP2 for suppressing a backward current from flowing to the second MOS transistor M2 is protected. This protection improves the withstand voltage when a power supply is reversely connected, as will be explained.

Here, FIG. 4 is a circuit diagram of a power supply device 2000 according to the second embodiment. In addition, in FIG. 4, the same symbols as the symbols of FIG. 1 are used to show components similar to those of the first embodiment.

As shown in FIG. 4, the power supply device 2000 is provided with a switching circuit 200 and a resistor R similar to corresponding components of power supply device 1000 of the first embodiment.

The switching circuit 200 is further provided with a diode (Zener diode) DX, which is not found in the switching circuit 100 of the first embodiment.

In this diode DX, an anode is connected to the back gate of the second MOS transistor M2, and a cathode is connected to the source of the second MOS transistor M2.

The breakdown voltage of the diode DX is set so that it is lower than the breakdown voltage of the parasitic diode DP2. Therefore, the withstand voltage is improved, thus enabling suppression of the breakdown of the parasitic diode DP2 at a time of reverse connection.

Also, the diode DX may alternatively be externally attached to the outside of the switching circuit 200.

FIG. 5 is a cross-section of the second MOS transistor M2 shown in FIG. 4. In addition, in FIG. 5, the same symbols as the symbols of FIG. 3 are used to show components similar to those of the first embodiment.

As shown in FIG. 5, the second MOS transistor M2 has a contact wiring 201, which is not found in the first embodiment.

This contact wiring 201 is formed in a fourth trench 201a extending from the upper surface of the first insulating layer 5 to the upper surface of the third semiconductor layer 4. The lower end of the contact wiring 201 is electrically connected to the third semiconductor layer 4.

In addition, in the diode DX shown in FIG. 4, an anode is electrically connected to the upper surface of the contact wiring 201, and a cathode is electrically connected to the source electrode 9.

With this configuration, the switching circuit 200 improves the withstand voltage by the diode DX, thus being enabling suppression of the breakdown of the parasitic diode DP2 at a time of reverse connection.

Here, other constitutions and functions of the switching circuit 200 are similar to those of the switching circuit 100 of the first embodiment.

In other words, according to the switching circuit of this embodiment, similar to the first embodiment, a current flowing to the output MOS transistor M2 can be suppressed when the power supply is reversely connected.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the
The scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

Claims

1. A switching circuit comprising:
   a first MOS transistor having a gate, a drain connected to a first terminal and a source connected to a back gate;
   a second MOS transistor having a drain connected to the first terminal, a source connected to a second terminal, a gate connected to the gate of the first MOS transistor, and a back gate connected to the source of the first MOS transistor; and
   a potential control circuit configured to control a current flowing between the source of the first MOS transistor and a third terminal to be connected to a resistor, so that a potential of the source of the first MOS transistor and a potential of the source of the second MOS transistor are substantially equal.

2. The switching circuit according to claim 1, wherein the second MOS transistor is configured to prevent a current from flowing from the second terminal to the first terminal.

3. The switching circuit according to claim 2, wherein the second MOS transistor includes a parasitic diode configured to prevent the current from flowing from the second terminal to the first terminal.

4. The switching circuit according to claim 3, further comprising a diode having an anode connected to the back gate of the second MOS transistor, and a cathode connected to the source of the second MOS transistor.

5. The switching circuit according to one of claims 1 to 4, wherein the first MOS transistor and the second MOS transistor are nMOS transistors.

6. The switching circuit according to one of claims 1 to 5, further comprising a switching control circuit configured to be turn off the first MOS transistor and the second MOS transistor by a control signal when a potential at a fourth terminal connected to ground is higher than a potential at the first terminal.

7. The switching circuit according to one of claims 1 to 6, wherein the potential control circuit comprises:
   a bipolar transistor connected between the source of the first MOS transistor and third terminal; and
   an amplifier configured to compare a potential of the source of the first MOS transistor with a potential of the source of the second MOS transistor and output a signal to a base of the bipolar transistor according to the comparison result to control a current flowing in the bipolar transistor.

8. The switching circuit according to one of claims 1 to 7, wherein the second MOS transistor comprises:
   a first semiconductor layer of a first conductive type with a first impurity concentration formed on a semiconductor substrate;
   a second semiconductor layer of the first conductive type with a second impurity concentration lower than the first impurity concentration formed on the first semiconductor layer;
   a third semiconductor layer of a second conductive type formed on the second semiconductor layer;
   a first gate insulating film formed on an inner surface of a first trench extending from an upper surface of the third semiconductor layer to an upper surface of the second semiconductor layer;
   a first gate electrode formed in the first trench; a second gate insulating film formed on an inner surface of a second trench extending from the upper surface of the third semiconductor layer to the upper surface of the second semiconductor layer;
   a second gate electrode formed in the second trench; a first diffusion layer of the first conductive type formed on the upper surface of the third semiconductor layer and being adjacent to the first gate electrode via the first gate insulating film; a second diffusion layer of the first conductive type formed on the upper surface of the third semiconductor layer and being adjacent to the second gate electrode via the second gate insulating film; a first insulating film disposed in a third trench formed through the upper surface of the third semiconductor layer; and a source electrode formed on the first diffusion layer and the second diffusion layer.

9. The switching circuit according to claim 8, wherein the second MOS transistor further comprises:
a contact wiring formed in a fourth trench, extending from an upper surface of the first insulating layer to the upper surface of the third semiconductor layer, and a lower surface of the contact wiring being connected to the third semiconductor layer.

10. The switching circuit according to claim 9, further comprising: a diode having an anode and a cathode, the anode electrically being connected to an upper surface of the contact wiring and the cathode electrically being connected to the source electrode.

11. A device, comprising:

   a power supply; and

   a switching circuit having a first terminal connected to the power supply, a second terminal connected to the load, and a third terminal connected to a resistor connected to ground, wherein the switching circuit comprises:

   a first MOS transistor having a gate, a drain connected to the first terminal and a source connected to a back gate,
   a second MOS transistor having a drain connected to the first terminal, a source connected to the second terminal, a gate connected to the gate of the first MOS transistor, and a back gate connected to the source of the first MOS transistor, and
   a potential control circuit configured to control a current flowing between the source of the first MOS transistor and the third terminal so that a potential of the source of the first MOS transistor and a potential of the source of the second MOS transistor are substantially equal.

12. The device of claim 11, wherein the switching circuit further comprises a switching control circuit configured to output a control signal to the gate of the first MOS transistor and the gate of the second MOS transistor, and to turn off the first MOS transistor and the second MOS transistor when the power supply is reversely connected.

13. The device of claim 12, wherein the first MOS transistor and the second MOS transistor are of the same conductive type.

14. The device of claim 13, wherein the second MOS transistor is larger in size than the first MOS transistor.

15. The device of one of claims 11 to 14, wherein the second MOS transistor is configured to prevent a current from flowing from the second terminal to the first terminal.
Fig. 2