Fabrication of single or multiple gate field plates

A process for fabricating single or multiple gate field plates, in particular for group-III nitride-based HEMTs, using consecutive steps of dielectric material deposition/growth, dielectric material etch and metal evaporation on the surface of a field effect transistor. This fabrication process permits a tight control on the field plate operation since dielectric material deposition/growth is typically a well controllable process. Moreover, the dielectric material deposited on the device surface does not need to be removed from the device intrinsic regions: this essentially enables the realization of field-plated devices without the need of low-damage dielectric material dry/wet etches. Using multiple gate field plates also reduces gate resistance by multiple connections, thus improving performances of large periphery and/or sub-micron gate devices.
Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. §119(e) of the following co-pending and commonly-assigned United States Provisional Patent Application:

Serial No. 60/501,557, entitled "FABRICATION OF SINGLE OR MULTIPLE GATE FIELD PLATES," filed on September 9, 2003, by Alessandro Chini, Umesh K. Mishra, Primit Parikh, and Yifeng Wu, attorneys docket number 30794.105-US-P1, which application is incorporated by reference herein.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

[0002] This invention was made with Government support under Grant No. N00014-01-1-0764 awarded by the ONR MURI program and Grant No. F49620-99-1-0296 awarded by the AFOSR MURI program. The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

[0003] This invention relates to semiconductor devices, and more particularly, to the fabrication of single or multiple gate field plates.

2. Description of the Related Art.

[0004] (Note: This application references to various publications as indicated in the specification by reference numbers enclosed in brackets, e.g., [x]. A list of these publications ordered according to these reference numbers can be found below in the section entitled "References." Each of these publications is incorporated by reference herein.)

[0005] In a semiconductor-based field effect transistor (FET), a large electric field arises during normal operation in the gate-drain access region. Field plating is a well-known technique for improving device performance under high electric field operation as well as alleviating surface traps phenomena [1], [2]. For example, field plating has been an effective and well-known technique in order to alleviate all the detrimental effects (breakdown voltages, trapping effects, reliability) that take place in devices operating at high electric field.

[0006] The basic concept of field plating relies on the vertical depletion of the device active region, thus enabling larger extensions of the horizontal depletion region. This results in a lower electric field in the device active region for a given bias voltage, alleviating all the detrimental effects (low breakdown, trapping phenomena, poor reliability) that take place whenever a device is operated at a high electric field. Moreover, a field plate positioned in the gate drain access region has also the capability of modulating the device active region, resulting in a decrease of surface traps effects that prevent proper device operation under large radio frequency (RF) signals.

[0007] What is needed, however, are improved methods of fabricating single or multiple gate field plates as well as improved structures incorporating single or multiple gate field plates.

SUMMARY OF THE INVENTION

[0008] Embodiments of the present invention provide improved methods of fabricating single and multiple gate field plates. A fabrication process according to the invention uses consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation on the surface of field effect transistors. The advantages of the fabrication process include tight control of the dielectric material thickness, and the absence of any exposure of the surface of the device active region to any dry or wet etch process that may induce damage in the semiconductor material forming the field effect transistor. Moreover, the dielectric material deposited on the device surface does not need to be removed from the device intrinsic regions, which enables the realization of field-plated devices without damage caused by the dry or wet etch processes. Using multiple gate field plates reduces gate resistance through the use of multiple connections, thus improving performances of large periphery and/or sub-micron gate devices. Finally, by properly adjusting the thickness of the dielectric material, parallel gate contacts can be deposited on top of the dielectric material, in order to significantly reduce gate resistance by electrically connecting the parallel gate contacts on device extrinsic regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1A is a cross-sectional and FIG. 1B is a top view of a field effect transistor (FET);
FIG. 2A is a device cross-section and FIG. 2B is a device top view illustrating dielectric material deposition/growth;
FIG. 3A is a device cross-section and FIG. 3B is a device top view illustrating dielectric material being removed from device extrinsic regions;
FIG. 4A is a device cross-section and FIG. 4B is a device top view illustrating evaporation of gate field plate;
FIG. 5A is a device cross-section and FIG. 5B is a device top view illustrating an example of multiple
In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Overview

The present invention describes a simple fabrication process for the realization of single or multiple gate field plate structures for field effect transistors (FETs). The present invention uses simple and typically well-controlled consecutive processing steps of dielectric material deposition or growth, dielectric material etch and metal evaporation.

Fabrication Process

FIGS. 1A, 1B, 2A, 2B, 3A, 3C, 4A, and 4B illustrate the steps of one possible realization of the fabrication process according an embodiment of the invention, wherein the fabrication process comprises a method of fabricating gate field plates.

FIG. 1A is a cross-sectional and FIG. 1B is a top view of a field effect transistor (FET) 10 that includes source and drain ohmic contacts 12 and 14, a gate contact 16 and an active region 18. The steps of the fabrication process are applied on the field effect transistor 10 or other device. The method generally comprises performing consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation to create one or more field plates on a surface of the device, wherein the steps permit a tight control on field plate operation and wherein the dielectric material deposited on the surface does not need to be removed from the active region 18, thereby enabling realization of a field-plated device without using a low-damage dielectric material dry or wet etch process. The performing step further comprises the steps of: (1) depositing or growing the dielectric material on the intrinsic and extrinsic regions of the device, wherein the dielectric material thickness is controlled in order to achieve proper operation of the device; (2) patterning the dielectric material by the dry or wet etch process or by a lift-off process, so that the dielectric material remains principally on an active region of the device; and (3) evaporating a field plate on the patterned dielectric material, wherein gate and field plate contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween. These steps are described in more detail below in conjunction with FIGS. 2A, 2B, 3A, 3B, 4A and 4B.

FIG. 2A is a device cross-section and FIG. 2B is a device top view illustrating the first step of the fabrication process, which comprises depositing or growing the dielectric material 20 on intrinsic and extrinsic regions of the device 10. The dielectric material 20 thickness is the critical parameter to be controlled in order to achieve proper operation of the finished device 10. However, this is usually a well controlled process in most deposition/growth techniques, e.g., PECVD (Plasma Enhanced Chemical Vapor Deposition). Typical materials are silicon nitrides and oxides, but others can be used, as long as they can be patterned by dry or wet etching or by lift-off.

FIG. 3A is a device cross-section and FIG. 3B is a device top view illustrating the second step of the fabrication process, which comprises patterning the dielectric material 20, by etch or removal from device extrinsic regions 22, so that the dielectric material 20 remains principally on an active region 18 of the device 10. In the case where the pattern is formed by etching, it should be stressed that the device 10 surface will be protected during this step, preventing any exposure of the surface of the active region 18 to any dry or wet etch process that may induce damage in the semiconductor material forming the device. After this step, ohmic contacts 12, 14 are electrically accessible, as well as the gate portion 16 that resides in the device extrinsic region 22.

FIG. 4A is a device cross-section and FIG. 4B is a device top view illustrating the third step of the fabrication process, which comprises creating a field plate 24 on the patterned dielectric material 20, wherein gate 16 and field plate 24 contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween. Preferably, metal evaporation is used to form the field plate 24, wherein the field plate 24 comprised of a metal stripe or contact. The field plate 24 is positioned in a gate 16 drain access region, thereby providing a capability of modulating the active region 18, resulting in a decrease of surface traps effect that prevent proper device operation under large RF signals. The field plate 24 is connected to both sides of the device intrinsic region, and the gate 16 and field plate 24 are electrically shorted at least at one side of the extrinsic region 22, providing a low resistance con-
nection between the two metal lines thereof. The offset and length of the field plate 24 are optimized with respect to the targeted device performance, i.e., breakdown voltage, RF performance, etc. [0017] If a multiple field plate structure is required, the three steps of dielectric material deposition/growth, dielectric material etch and metal evaporation described in FIGS. 2A, 2B, 3A, 3B, 4A and 4B can be repeated. [0018] FIG. 5A is a device cross-section and FIG. 5B is a device top view illustrating an example of creating multiple connections using multiple gate field plates in order to reduce gate resistance, thereby improving the performance of a large periphery device and/or sub-micron gate device. This example is a two field plate structure, which includes another layer of dielectric material 26 and another field plate 28 comprised of a metal stripe or contact. Dielectric material 26 thickness, field plate 28 length and offset with respect to the gate 16 and other field plates 24, and the number of field plates 24, 28 introduced, comprise fabrication process parameters. Using multiple field plates 24, 28 allows more freedom in device design, and has a significant impact in the realization of high voltage devices 10. [0019] Another advantage of the present invention is the possibility of alleviating the decrease in RF performance induced by gate resistance in a large periphery device. Typically, the frequency of maximum oscillation \( f_{\text{max}} \) decreases at the increasing of the gate finger width due to the increase in gate resistance. [0020] FIG. 6 is a graph of simulation of \( f_{\text{max}} \) dependence vs. gate finger width. As indicated in the graph, the introduction of a field plate structure shorted on both ends of the active region can improve \( f_{\text{max}} \) performances of devices with large finger width. Using a field plate with a resistance \( R_f \) equivalent to the gate resistance \( R_g \) and connected to both sides of the active region significantly improves \( f_{\text{max}} \) performance. Further improvement can be achieved by lowering field plate resistance. It should be stressed that this decrease will be observed only if the parasitic capacitances added by the field plate structure are negligible compared to those of the intrinsic device. This can be achieved by proper choice of dielectric material and its thickness, and has to be considered as an optimization process. [0021] Multiple connections between the gate and field plate also results in a significant decrease in the gate resistance. In order to achieve this multiple connection without severely degrading RF operation, a small portion of the active region is etched prior to gate deposition to create the multiple connections between the gate and the field plates without degrading the device’s RF operation. [0022] In this region, the gate and field plates can be connected without introducing any additional parasitic capacitance to the device. Again, device performance improves only if the introduced parasitic capacitance is small as compared to those of the intrinsic device. Furthermore, the spacing between individual active regions is used to engineer the thermal impedance of the device more effectively than a device with a conventional topology. [0023] Critical parameters are the choice of dielectric material, the thickness of the dielectric material, and the length of the field plates. These critical parameters have to be considered as optimization steps of the proposed fabrication process. [0024] Using this method allows the fabrication of large periphery devices with a reduced number of air bridges. Moreover, the fabrication of sub-micron devices can take advantage of the present invention. Typically, sub-micron gates are fabricated using a T-shape process, since the T-shape reduces gate resistance as compared to a standard gate shape. Low gate resistance can be achieved even with sub-micron gates by creating the multiple connections without a T-shape process. [0025] In addition, a parallel gate contact can be deposited on top of the dielectric material by properly adjusting the material dielectric thickness, in order to significantly reduce gate resistance by creating multiple connections using the parallel field plates on the device extrinsic regions. The low resistance path is provided by the parallel field plates, through a proper choice of the width at which the connection between the gate and field plates occurs. [0026] FIG. 7A is a device cross-section, FIG. 7B is a device top view and FIG. 7C is a device cross-section illustrating examples of multiple field plate structures for reduced gate resistance. Moreover, having a field plate covering the gate source access region, such as shown in FIGS. 7A, 7B and 7C, is also used for of modulating source access resistance for improving device linearity performance. Gallium Nitride-Based High Electron Mobility Transistor with Field Plates [0027] GaN based transistors including AlGaN/GaN High Electron Mobility Transistors (HEMTs) are capable of very high voltage and high power operation at RF, microwave and millimeter-wave frequencies. However, electron trapping and the ensuing difference between DC and RF characteristics has limited the performance of these devices. SiN passivation has been successfully employed to alleviate this trapping problem, resulting in high performance devices with power densities over 10 W/mm at 10 GHz. For example, [3] discloses methods and structures for reducing the trapping effect in GaN transistors. However, due to the high electric fields existing in these structures, charge trapping is still an issue. [0028] The present invention has been successfully utilized for improving the performance of AlGaN/GaN HEMT power devices. At 4 GHz operation, power densities of 12W/mm and 18.8W/mm have been achieved for devices on sapphire and silicon carbide substrate, respectively. Due to the simplicity of the processing step involved in the field plate fabrication, the present inven-
A GaN-based HEMT includes a channel layer and a barrier layer on the channel layer. Metal source and drain ohmic contacts are formed in contact with the barrier layer. A gate contact is formed on the barrier layer between the source and drain contacts and a spacer layer is formed above the barrier layer. The spacer layer may be formed before or after formation of the gate contact.

The spacer layer may comprise a dielectric layer, a layer of undoped or depleted Al_{x}Ga_{1-x}N (0<=x<=1) material, or a combination thereof. A conductive field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from the edge of the gate contact towards the drain contact. The field plate may be electrically connected to the gate contact. In some embodiments, the field plate is formed during the same deposition step as an extension of the gate contact. In other embodiments, the field plate and gate contact are formed during separate deposition steps. This arrangement may reduce the peak electric field in the device resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field may also yield other benefits such as reduced leakage currents and enhanced reliability.

An embodiment of the invention is illustrated in FIG. 8, which is a schematic cross-section of a unit cell 30 of a nitride-based HEMT device. Specifically, the device 30 includes a substrate 32, which may comprise silicon carbide, sapphire, spinel, ZnO, silicon or any other material capable of supporting growth of Group III-nitride materials. An Al_{x}Ga_{1-x}N (0<=x<=1) nucleation layer 34 is grown on the substrate 32 via an epitaxial crystal growth method, such as MOCVD (Metalorganic Chemical Vapor Deposition), HVPE (Hydride Vapor Phase Epitaxy) or MBE (Molecular Beam Epitaxy). The formation of nucleation layer 34 may depend on the material of substrate 32. For example, methods of forming nucleation layer 34 on various substrates are taught in [4] and [5]. Methods of forming nucleation layers on silicon carbide substrates are disclosed in [6], [7] and [8].

A high resistivity Group III-nitride channel layer 36 is grown on the nucleation layer 34. Channel layer 36 may comprise Al_{x}Ga_{1-x}N (0<=x<=1), 0<=y<=1, x+y<=1). Next, an Al_{x}Ga_{y}N (0<=x<=1) barrier layer 38 is formed on the channel layer 36. Each of the channel layer 36 and barrier layer 38 may comprise sub-layers that may comprise doped or undoped layers of Group III-nitride materials. Exemplary structures are illustrated in [3], [9], [10], [11] and [12]. Other nitride-based HEMT structures are illustrated in [13] and [14].
The effect of field plate distance (Lf) on device 

V and 4GHz.

cept that the field plate length Lf was varied from a dis-

tance of 0 to 0.9 μm. The PAE of the resulting devices 

was then measured. As illustrated in FIG. 10, the PAE 

showed improvement once the field plate length was ex-

tended to 0.5 μm, with an optimum length of about 0.7 μm. However, the optimum length may depend on the specific device design as well as operating voltage and frequency.

References

The following references are incorporated by reference herein:


ulting semiconductor devices."


Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

The following numbered paragraphs (paras.) contain statements of broad combinations of the inventive technical features herein disclosed:-

1. A method of fabricating one or more gate field plates, comprising:

performing consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation to create one or more field plates on a surface of a device, where the dielectric material deposited on the surface does not need to be removed from an active region, thereby enabling realization of a field-plated device without using a low-damage dry or wet etch process.

2. The method of para 1, wherein the steps permit a tight control on field plate operation.

3. The method of para 1, further comprising creating multiple connections using multiple gate field plates in order to reduce gate resistance.

4. The method of para 1, wherein the field plate is
positioned in a gate drain access region, thereby providing a capability of modulating the active region, resulting in a decrease of surface traps effect that prevent proper device operation under large radio frequency (RF) signals.

5. The method of para 1, further comprising preventing any exposure of the surface of the active region to the dry or wet etch process that may induce damage in the device.

6. The method of para 1, further comprising depositing a parallel gate contact on top of the dielectric material by properly adjusting the dielectric material thickness, in order to significantly reduce gate resistance by electrically connecting at least two parallel gates on extrinsic regions.

7. The method of para 1, wherein the device is a field effect transistor that includes source and drain ohmic contacts, a gate contact and an active region.

8. The method of para 1, wherein the performing step further comprises:

(1) depositing or growing the dielectric material on intrinsic and extrinsic regions of the device;
(2) patterning the dielectric material, so that the dielectric material remains principally on an active region of the device; and
(3) creating a field plate on the patterned dielectric material, wherein gate and field plate contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween.

9. The method of para 8, wherein the dielectric material thickness is controlled in order to achieve proper operation of the device.

10. The method of para 8, wherein the patterning step (3) comprises patterning the dielectric material by a dry or wet etch process or by a lift-off process.

11. The method of para 8, wherein the creating step (3) comprises evaporating a field plate on the patterned dielectric material.

12. The method of para 8, wherein steps (1)-(3) are repeated to create a plurality of the field plates.

13. The method of para 8, wherein the field plate has a resistance $R_f$ that is equivalent to a gate resistance $R_g$.

14. The method of para 8, wherein the field plate is connected to both sides of the device intrinsic region.

15. The method of para 8, further comprising creating multiple connections between the gate and the field plate to decrease gate resistance.

16. The method of para 15, wherein the creating step comprises etching a small portion of the active region prior to deposition of the gate to create multiple connections between the gate and the field plate.

17. The method of para 15, further comprising spacing between the active regions to engineer a thermal impedance of the device.

18. The method of para 15, wherein the device comprises a large periphery device with a reduced number of air bridges.

19. The method of para 15, wherein the creating step comprises the step of creating the multiple connections without a T-shape process in order to lower gate resistance.

20. The method of para 15, wherein the creating step comprises the step of creating the multiple connections using parallel field plates.

21. The method of para 20, wherein the creating step comprises the step of creating the field plate covering the gate source access region in order to modulate source access resistance for improving device linearity performance.


23. A method of fabricating gate field plates, comprising:

(a) depositing or growing the dielectric material on intrinsic and extrinsic regions of the device;
(b) patterning the dielectric material, so that the dielectric material remains principally on an active region of the device; and
(c) creating a field plate on the patterned dielectric material, wherein gate and field plate contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween.

24. The method of para 23, wherein the dielectric material thickness is controlled in order to achieve proper operation of the device.

25. The method of para 23, wherein the patterning step (b) comprises patterning the dielectric material by a dry or wet etch process or by a lift-off process.

26. The method of para 23, wherein the creating step (c) comprises evaporating a field plate on the pat-
terned dielectric material.

27. The method of para 23, wherein steps (a)-(b) are repeated to create a plurality of the field plates.

28. A high electron mobility transistor (HEMT), comprising:

a substrate;
a nucleation layer grown on the substrate;
a channel layer formed on the nucleation layer;
a barrier layer formed on the channel layer;
a semiconductor spacer layer grown on the barrier layer; and
source and drain electrodes formed making ohmic contacts through the barrier layer such that an electric current flows between the source and drain electrodes when a gate electrode is biased at an appropriate level;
wherein the spacer layer is etched and the gate electrode is deposited such that at least a portion of the gate electrode is on a surface of barrier layer, and
wherein a portion of the gate electrode is patterned to extend across the spacer layer so that the gate electrode forms a field plate extending a distance away from the gate electrode towards the drain electrode.

29. The HEMT of para 28, wherein the electric current flows between the source and drain electrodes via a two-dimensional electron gas (2DEG) induced at a heterointerface between the channel layer and barrier layer when the gate electrode is biased at the appropriate level.

30. The HEMT of para 28, wherein a portion of the gate electrode on the spacer layer forms an epitaxial field plate.

31. The HEMT of para 28, further comprising a dielectric passivation layer covering the spacer layer.

32. The HEMT of para 28, wherein the spacer layer comprises a dielectric layer, a layer of undoped or depleted AlxGa1-xN (0<=x<=1) material, or a combination thereof.

33. The HEMT of para 28, wherein the field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from the edge of the gate electrode towards the drain electrode.

34. The HEMT of para 28, wherein the field plate is electrically connected to the gate electrode.

35. The HEMT of para 28, wherein the field plate is formed during the same deposition step as an extension of the gate electrode.

36. The HEMT of para 28, wherein the field plate and gate electrode are formed during separate deposition steps.

37. The HEMT of para 28, wherein the substrate comprises silicon carbide, sapphire, spinel, zinc oxide, silicon or any other material capable of supporting growth of Group III-nitride materials.

38. The HEMT of para 28, wherein the nucleation layer is an AlxGa1-x,N (0<=x<=1) nucleation layer.

39. The HEMT of para 28, wherein the nucleation layer is an AlN layer.

40. The HEMT of para 28, wherein the channel layer is a high resistivity Group III-nitride channel layer.

41. The HEMT of para 28, wherein the channel layer comprises AlxGa1-xN (0<=x<=1, 0<=y<=1, x+y<=1).

42. The HEMT of para 28, wherein the channel layer comprises GaN:Fe.

43. The HEMT of para 28, wherein the barrier layer comprises AlxGa1-xN (0<=x<=1).

44. The HEMT of para 28, wherein the barrier layer comprises AlN and AlGaN.

45. The HEMT of para 28, wherein each of the channel layer and barrier layer comprise sub-layers that are doped or undoped layers of Group III-nitride materials.

46. The HEMT of para 28, wherein the spacer layer is a Group III-nitride semiconductor spacer layer is grown on an AlxGa1-x,N barrier layer.

47. The HEMT of para 28, wherein the spacer layer has a uniform composition.

48. The HEMT of para 28, wherein the spacer layer has a graded composition.

49. The HEMT of para 28, wherein the spacer layer is undoped.

50. The HEMT of para 28, wherein the spacer layer is fully depleted as grown.

51. The HEMT of para 28, wherein the gate electrode is formed after formation of the barrier layer and passivation layer is deposited on the device, wherein the field plate is then formed on the passivation layer.
overlapping the gate and extending a distance \( L_f \) in the gate-drain region, and the passivation layer serves as a spacer layer for the field plate.

**Claims**

1. A method of fabricating a high electron mobility transistor (HEMT), comprising:

   - forming a barrier layer on a channel layer;
   - forming metal source and drain ohmic contacts in contact with the barrier layer;
   - forming a spacer layer above the barrier layer;
   - etching the spacer layer to provide an opening for a gate contact;
   - depositing the gate contact in the opening such that the bottom of the gate contact is on the barrier layer;
   - forming a conductive field plate above the spacer layer that extends a distance \( L_f \) (field plate distance) from an edge of the gate contact towards the drain contact.

2. The method according to claim 1, wherein the conductive field plate is formed during a same deposition step as the gate contact as an extension of the gate contact.

3. The method according to claim 1, wherein the conductive field plate is formed during a different deposition step to the gate contact.

4. The method according to any one of the previous claims, wherein the channel layer comprises a high resistivity Group III-nitride.

5. The method according to claim 4, wherein the channel layer comprises \( \text{Al}_x\text{Ga}_y\text{In}_{1-x-y} \)N (0\( \leq x \leq 1 \), 0\( \leq y \leq 1 \), \( x+y \leq 1 \)).

6. The method according to any one of the previous claims, wherein the barrier layer comprises \( \text{Al}_x\text{Ga}_{1-x} \)N (0\( \leq x \leq 1 \)).

7. The method according to claim 6, wherein the spacer layer comprises a Group III-nitride semiconductor grown on the \( \text{Al}_x\text{Ga}_{1-x} \)N (0\( \leq x \leq 1 \)) barrier layer.

8. The method according to any one of the previous claims, wherein the method further comprises forming a dielectric passivation layer covering the conductive field plate and the spacer layer.

9. A high electron mobility transistor (HEMT), comprising:

   a barrier layer on a channel layer;

   metal source and drain ohmic contacts in contact with the barrier layer;

   a spacer layer above the barrier layer;

   an opening in the spacer layer for a gate contact;

   a gate contact in the opening, wherein the bottom of the gate contact is on the barrier layer;

   a conductive field plate above the spacer layer that extends a distance \( L_f \) (field plate distance) from an edge of the gate contact towards the drain contact.

10. The HEMT according to claim 9, wherein the conductive field plate is an extension of the gate contact.

11. The HEMT according to claim 9 or claim 10, wherein the channel layer comprises a high resistivity Group III-nitride.

12. The HEMT according to claim 11, wherein the channel layer comprises \( \text{Al}_x\text{Ga}_y\text{In}_{1-x-y} \)N (0\( \leq x \leq 1 \), 0\( \leq y \leq 1 \), \( x+y \leq 1 \)).

13. The HEMT according to any one of claims 9 to 12, wherein the barrier layer comprises \( \text{Al}_x\text{Ga}_{1-x} \)N (0\( \leq x \leq 1 \)).

14. The HEMT according to claim 13, wherein the spacer layer comprises a Group III-nitride semiconductor grown on the \( \text{Al}_x\text{Ga}_{1-x} \)N (0\( \leq x \leq 1 \)) barrier layer.

15. The HEMT according to any one of claims 9 to 14, wherein the HEMT further comprises a dielectric passivation layer covering the conductive field plate and the spacer layer.
### Documents Considered to Be Relevant

<table>
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<tr>
<th>Category</th>
<th>Citation of document with indication, where appropriate, of relevant passages</th>
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The present search report has been drawn up for all claims.

Place of search: Munich  
Date of completion of the search: 8 April 2013  
Examiner: Dauw, Xavier

**Category of Cited Documents**

- **X**: particularly relevant if taken alone  
- **Y**: particularly relevant if combined with another document of the same category  
- **A**: technological background  
- **O**: non-written disclosure  
- **P**: intermediate document

**Classification of the Application (IPC)**

- **INV.**: invention  
- **H01L**: electrical energy conversion or transport

**Technical Fields Searched (IPC)**

- **H01L**: electrical energy conversion or transport
ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO. EP 12 19 2425

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on 08-04-2013. The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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For more details about this annex: see Official Journal of the European Patent Office, No. 12/82.
REFERENCES CITED IN THE DESCRIPTION

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