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Method of manufacturing multilayer printed wiring board
Verfahren zur Herstellung einer mehrschichtigen gedruckten Leiterplatte
Procédé de fabrication d’une carte à circuit imprimé multicouche

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Description

Technical Field

[0001] The present invention relates to a process for producing a multi-layer printed wiring board, said process permitting mass production of a multi-layer printed wiring board with small-diameter via holes. Increased productivity is made possible, by driving the galvano head at a higher speed.

Background Art

[0002] A build-up multilayer wiring board alternately has interlayer resin insulators and conductive circuit layers, provides holes to the interlayer resin insulator layers, and then electrically connects the upper layers and lower layers by forming conductive films on the surface of the walls of these holes.

[0003] A hole (via hole) in the interlayer resin insulating layer is generally formed with the use of an exposure and developing process, which gives photosensitive property to the interlayer resin.

[0004] However, the required diameter of these via holes in a multilayer printed wiring board is almost 100 μm or less, thus it is necessary to develop technology which makes it possible to maintain this small diameter. Due to such stringent requirements, the employment of a processing method utilizing a laser beam for the boring of the holes in the build-up multilayer wiring board will now be investigated.

[0005] Technology using laser for boring is proposed, in JPA HEI 3-54884. According to this method, a light beam from a laser source is received by a processing head for deflection. Thereby, the laser beam is irradiated to a predetermined resin insulator to form a hole.

[0006] Document GB-A-2 307 352 discloses a process for producing a multi-layer printed wiring board, which comprises following steps (a) to (c):

(a) forming an interlayer insulating resin layer having a metal film and an opening formed in said metal film on a board covered with a conductor layer,
(b) removing that part of said interlayer insulating resin layer which is exposed through said opening in said metal film, by irradiation of a laser beam, thereby forming an opening through which a via hole is formed, and
(c) forming via holes and conductor circuits.


[0008] In mass production of multi-layer printed wiring boards, which have hundreds to thousands of via holes in each layer, efficient hole drilling is essential. In addition, via holes need accurate positioning for electrical connection to conductor circuits in the layers below.

[0009] Unfortunately, it has been difficult to control, with high accuracy, the position of laser irradiation for via hole drilling in mass production. This has aroused a need for a process for fabricating a multi-layer printed wiring board containing openings at accurate positions. However, the current method of manufacture can not guarantee accurate positioning of laser irradiation. Improvement in positioning accuracy is offset by a necessary decrease in head driving speed, which in turn lowers productivity.

[0010] The present invention aims to address the above-mentioned problems.

[0011] It is an object of the present invention to provide a process for producing a multi-layer printed wiring board, said process permitting accurate positioning of via holes independent of the accuracy of position for laser irradiation, thereby drilling a large number of holes efficiently by laser irradiation.

[0012] It is another object of the present invention to provide a method for increasing the driving speed of the scanning head without decreasing the accuracy of positions of via holes.

Disclosure of the Invention

[0013] In order to achieve the aforementioned objectives, the present invention according to claim 1, provides a process for producing a multi-layer printed wiring board, which comprises the following steps (a) to (c):

(a) forming an interlayer insulating resin layer having a metal film, an opening formed on the metal film and a register mark on the surface thereof on a board covered with a conductor layer,
(b) removing that part of the interlayer insulating resin layer which is exposed through the opening in said metal film, by irradiation of a laser beam aimed at the opening according to data obtained by sensing the position of the register mark, thereby forming an opening through which a via hole is formed, and
(c) forming via holes and conductor circuits.

[0014] According to the present invention, via holes are drilled in the resin insulating layer, through openings made in a metal film attached thereto, by laser irradiation directed approximately to said openings in response to the board position sensed by a camera relative to the register marks inscribed on the metal film. (This metal film functions as a resist mask for the laser beam, and it is referred to as conformal mask hereinafter.)

[0015] In this way it is possible to form via holes at adequate positions even though the accuracy of position for laser irradiation is not high, because the accuracy of the position of via holes depends solely on the accuracy of the board position.
of the position of the openings in the metal film (or conformal mask).

[0016] In this way it is also possible to make hundreds to thousands of via holes efficiently owing to the register marks inscribed in the metal film having openings for via holes. These register marks permit the position of the board to be determined accurately relative to the scanning head (galvano head) whose movement has already been programmed. The resulting data controls the positioning of the table and scanning head.

[0017] According to the present invention, it is possible to employ laser irradiation without sacrificing the accuracy of the position of via holes even though the board is not located very accurately. This implies that the scanning head can move faster, making more via holes per unit time, which leads to improved productivity.

[0018] In the present invention, the register marks on the multi-layer printed wiring board should ideally be inscribed on the metal film with the use of etching or the like. They may be circular, square, or rectangular in form.

[0019] Being opaque to light, the metallic register mark gives a silhouette when it is illuminated upward from the table or reflects light when it is illuminated downward. In other words, it can be recognized by the camera regardless of the direction from which it is illuminated.

[0020] The register marks should be inscribed at the same time as etching for openings on the metal film. This eliminates the necessity of performing two steps separately for making the openings and inscribing the register marks.

[0021] In another preferred embodiment, a sub-layer mark is formed on the surface of the board which is covered with an interlayer insulating resin layer and an opening (as the register mark) is formed in the metal film which functions as the conformal mask, as shown in Figs. 11 and 12. The position is determined by sensing the sub-layer mark which is visible in the opening (or the register mark) through the resin layer. The advantage of this embodiment is that the sub-layer mark 220B, which is covered with a resin layer, does not oxidize to decrease in reflectivity, nor does it peel off (and hence it poses no problem with recognition in silhouette).

[0022] To be more concrete, the process consists of steps of forming the interlayer insulating resin layer, forming on it the metal film (which functions as the conformal mask) by physical or chemical vapor deposition or electroless plating or by hot-pressing a resin film covered with a metal film, and forming the register mark at the same time as the opening is formed by etching.

[0023] The above-mentioned interlayer insulating resin layer may be formed from a thermosetting resin or a thermoplastic resin or a combination thereof.

[0024] It may also be formed from an adhesive for electroless plating. In its most desirable form, the adhesive is composed of an uncured heat-resistant resin slightly soluble in acid or oxidizing agent and particles (dispersed therein) of a cured heat-resistant resin soluble in acid or oxidizing agent that dissolves and removes the heat-resistant resin particles, thereby forming a rough surface with minute pits for anchorage.

[0025] The adhesive for electroless plating should preferably be one which contains the cured heat-resistant resin particles specified by any of the following, because it gives anchorage of a more complex structure.

1. Heat-resistant resin particles which have an average particle diameter smaller than 10 µm.

2. Agglomerate of heat-resistant resin powder having an average particle diameter smaller than 2 µm.

3. A mixture of heat-resistant resin powder having an average particle diameter of 2 - 10 µm and heat-resistant resin powder having an average particle diameter smaller than 2 µm.

4. Pseudo agglomerate of heat-resistant resin powder having an average particle diameter of 0.1 - 5 µm, each particle of which carries on its surface heat-resistant resin powder or inorganic powder or both having an average particle diameter smaller than 2µm.

5. A mixture of heat-resistant resin powder having an average particle diameter of 0.1 - 8 µm and heat-resistant resin powder having an average particle diameter larger than 0.8 µm and smaller than 2 µm.

6. Heat-resistant resin powder which has an average particle diameter of 0.1 - 10 µm.

[0026] For good adhesion, the rough surface should ideally have a roughness of Rmax = 0.01 - 20 µm. In the case of a semi-additive process, the preferred roughness is 0.1 - 5 µm, which ensures good adhesion while permitting the electrolessly plated film to be removed.

[0027] The above-mentioned heat-resistant resin slightly soluble in acid or oxidizing agent should preferably be a "composite of thermosetting resin and thermoplastic resin" or a "composite of photosensitive resin and thermoplastic resin". The former is superior in heat resistance and the latter can be applied by photolithography to form the opening for the via hole.

[0028] The above-mentioned thermosetting resin includes, for example, epoxy resin, phenol resin, and polyimide resin. These chemicals may be made photosensitive if their thermosetting groups are modified with methacrylic acid or acrylic acid. Acryl-modified epoxy resin is most suitable.

[0029] The epoxy resin includes, for example, epoxy resins of phenol novolak type or cresol novolak type and alicyclic epoxy resins formed by modification with dicyclopentadiene.

[0030] The thermoplastic resin includes, for example, polyethersulfone (PES), polysulfone (PSF), polyphen-
(PPS), polyphenylene sulfide (PPES), polyphenylene oxide (PPO), polyetherimide (PEI), and fluoro-zenesulfone (PPS), polyphenylene sulfide (PPES), polyphenylene ether (PPE), polyetherimide (PI), and fluoro-plastics.

[0031] The mixing ratio of the thermosetting (photosensitive) resin to the thermoplastic resin should ideally be from 5/5 to 50/50, so that the resulting compound has good toughness without a loss in heat resistance.

[0032] The amount of the heat-resistant resin particles should be 5 - 50 wt%, preferably 10 - 40 wt%, of solids in the heat-resistant resin matrix.

[0033] The heat-resistant resin particles should preferably be those of amino resin (such as melamine resin, urea resin, and guanamine resin) and epoxy resin.

[0034] Incidentally, the adhesive may be composed of two layers, each differing in composition as explained later.

[0035] Forming an interlayer insulating resin layer and a metal film simultaneously is acceptable. In this case, the board having conductor layers formed thereon is hot-pressed together with a prepreg placed thereon, said prepreg being a thermosetting resin, a thermoplastic resin, or a composite of thermosetting resin and thermoplastic resin, which is impregnated into a fibrous substrate.

[0036] The fibrous substrate may be glass cloth or aramid fiber cloth.

[0037] Another acceptable process consists of placing a metal-clad resin film on the board having conductor layers formed thereon, performing hot-pressing, thereby forming the interlayer insulating resin layer and the metal film, and etching the metal film, thereby forming the opening and register mark.

[0038] The resin film mentioned above may be of thermosetting resin, thermoplastic resin, or a composite of thermosetting resin and thermoplastic resin.

[0039] The thermosetting resin includes, for example, one or more of the following: epoxy resin, polyimide resin, phenolic resin, bismaleimide triazine resin (BT). The thermoplastic resin includes, for example, one or more of the following: polyether sulfone (PES), polyether amide (PEA), polyphenylene ether (PPE), polyphenylene sulfide (PPS), and fluoro-plastics. The thermoplastic resin should be used in the form of uncured resin film.

[0040] Hot-pressing may be performed at 100 - 150°C and 5 - 50 kg/cm² for thermosetting resins and 100 - 350°C and 5-100 kg/cm² for thermoplastic resins.

[0041] The resin film should ideally be 5 - 100 μm thick. Excessive thickness presents difficulties when hole drilling with a laser beam. Excessively thin films do not provide satisfactory interlayer insulation.

[0042] The metal film may be of one or more of the following metals; copper, nickel, aluminum, and precious metal (such as gold, silver, palladium, and platinum). Copper foil is the most desirable because of its low price and good resistance to laser beams.

[0043] The metal film should ideally be 1 - 20 μm thick. Excessive thickness does not yield fine patterns, and excessively thin films are easily damaged by laser beams.

[0044] In a preferred embodiment of the present invention, the metal film as the conformal mask is formed by physical or chemical vapor deposition. Through this mask, openings for via holes are formed with the use of a laser. On this metal film is formed a layer by electroless plating. On this layer is formed another layer by electrolytic plating. Incidentally, the electrolessly-plated layer should be given a plated resist prior to electrolytic plating. The electrolessly-plated layer under the plating resist is removed by etching when conductor circuits and via holes are formed. The plating resist protects the electrolytically plated layer used to form conductor circuits and via holes from damage by the etching process because the metal film and electrolessly plated layer are thin enough for easy removal. Thus it is possible to create wiring with a fine pitch and via holes with an extremely small diameter. Suitable etching solutions include aqueous solution of sulfuric acid and hydrogen peroxide, aqueous solution of ammonium persulfate, and aqueous solution of ferric chloride.

[0045] The physical or chemical vapor deposition may be accomplished by sputtering or vacuum deposition.

[0046] The deposited metal film and the electrolessly-plated film covering it should preferably be thinner than 2 μm. Such a thin film is easily removed by etching when conductor circuits and via holes are formed by removing unnecessary parts of the metal film and electrolessly plated layer. Therefore, the electrolytically plated layer used to form conductor circuits and via holes are not damaged by the etching process. Thus it is possible to create wiring with a fine pitch and via holes with an extremely small diameter.

[0047] In the present invention, it is permissible to form the metal film simultaneously with the interlayer insulating resin layer. This is achieved by laminating a prepreg and then performing hot pressing to cure the resin. The prepreg is a glass fiber cloth or aramid fiber cloth impregnated with resin in B stage. A resin film may replace it in B stage.)

[0048] In this case, the steps shown in Fig. 4(D) and Fig. 5(E) are replaced by the steps shown in Fig. 9(D') and Fig. 9(E').

Brief Description of the Figures

Fig. 1 is a schematic diagram showing the apparatus for producing a multi-layer printed wiring board according to the first embodiment of the present invention.

Fig. 2 is a block diagram showing the control system for the production unit shown in Fig. 1.

Fig. 3 is a flow diagram showing processing by the control system shown in Fig. 2.

Figs. 4(A) to 4(D) are diagrams showing the process
of producing a printed wiring board according to the first embodiment of the present invention.

Figs. 5(E) to 5(H) are diagrams showing the process of producing a printed wiring board according to the first embodiment of the present invention.

Figs. 6(I) to 6(L) are diagrams showing the process of producing a printed wiring board according to the first embodiment of the present invention.

Figs. 7(M) to 7(P) are diagrams showing the process of producing a printed wiring board according to the first embodiment of the present invention.

Fig. 8(A) is a plan view showing the board having an annular register mark formed thereon. Fig. 8(B) is a plan view showing the board having a square register mark formed thereon.

Figs. 9(D') and 9(E') are diagrams showing the process of producing a printed wiring board according to the first embodiment (with modification) of the present invention.

Figs. 10(A) to 10(E) are diagrams showing the process of producing a printed wiring board according to the first embodiment (with another modification) of the present invention.

Figs. 11(A) to 11(E) are diagrams showing the process of producing a printed wiring board according to the first embodiment (with another modification) of the present invention.

Figs. 12(F) to 12(H) are diagrams showing the process of producing a printed wiring board according to the first embodiment (with another modification) of the present invention.

Best Mode for Carrying out the Invention

[0050] The embodiments of the present invention will be described with reference to the drawings.

[0051] The first embodiment of the present invention employs an apparatus as shown in Fig. 1 for production of a multi-layer printed wiring board.

[0052] In this embodiment, a CO₂ laser emitter 60 generates a laser beam. The laser beam is reflected by a mirror 66 and transmitted to a galvano head 70 through a transfer mask 62 for sharp focusing on the board.

[0053] The galvano-head (scanning head) 70 is composed of a set of galvano-mirrors including: a galvano-mirror 74X for scanning the laser beam in an X direction and a galvano-mirror 74Y for scanning the laser beam in a Y direction. Control motors 72X, 72Y drive these mirrors 74X, 74Y. The motors 72X, 72Y adjust the angles of the mirrors 74X, 74Y depending on the control command from the computer (to be explained later), and also transmit the detection signal from the built-in encoder to the computer side.

[0054] The scan area of the galvano-mirror is 30 x 30mm. Moreover, the positioning velocity of the galvano-mirror is 400 points/sec within the scanning area. The laser beam is repeatedly scanned in X-Y directions through the galvano-mirrors 74X, 74Y and passes the f-θ lens 76 and collides with the aperture 30a of the metal layer of a substrate 20 (to be explained later) to form a via hole (aperture).

[0055] The substrate 20 is placed on the X-Y table 80 moving in X-Y directions. As explained above, since the scanning area of the galvano-mirror of each galvano-head 70 is 30mm x 30mm and the substrate 20 of 500mm x 500mm is used, the number of step areas of the X-Y table 80 is 289 (17 x 17). Namely, the processing of the substrate 20 can be completed by repeating the movement of 30mm in an X direction 17 times, and the movement in a Y direction 17 times, respectively.

[0056] The manufacturing apparatus explained above is also provided with a CCD camera 82, therefore the positions of the positioning marks 30b placed on each of the four corners of a substrate 20, are measured to start processing after compensating for errors.

[0058] Subsequently, the control mechanism of this manufacturing apparatus will be explained with reference to Fig. 2.

[0059] The control apparatus comprises of a computer 50 which processes and receives, hole coordinate data (processing data) of the multilayer printed wiring board, obtained from the input section 54, and the position of the positioning mark 30b measured by the CCD camera 82 to generate the processing data to be stored in the memory section 52. The actual boring process can be conducted by driving the X-Y table 80, laser 60, and the galvano-head 70, on the basis of the processing data.

[0060] Here, the processing data generating process by the computer 50 will be explained in further detail with reference to Fig. 3.

[0061] First the computer 50 drives the X-Y table 80 to align the CCD camera 82, with the positioning mark 30b (first process). Errors such as deviation in the X direction, deviation in the Y direction, the compression amount of the substrate and the amount of rotation are measured by calculating locations of the four positioning marks 30b with the CCD camera 82 (second process). Here, error data is generated for correcting any errors of measurement (third process).

[0062] Subsequently, the computer 50 corrects the hole coordinate data consisting of the coordinates of respective holes with the error data generated in the third process to generate the actual processing data consisting of the coordinates of the holes actually bored (fourth process). On the basis of the actual processing data, the galvano-head data for driving the galvano-head 70 is generated (fifth process), the table data for driving the X-
Y table is generated (sixth process), and the laser data for the timing of oscillating the laser 60 is also generated (seventh process). This data is temporarily stored in the memory section 52 as explained above and the actual boring process is conducted by driving the X-Y table 80, laser 60, and galvano-head 70 depending on this data. [0063] In the first embodiment, printed wiring bards are produced according to steps sequentially explained below with reference to Figs. 4 to 7.

(1) The base material is a copper-clad laminate 20a. See Fig. 4(A). It is a 1-mm thick board 20 of glass epoxy resin or BT resin (bismaleimide triazine), having both sides thereof laminated with 18-μm thick copper foil 22. The copper foil is patterned by etching using the standard method, to form a copper pattern 22A and a register mark 22B on each side of the board. In actuality, there are four register marks. See Fig. 4(B).

(2) After washing with water and drying, the board 20 undergoes acid degreasing and soft etching. It is then treated with a catalyst solution composed of palladium chloride and organic acid. The Pd-activated board 20 undergoes electroless plating, so that the copper pattern 22A is covered with a 2.5-μm thick layer of Ni-P-Cu alloy, which has a rough surface 23. See Fig. 4(C).

(3) The board 20 is hot-pressed between two 20-μm thick fluoroplastic sheets ("Teflon" from DuPont) under a pressure of 20 kg/cm² at 300°C for 30 minutes, so as to form the interlayer insulating resin layers 26. See Fig. 4(D).

(4) The Cu layer 30 is covered with a commercial photosensitive dry film 31, which is subsequently exposed to light (100 mJ/cm²) through a mask 31 placed thereon which has a black spot 31a (for a via hole) and a black spot 31b (for a register mark). See Fig. 5(F). Alignment of the mask 31 with the board 20 is achieved by aligning the mark 31b on the mask 31 with the register mark 22B on the board 20 by with the use of an X-ray camera (not shown).

(5) Etching with an aqueous solution of sulfuric acid and hydrogen peroxide is performed through the etching resist 32, so that the Cu layer 30 is partly removed at the opening 32a for the via hole and the opening 32b for the register mark. Thus, an opening 30a (20 μm in diameter) and register marks 30b and 30b' are formed. See Fig. 5(H). The etching resist 32 is removed with an aqueous solution of sodium hydroxide. See Fig. 6(I). The thus obtained board 20, which has openings 30a and register marks 30b is shown in Fig. 6(A). In Fig. 6(I), two register marks 30b and 30b' are shown on either side; in actuality, however, the register marks 30b and 30b' are positioned on the four corners of the board 20 as shown in Fig. 1. The register marks 30b shown here are annular, but it may also be square as shown in Fig. 8(b).

(6) The board 20 is placed on an X-Y table 80 shown in Fig. 1. The position of the board 20 is determined and corrected with the aid of the register marks 30b thereon, which are sensed by the CCD camera 82. The board is subjected to laser pulses (50 μs) from the laser emitter 60 (400W output and 10.6 μm wave-length). That part of the resin 26 which is exposed to these laser pulses through the openings 30a in the Cu layer 30 is removed. As a result, an opening 26a (20 μm in diameter) for a via hole is formed, through which the copper pattern 22A is partly exposed. See Fig. 6(J1). In other words, the Cu layer (0.5 μm thick) is used as a conformal mask when the opening 26a for a via hole is formed by a laser beam. In this embodiment, the CO₂ laser beam is
Incidentally, the beam should ideally have a diameter larger than 1.3 times the diameter (20 μm) of the opening, so as to ensure that the laser beam drills a via hole through the opening 26a even in the case where the position of the laser beam is slightly dislocated. It follows that the accuracy of the position of the via hole (or the accuracy of the position of the opening 26a for the via hole relative to the register mark 30b) depends on the accuracy of the position of the opening 30a for the via hole relative to the register mark 30b formed on the Cu layer 30 as the conformal mask. Therefore, this embodiment makes it possible to form the via hole at an adequate position even in the case of low accuracy in the laser beam positioning.

In this embodiment, 5000 holes are bored at random on the substrate (500mm × 500mm) with a laser beam. Here, as explained above, the scanning area of the galvano-mirror is 30 × 30mm and the positioning velocity is 400 points/sec in the scanning area. On the other hand, the number of step areas of the X-Y table is 298 (17 × 17). Namely, the laser process is completed by repeating the movement of 30 mm in the X direction 17 times and the movement of 30 mm in the Y direction 17 times. The moving velocity of the X-Y table 80 is 15000mm/min. Meanwhile, the processing time of the four positioning marks 30b by the CCD camera 82 is 9 seconds including the moving time of the table 80. When the substrate 20 is processed by such manufacturing apparatus, the manufacturing time is 289.5 seconds.

(7) The board 20, with the opening 26a formed therein, is dipped in chromic acid for one minute for its de-smearing treatment. Then, the board 20 is dipped in chromic acid solution (800 g/l) at 70°C for three minutes and remove the Cu layer 30 and the plated copper film 40, which are under the resist 38. In this way there are formed a conductor circuit 46 and a via hole 48 (both 16 m thick), each consisting of a Cu layer 30, electrolessly plated copper film 40, and an electrolytically plated copper layer 44. See Fig. 7(N). (8) The board 20 is given a palladium catalyst (from Atotech Corp.) and then dipped in an electroless copper plating solution of the following composition so as to form a 0.5-μm thick copper film 40 on the Cu layer 30 and inside the opening 26a for the via hole. See Fig. 6(K).

**Composition of electroless plating solution**

<table>
<thead>
<tr>
<th>Additive</th>
<th>Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDTA</td>
<td>150 g/l</td>
</tr>
<tr>
<td>Copper sulfate</td>
<td>20 g/l</td>
</tr>
</tbody>
</table>

(9) The electroless plating solution is covered with a commercial photosensitive dry film 34, which is subsequently exposed to light (100 mJ/cm²) through a mask 36 placed thereon which has black spots 36a at prescribed positions. See Fig. 6(L). Exposure is followed by development with 0.8% sodium carbonate solution, which removes the unexposed section. In this way there is obtained a 15-μm thick etching resist 38. See Fig. 7(M).

(10) Electrolytic copper plating is performed under the following conditions so as to form a 15-μm thick copper layer 44. See Fig. 7(N).

**Electrolytic plating solution**

<table>
<thead>
<tr>
<th>Electrolyte</th>
<th>Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sulfuric acid</td>
<td>180 g/l</td>
</tr>
<tr>
<td>Copper sulfate</td>
<td>80 g/l</td>
</tr>
<tr>
<td>Additive</td>
<td>1 ml/l</td>
</tr>
</tbody>
</table>

(11) The resist 38 is removed by treatment with 5% KOH solution. See Fig. 7(O). Etching with a mixture of sulfuric acid and hydrogen peroxide is performed to dissolve and remove the Cu layer 30 and the plated copper film 40, which are under the resist 38. In this way there are formed a conductor circuit 46 and a via hole 48 (both 16 μm thick), each consisting of a Cu layer 30, electrolessly plated copper film 40, and an electrolytically plated copper layer 44. See Fig. 7(P). The board is then dipped in chromic acid solution (800 g/l) at 70°C for three minutes until the interlayer insulating resin layer 26 between the conductor circuits is etched to a depth of 1μm and the surface thereof is cleaned of residual palladium catalyst. This treatment is necessary to ensure insulation between conductor circuits. (For convenience, only one conductor circuit 46 is shown in the figure although an actual printed wiring board has a number of conductor circuits.) In this way it is possible to form a fine conductor circuit 46 about 20 μm wide. By repeating the above-mentioned steps and building up the wiring layer, it is possible to complete a multi-layer printed wiring board.

[0071] In this embodiment, the Cu layer 30 as the conformal mask is formed by sputtering on the interlayer insulating resin layer 26. This means that it is possible to make the conformal mask 30 thin with good adhesion to the interlayer insulating resin layer 26. The advantage of having such a thin conformal mask 30, is that it can be easily removed by etching when the conductor circuit 46 and the via hole 48 are formed, hence there is no possibility of the etching severely damaging the electrolytically
plated copper layer 44 which forms the conductor circuit 46 and the via hole 48. This results in wiring with a fine pitch and via holes with an extremely small diameter:

[0072] Incidentally, the Cu layer 30 formed by sputtering and the film 40 formed by electroless plating should ideally be thinner than 2.0 μm so that they undergo etching easily when their unnecessary parts are removed.

[0073] The above-mentioned embodiment may be modified by replacing the galvano head for scanning with a polygon mirror and replacing the CO₂ laser with any other laser. Also, instead of directing a laser beam to the opening 30a of the Cu layer 30 one by one in the above-mentioned embodiment, it is possible to scan the entire surface of the board with a laser beam so that the resin 26 under the opening 30a is removed.

[0074] Instead of forming the interlayer insulating resin layer and the metal film sequentially in the above-mentioned embodiment, it is also possible to form them simultaneously. In this case, the steps shown in Figs. 4(D) and 5(E) are replaced by those shown in Figs. 9(D') and 9(E'). In the step shown in Fig. 9(D'), the board 120 is laminated with a prepreg 126 and a metal foil 130. In the process shown in Fig. 9(E'), these layers are bonded together through curing by hot pressing. (The prepreg is a glass fiber cloth or aramid fiber cloth impregnated with a resin in B stage. A resin film may replace it in B stage.)

[0075] Another embodiment in which the interlayer insulating resin layer and the metal film are formed simultaneously is explained below with reference to Fig. 10.

1. A 9-μm thick copper foil 230 is coated on one side thereof with an epoxy resin of cresol-novolak type. By heating at 60°C for three hours, the resin is converted into B-stage resin 226. Thus there is obtained a resin film 250. See Fig. 10(A).

2. On both sides of the board 20 an internal layer copper pattern 22A, and a register mark 22B, are formed in the same manner as in step (1) of the first embodiment, which was explained above with reference to Fig. 4(B). See Fig. 10(B).

3. On the surface of the internal layer copper pattern 22A a 2.5-μm thick Ni-P-Cu alloy layer with a rough surface is manifested in the same manner as in step (2) of the first embodiment, which was explained above with reference to Fig. 4(C). See Fig. 10(B). On this rough surface a 0.3-μm thick tin-substituted plating layer is created (not illustrated).

4. The board 20 is sandwiched between two pieces of the resin film 250, which has been prepared in step (1). See Fig. 10(D). The resulting laminate is hot-pressed at 120°C for one hour and at 150°C for three hours under a pressure of 10 kg/cm². In this way there are formed the interlayer insulating resin layer 26 and the metal film 230. See Fig. 10(E).

5. A multi-layer printed circuit board is produced in the same manner as in steps (4) to (11), which were explained above with reference to Fig. 5(E) to Fig. 7(P).

[0076] Another example of a modified embodiment will be explained with reference to Figs. 11 and 12.

[0077] It is characterized by the register mark 30b being circular instead of annular (as in the previous embodiment) and the mark 230B also being circular.

[0078] The board 20 is provided with a sub-layer mark 220B and a conductor circuit 22A, as shown in Fig. 11(B). The sub-layer mark 220B and the conductor circuit 22A have their surfaces roughened, as shown in Fig. 11(C). The copper-clad resin film 250, which is shown in Fig. 11(A), is laminated as shown in Fig. 11(D). The laminate is heat-pressed to form the interlayer insulating resin layer 226 and the metal film 230, as shown in Fig. 11(E). The copper foil 30 is etched to form an opening 30b for the register mark and an opening 30a for the via hole, as shown in Fig. 12(F).

[0079] The sub-layer mark 220B under the register mark 30b is viewed by the CCD camera 82 through the resin layer 226 to determine and correct the position of the board 20, as shown in Fig. 12(G). A laser beam is directed at the opening 30a in the Cu layer 30 so as to remove that part of the resin layer 226 which is exposed through it. This process creates an opening 26a (20 μm in diameter) for the via hole, as shown in Fig. 12(H). Being covered with the resin 26, the sub-layer mark 220B does not oxidize to decrease in reflectivity, nor does it peel off (hence it poses no problem with recognition in silhouette). In this embodiment, therefore, it is possible to determine and correct the position of the board 20 relative to the sub-layer mark 220B and to control the direction of the laser beam relative to the register mark 30b.

[0080] The sub-layer 220B is an index for the position of the internal layer pad to which the via hole is connected, and the register mark 30b is an index for the position of the via hole. Therefore, if the sub-layer mark 220B and the register mark 30b are excessively dislocated relative to each other, it follows that the via hole will not connect to the internal layer pad. Measuring the amount of relative dislocation makes it possible to detect defects during the fabricating process.

Exploitation in Industry

[0081] As explained above, the present invention ensures the accurate positioning of the opening for a via hole even in the case of the laser beam aiming with low accuracy. This is advantageous to mass production of multi-layer printed wiring boards, which require hundreds to thousands of holes to be drilled by laser beams.

[0082] In addition, the present invention permits the laser scanning head to operate faster with low accuracy for the position of laser aiming without sacrificing the accuracy for sensing the position of the opening for a via
hole. The result is an increase in the number of openings to be formed per unit time, hence increasing productivity.

Claims

1. A process for producing a multi-layer printed wiring board, which comprises following steps (a) to (c).

(a) forming an interlayer insulating resin layer (26) having a metal film (30), an opening (30a) formed in said metal film and a register mark (30b) on the surface thereof on a board (20) covered with a conductor layer (22),
(b) removing that part (26a) of said interlayer insulating resin layer which is exposed through the opening (30a) in said metal film, by irradiation of a laser beam aimed at said opening according to data obtained by sensing the position of said register mark (30b), thereby forming an opening through which a via hole is formed, and
(c) forming via holes and conductor circuits.

2. The process according to claim 1, wherein step (c) comprises following steps (d) to (g).

(d) forming a film by electroless plating on said board obtained in step (b) above,
(e) forming a plating resist on said board obtained in step (d) above,
(f) performing electrolytic plating on section where said plating resist is not formed, and
(g) removing said plating resist and, removing by etching, said metal film and electrolessly plated film under said plating resist, thereby forming a via hole and a conductor circuit.

3. The process according to claim 1 or 2, wherein in step

(a) openings are formed in said metal film and register marks on the surface thereof on said board covered with said conductor layer; and step (b) further comprises the following steps:

placing said board with said register marks on a table of an apparatus for producing a multi-layer printed wiring board, said apparatus including: an emitter of fabricating laser, a scanning head to deflect direction of a laser beam in X-Y directions, a camera to sense a register mark on a board, a table to support a board, an entry part for entrance of data for fabricating a board, a memory to store fabricating data or computed results, and an operation part, entering processing data into said apparatus,
sensing position of a register mark on a board by means of said camera and comparing results of sensing with previously entered processing data, thereby generating in an operation part, data necessary to drive said scanning head, said table, and storing data in memory, irradiating openings in said metal film with a laser beam, with said scanning head and table controlled by a control part which reads driving data from memory, thereby removing said interlayer resin layer to form openings through which via holes are created.

4. The process according to claim 3, wherein step (b) comprises:

sensing positions of register marks on a board by means of said camera.

5. A process for producing a printed wiring board as defined in one of Claims 1 to 4, wherein said register mark is an opening formed in said metal film and sensing of said register mark is accomplished by sensing said sub-layer mark which is visible in an opening formed in said metal film through said interlayer insulating resin layer.

6. A process for producing a printed wiring board as defined in one of claims 1 to 5, wherein said opening and said register mark are formed in said metal film at a same time.

Patentansprüche

1. Verfahren zum Herstellen einer mehrschichtigen gedruckten Leiterplatte, das die folgenden Schritte (a) bis (c) aufweist:

(a) Bilden einer isolierenden Harzzwischen- schicht (26), die einen Metallfilm (30), eine im Metallfilm ausgebildete Öffnung (30a) und eine Registermarke (30b) auf dessen Oberfläche aufweist, auf einer mit einer Leiterschicht (22) bedeckten Platte (20);
(b) Entfernen des Teils (26a) der isolierenden Harzzwischenschicht, die durch die Öffnung (30a) im Metallfilm freiliegt, durch Einstrahlung eines auf die Öffnung gerichteten Laserstrahls gemäß Daten, die durch Abtasten der Position der Registermarke (30b) erhalten werden, wo- durch eine Öffnung gebildet wird, durch die ein Kontaktloch gebildet wird, und
(c) Bilden von Kontaktlöchern und Leiterschalt- kreisen.
2. Verfahren nach Anspruch 1, wobei Schritt (c) die folgenden Schritte (d) bis (g) aufweist:

(d) Bilden eines Films durch stromloses Galvanisieren auf der im obigen Schritt (b) erhaltenen Platte,
(e) Bilden eines Galvanoresists auf der im obigen Schritt (d) erhaltenen Platte,
(f) Durchführen eines elektrolytischen Galvanisiersens auf einem Abschnitt, wo das Galvanoresist nicht ausgebildet ist, und
(g) Entfernen des Galvanoresists und Entfernen des Metallfilms und des stromlos galvanisierten Films unter dem Galvanoresist durch Ätzen, wodurch ein Kontaktloch und ein Leiterschaltkreis gebildet werden.

3. Verfahren nach Anspruch 1 oder 2, wobei im Schritt (a) Öffnungen im Metallfilm und Registermarken auf dessen Oberfläche auf der mit der Leiterschicht bedeckten Platte gebildet werden; und Schritt (b) ferner die folgenden Schritte aufweist:

Anordnen der Platte mit den Registermarken auf einen Tisch einer Vorrichtung zur Herstellung einer mehrschichtigen gedruckten Leiterplatte, wobei die Vorrichtung aufweist: einen Strahler eines Fertigungslasers, einen Ablenkkopf, um die Richtung eines Laserstrahls in X-Y-Richtungen abzulenken, eine Kamera, um eine Registermarke auf einer Platte abzutasten, einen Tisch, um eine Platte zu halten, ein Eingabeteil zur Eingabe von Daten zur Fertigung einer Platte, einen Speicher, um Fertigungsdaten oder Berechnungsergebnisse zu speichern, und ein Betriebsteil,
Eingeben von Bearbeitungsdaten in die Vorrichtung, Abtasten der Position einer Registermarke auf einer Platte mittels der Kamera.

4. Verfahren nach Anspruch 3, wobei Schritt (b) aufweist:

Abtasten von Positionen von Registermarken auf einer Platte mittels der Kamera.

5. Verfahren zum Herstellen einer gedruckten Leiterplatte nach einem der Ansprüche 1 bis 4, wobei die Registermarke eine im Metallfilm ausgebildete Öffnung ist, und das Abtasten der Registermarke durch Abtasten der Unterschichtmarke erreicht wird, die in einer Öffnung sichtbar ist, die durch die isolierende Harzzwischenschicht im Metallfilm ausgebildet ist.

6. Verfahren zum Herstellen einer gedruckten Leiterplatte nach einem der Ansprüche 1 bis 5, wobei die Öffnung und die Registermarke im Metallfilm gleichzeitig gebildet werden.

Revendications

1. Procédé pour produire une carte à circuit imprimé multicouches, qui comprend les étapes (a) à (c) suivantes :

(a) formation d’une couche intercalaire de résine isolante (26) dotée d’un film métallique (30), d’une ouverture (30a) formée dans le film métallique et d’un repère (30b) à la surface de celui-ci sur une carte revêtue d’une couche conductrice (22);
(b) suppression de la partie (26a) de la couche intercalaire de résine isolante qui est exposée par l’ouverture (30a) dans le film métallique, par irradiation d’un faisceau laser dirigé vers l’ouverture en fonction des données obtenues en détectant la position du repère (30b), formant ainsi une ouverture à travers laquelle est formé un trou d’interconnexion, et
(c) formation de trous d’interconnexion et de circuits conducteurs.

2. Procédé selon la revendication 1, où l’étape (c) comprend les étapes (d) à (g) suivantes :

(d) formation d’un film par placage anélectrolytique sur la carte obtenue à l’étape (b) susmentionnée,
(e) formation d’une réserve de placage sur la carte obtenue à l’étape (d) susmentionnée,
(f) réalisation d’un placage électrolytique sur la section où la réserve de placage n’est pas formée, et
(g) suppression de la réserve de placage et suppression par attaque chimique du film métallique et du film plaqué de manière anélectrolytique sous la réserve de placage, formant ainsi un trou d’interconnexion et un circuit conducteur.

3. Procédé selon la revendication 1 ou la revendication 2, où, en étape (a), des ouvertures sont formées sur
le film métallique et des repères à la surface de celui-ci revêtus de la couche conductrice ; et où l’étape (b) comprend en outre les étapes suivantes :

positionnement de la carte avec les repères sur une table d’un appareil pour la production d’une carte à circuit imprimé multicouches, ledit appareil comprenant : un émetteur de fabrication par laser, une tête de balayage pour varier la direction d’un faisceau laser en directions X-Y, une caméra pour détecter un repère sur une carte, une table pour supporter une carte, une partie d’entrée pour l’entrée des données de fabrication d’une carte, une mémoire pour stocker les données de fabrication ou les résultats calculés, et une partie de fonctionnement, entrée des données de traitement dans l’appareil, détection de position d’un repère sur une carte au moyen de la caméra et comparaison des résultats de détection avec les données de traitement préalablement entrées, générant ainsi dans une partie de fonctionnement les données nécessaires pour entraîner la tête de balayage, la table, et stockage des données en mémoire, irradiation des ouvertures dans le film métallique par un faisceau laser, la tête de balayage et la table étant commandées par une partie de commande lisant les données d’entraînement dans la mémoire, supprimant ainsi la couche intercalaire de résine pour former des ouvertures à travers lesquelles sont réalisés les trous d’interconnexion.

4. Procédé selon la revendication 3, où l’étape (b) comprend :

détectection des positions de repères sur une carte au moyen de la caméra.

5. Procédé pour produire une carte à circuit imprimé selon l’une des revendications 1 à 4, où le repère est une ouverture formée dans le film métallique et où la détection dudit repère est exécutée par détection du repère de sous-couche visible dans une ouverture formée dans le film métallique à travers la couche intercalaire de résine isolante.

6. Procédé pour produire une carte à circuit imprimé selon l’une des revendications 1 à 5, où l’ouverture et le repère sont formés simultanément dans le film métallique.
Fig. 2

82  CCD  CAMERA
54  INPUT  SECTION
52  MEMORY  SECTION
60  LASER
50
50
70  GALVANO-HEAD

COMPUTER

80  X-Y  TABLE
Fig. 3

HOLE COORDINATES DATA

1st PROCESS

TARGET DATA

MOVING THE TARGET TO THE CAMERA POSITION

2nd PROCESS

MARSURING AN ERROR WITE A CAMERA

3rd PROCESS

GENERATION OF ERROR DATA

4th PROCESS

GENERATION OF REAL PROCESSING DATA

5th PROCESS

GENERATION OF GALVANO DATA

6th PROCESS

GENERATION OF TABLE DATA

7th PROCESS

GENERATION OF LASER DATA

GALVANO-HEAD DRIVE

TABLE DRIVE

LASER OSCILLATION
Fig. 9
REFERENCES CITED IN THE DESCRIPTION

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