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(54) APPARATUS AND METHOD FOR PROTECTING A MEMORY

VORRICHTUNG UND VERFAHREN ZUM SCHUTZ EINES SPEICHERS

APPAREIL ET PROCEDE PERMETTANT DE PROTEGER UNE MEMOIRE

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Description

[0001] The present invention generally relates to electrical devices such as television signal receivers, and more particularly, to a technique for protecting a memory included in such a device from being inadvertently written to when, for example, signal control lines connected to the memory are shared between different devices.

[0002] Electrical devices such as television signal receivers often include one or more circuit boards. Each circuit board typically has attached thereto electrical components, such as integrated circuits ("ICs") and other elements, which enable various device operations to be performed. Prior designs for television signal receivers often employed only a single circuit board. With these prior designs, a primary incentive was to maximize the use of board area. However, since only one circuit board was used, no issues regarding connections between different circuit boards existed.

[0003] Current designs for television signal receivers, on the other hand, may use multiple circuit boards. The use of multiple circuit boards, as compared to a single board, is particularly attractive since it enables the circuit design to be modularized. In particular, different board sections can be re-designed without having to reorganize the layout of all receiver circuits, as is often the case when using only a single circuit board. Moreover, the use of multiple circuit boards allows a single-sided board to be used for one group of circuits, and a multi-layer board for other circuits.

[0004] Despite its advantages, the use of multiple circuit boards does create disadvantages regarding connections between different boards. In particular, it is desirable to minimize the number of connectors (e.g., pins) used to provide a connection between circuit boards. Minimizing the number of such connectors is especially desirable since the cost of each connector is quantifiable in a monetary sense. This is particularly significant in certain industries, such as the consumer electronics industry, where product cost is a driving force among competitors. Accordingly, there is a need for a technique which reduces the number of connections required between circuit boards in an apparatus, such as a television signal receiver.

[0005] One such technique for reducing the number of connections between circuit boards involves sharing signal control lines connected between two circuit boards of an apparatus, such as a television signal receiver. According to this technique, a microcontroller on one circuit board uses the signal control lines to read a memory on another circuit board when the apparatus is in the OFF state, and uses the same signal control lines to control another operation of the apparatus (e.g., a deflection operation) when the apparatus is in the ON state.

[0006] In practicing the aforementioned technique, a problem has been identified in that the memory may be inadvertently written to when the microcontroller uses the signal control lines to control an apparatus operation while the apparatus is placed in the ON state. Accordingly, there is a need for a technique that enables the signal control lines to be shared, but prevents the memory connected to the lines from being inadvertently written to by the microcontroller, or other devices connected to the control lines. The present invention addresses these and other issues.

[0007] In accordance with the present invention, an apparatus includes first and second circuit boards. The first circuit board includes a memory, and control circuitry for controlling at least one function of the apparatus. The second circuit board is operably coupled to the first circuit board via control lines. The second circuit board includes a controller for generating first and second control signals. The control lines transmit the first control signals from the controller to the memory when the apparatus is in a first operational state, and transmit the second control signals from the controller to the control circuitry when the apparatus is in a second operational state. To prevent inadvertent writes to the memory during the second operation state, the memory is placed in an unpowered state during the second operational state when the controller transmits the second control signals to the control circuitry. Additionally, the memory is coupled to means for preventing the memory from keeping the control lines in a low state during the unpowered state.

[0008] In an exemplary embodiment, the apparatus comprises a television signal receiver having a first circuit board that has attached thereto a memory device and circuitry for controlling deflection, a second circuit board that has attached thereto a microcontroller, the first and second circuit boards being coupled to each other via control lines. In the first operational state the microcontroller generates first control signals via the control lines to retrieve operational data from the memory, and in the second operational state the microcontroller uses the retrieved operational data to control the circuitry for controlling deflection. During the second operational state the microcontroller places the memory in an unpowered state. The memory device may include means for preventing the memory device from loading the control lines, thereby allowing the other devices connected to the control line to continue communicating. In one embodiment, the memory includes a zener diode coupled to the Vcc input to prevent the memory, in the unpowered state, from keeping the control lines in the low state. This ensures that the microcontroller can continue to communicate with the control circuitry via the control lines. A method performed by the foregoing apparatus is also disclosed herein.

[0009] The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become more apparent and the invention will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a diagram of a relevant portion of an appa-
ratus suitable for implementing the present invention; and
FIG. 2 is a flowchart illustrating exemplary steps for practicing the present invention.

The exemplifications set out herein illustrate preferred embodiments of the invention, and such exemplifications are not to be construed as limiting the scope of the invention in any manner.

Referring now to the drawings, and more particularly to FIG. 1, a diagram of a relevant portion of an apparatus 100 suitable for implementing the present invention is shown. For purposes of example and explanation, apparatus 100 of FIG. 1 is represented as a television signal receiver. However, it is noted that the principles of the present invention may be applicable to other types of electronic devices, particularly those that utilize multiple circuit boards connected together.

Receiver 100 of FIG. 1 comprises a first circuit board 10, a second circuit board 20, and a board connector 30. According to an exemplary embodiment, first circuit board 10 enables operations related to power supply and deflection functions of receiver 100, and second circuit board 20 enables operations related to signal processing functions of receiver 100. First board 10 is electrically connected to second circuit board 20 via board connector 30.

First circuit board 10 includes a switch mode transformer ("SMT") 11, which enables receiver 100 to be placed in the ON or OFF state in response to, for example, a user input. An electrically erasable, programmable read-only memory ("EEPROM") 12 operates as a non-volatile memory for storing data, such as voltage data used to control deflection operations of receiver 100. EEPROM 12 includes a voltage input ("Vcc") terminal, a clock ("CLK") terminal, and a data ("DAT") terminal. The Vcc terminal is electrically coupled to receive a signal that turns EEPROM 12 ON and OFF. Transistor Q1 is preferably embodied as an NPN-type bipolar junction transistor ("BJT"). Capacitor C1 is a bypass capacitor for transistor R2 has a preferred value of 1 K ohms. The collector junction of transistor Q1 is electrically coupled to the Vcc terminal of EEPROM 12, and provides the signal that turns EEPROM 12 ON and OFF. Transistor Q1 is preferably embodied as an NPN-type bipolar junction transistor ("BJT"). Capacitor C1 is a bypass capacitor for EEPROM 12, and has a preferred value of 100 nanofarads.

Resistors R3 and R4 are provided to create resistance on SDA 15 and SCL 13, respectively. According to an exemplary embodiment, resistors R3 and R4 each provide 1K ohms of resistance. As indicated in FIG. 1, SCL 13 and SDA 15 are tapped in first circuit board 10 to provide two separate control channels. In particular, SDA 15 is tapped to provide a first control channel which generates an output signal represented at reference numeral 17, and SCL 13 is tapped to provide a second control channel, which generates an output signal represented at reference numeral 19. Output signals 17 and 19 control deflection operations of receiver 100. The circuitry making up the first and second control channels may collectively be referred to herein as control circuitry.

The first control channel includes resistors R5 to R7, capacitor C2, and transistor Q2. Resistor R5 provides a resistance between SDA 15 and the base junction of transistor Q2, and has a preferred value of 10K ohms. Transistor Q2 is preferably embodied as an NPN-type BJT. The collector junction of transistor Q2 provides an output path for the first control channel. Resistor R6 operates as a pull-up resistor and is electrically coupled to a voltage source V2, which according to an exemplary embodiment is 5.1 volts. The preferred value for resistor R6 is 1 K ohms. Resistor R7 and capacitor C2 establish a time constant, and preferably have values of 1 K ohms and 820 nanofarads, respectively. According to an exemplary embodiment, output signal 17 is used to establish the voltage of a flyback transformer (not shown), which is used in the deflection operations of receiver 100.

The second control channel includes resistors R8 to R10, capacitor C3, and transistor Q3. Resistor R8 provides a resistance between SCL 13 and the base junction of transistor Q3, and has a preferred value of 10K ohms. Transistor Q3 is preferably embodied as an NPN-type BJT. The collector junction of transistor Q3 provides an output path for the second control channel. Resistor R9 operates as a pull-up resistor and is electrically coupled to voltage source V2, which as previously indicated is 5.1 volts. The preferred value for resistor R9 is 1 K
ohms. Resistor R10 and capacitor C3 establish a time constant, and preferably have values of 1 K ohms and 820 nanofarads, respectively. According to an exemplary embodiment, output signal 19 is used to control the voltage of the flyback transformer (not shown).

[0018] Second circuit board 20 includes a microcontroller 21, which controls various operations of receiver 100. Microcontroller 21 includes an input/output ("I/O") terminal, a CLK terminal and a DAT terminal. The I/O terminal is electrically coupled to a signal line 22 and provides, among other things, an output signal that enables various components of receiver 100 to be powered up when receiver 100 is turned on. The CLK terminal is electrically coupled to SCL 13, and the DAT terminal is electrically coupled to SDA 15. Although not expressly shown in FIG. 1, microcontroller 21 is electrically coupled to a voltage source, such as voltage source V1. The terms "microcontroller" and "controller" may be used interchangeably herein.

[0019] Microcontroller 21 also includes first and second pulse width modulated ("PWM") terminals ("PWM1" and "PWM2"), which output first and second PWM signals, respectively. The PWM1 and PWM2 terminals are electrically coupled to SDA 15 and SCL 13, respectively, and thereby provide the first and second PWM signals to the first and second control channels of first circuit board 10, respectively. Accordingly, the first PWM signal is used to generate output signal 17, and the second PWM signal is used to generate output signal 19. While PWM signals are utilized in a preferred embodiment, signals of other formats may, of course, also be utilized.

[0020] Second circuit board 20 also includes six resistors R11 to R16, and three capacitors C4 to C6. Resistor R11 operates as a pull-up resistor for signal line 22 connected to the I/O terminal of microcontroller 21, and is electrically coupled to voltage source V1, which as previously indicated is 3.3 volts. Resistor R11 has a preferred value of 10K ohms. Resistor R12 and capacitor C4 operate to filter out radio frequency interference from the signal line connected to the I/O terminal of microcontroller 21. Resistor R12 and capacitor C4 have preferred values of 1 K ohms and 1 nanofarad, respectively. Similarly, resistor R13 and capacitor C5 operate to filter out radio frequency interference from SDA 15, while resistor R14 and capacitor C6 operate to filter out radio frequency interference from SCL 13. According to an exemplary embodiment, resistors R13 and R14 each have values of 1 K ohms, and capacitors C5 and C6 each have values of 100 picofarads. Resistors R15 and R16 operate as pull-up resistors and are electrically coupled to voltage source V1, which as previously indicated is 3.3 volts. Resistors R15 and R16 each have preferred values of 10K ohms.

[0021] In operation, the IIC bus (i.e., SCL 13 and SDA 15) is shared between two different operations of microcontroller 21. In particular, when receiver 100 is in a first operational state (i.e., receiver 100 is connected to a power source, but is in the OFF state), microcontroller 21 operates as a master IC and transmits first control signals to EEPROM 12 via SCL 13 and SDA 15 to thereby read data from EEPROM 12, which operates as a slave IC. Microcontroller 21 and EEPROM 12 receive electrical power from a standby power source, namely voltage source V1, during the first operational state. According to an exemplary embodiment, the data read from EEPROM 12 by microcontroller 21 comprises voltage data used to control deflection operations of receiver 100.

[0022] During the data reading operation, SCL 13 propagates clock signals from microcontroller 21 to EEPROM 12. SDA 15 is used to transfer data using serial digital transactions. Typically, one or more bits are used as acknowledgment bits. According to an exemplary design, when both SCL 13 and SDA 15 are held in a logic high state, no data can be transferred between microcontroller 21 and EEPROM 12. A transition from a logic high state to a logic low state on SDA 15, while SCL 13 is in a logic high state, indicates a stop condition. According to an exemplary embodiment, microcontroller 21 generates one clock pulse for each bit of digital data transferred on SDA 15, and a logic state on SDA 15 can only change when the clock signal on SCL 13 is in a logic low state. Of course, signal protocols other than the foregoing one may be used. When microcontroller 21 reads data from EEPROM 12, the PWM1 and PWM2 terminals of microcontroller 21 are in a high-impedance state, and resistors R5 and R8 prevent the control circuitry of the first and second control channels from loading SDA 15 and SCL 13. The input and output status of the pins of microcontroller 21, and thus the impedance, may be controlled as known, such as via the data direction registers.

[0023] When receiver 100 is in a second operational state (i.e., receiver 100 is connected to a power source and placed in the ON state), the DAT and CLK terminals of microcontroller 21 are in a high-impedance state, and the PWM1 and PWM2 terminals may be used to output the first and second PWM signals, respectively. The first and second PWM signals may be referred to herein as second control signals. The PWM1 terminal is electrically coupled to SDA 15 and thereby provides the first PWM signal to the first control channel of first circuit board 10 to enable generation of output signal 17. Similarly, the PWM2 terminal is electrically coupled to SCL 13 and thereby provides the second PWM signal to the second control channel of first circuit board 10 to enable generation of output signal 19. According to an exemplary embodiment, the first and second PWM signals are generated by microcontroller 21 in dependence upon the voltage data read from EEPROM 12 in the first operational state, i.e., when receiver 100 is in the OFF state. In the aforementioned manner, SCL 13 and SDA 15 are shared between two different devices during two different operations of microcontroller 21. Capacitor C1 may be includ-
ed between the Vcc input terminal and the ground terminal to compensate for the peak currents during data read/write operations to EEPROM 12.

[0024] When the first and second PWM signals are transmitted to the control circuitry of first circuit board 10, as described above, a potential problem has been recognized in that EEPROM 12 can be inadvertently written to and thereby corrupt data stored within EEPROM 12. In particular, when the PWM signals are transmitted over the IIC bus, if a start condition is generated (i.e., a transition from a logic high state to a logic low state on SDA 15, while SCL 13 is in a logic high state), and address information generated by the phasing of the PWM signals corresponds to address information of EEPROM 12, then EEPROM 12 may be inadvertently written to by microcontroller 21.

[0025] To avoid this potential problem, the present invention causes electrical power to be removed from EEPROM 12 before the PWM signals are transmitted over the IIC bus. More specifically, when receiver 100 is placed in the ON state, and thereby enters the second operational state, microcontroller 21 outputs a power control signal from its I/O terminal to signal line 22. The power control signal is transferred to first circuit board 10 via board connector 30, and controls certain power functions of receiver 100. In particular, the power control signal, which according to an exemplary embodiment is a logic high signal, is provided to SMT 11 which turns ON a power supply (not shown) of receiver 100 used during the second operational state. Moreover, the power control signal is provided to the base junction of transistor Q1, which operates as an inverter, and thereby disconnects voltage source V1 from the Vcc terminal of EEPROM 12. Then, once EEPROM 12 is in an unpowered state, microcontroller 21 can transmit the PWM signals over the IIC bus without the risk of inadvertently writing to EEPROM 12.

[0026] In the exemplary embodiment, EEPROM 12 includes means for preventing EEPROM 12 from loading down control lines 13 and 15 when EEPROM 12 is in the unpowered state. Generally, ICs include electrostatic discharge (“ESD”) protection diodes coupled to the pins. In the present embodiment, EEPROM 12 includes the above-mentioned preventing means coupled to, for example, the Vcc pin. Various devices and methods that are known for providing such functionality, for example, zener diodes, and bipolar transistors, may be used.

[0027] Referring now to FIG. 2, a flowchart 200 illustrating exemplary steps for practicing the present invention is shown. For purposes of example and explanation, the steps of FIG. 2 will be described with reference to television signal receiver 100 of FIG. 1.

[0028] At step 201, receiver 100 is in an unpowered state. That is, receiver 100 is not connected to an electrical power source, such as a household plug outlet or the like. At step 202, receiver 100 is connected to an electrical power source (e.g., plugged in), but is not turned on. That is, receiver 100 enters the first operational state at step 202. As previously indicated herein, certain components of receiver 100, such as microcontroller 21 and EEPROM 12 receive electrical power from a standby power source, namely voltage source V1, during the first operational state.

[0029] In response to being connected to a power source at step 202, process flow advances to step 203, where receiver 100 performs an initialization process. In particular, as part of this initialization process, microcontroller 21 operates as a master IC and transmits the first control signals to EEPROM 12 via SCL 13 and SDA 15 to thereby read data from EEPROM 12, which operates as a slave IC. According to an exemplary embodiment, the data read from EEPROM 12 by microcontroller 21 comprises voltage data used to control deflection operations of receiver 100. Microcontroller 21 stores the read data in an internal memory (not shown), and retains it there as long as receiver 100 is plugged in, or otherwise powered.

[0030] Next, at step 204, receiver 100 is turned on, for example, in response to receiving a user input at an input terminal such as a hand-held remote control unit. As previously indicated herein, receiver 100 is in the second operational state when it is both connected to a power source, and turned on. Accordingly, step 204 causes receiver 100 to enter the second operational state. In response to step 204, microcontroller 21 outputs the power control signal from its I/O terminal to signal line 22. The power control signal causes, among other things, transistor Q1 of first circuit board 10 to disconnect voltage source V1 from the Vcc terminal of EEPROM 12, at step 205.

[0031] Then, once EEPROM 12 is in an unpowered state, process flow advances to step 206 where microcontroller 21 transmits the second control signals, namely the first and second PWM signals, to the control circuitry of first circuit board 10. That is, the PWM1 terminal outputs the first PWM signal to SDA 15, and thereby provides the first PWM signal to the control channel of first circuit board 10 to enable generation of output signal 17. Similarly, the PWM2 terminal outputs the second PWM signal to SCL 13, and thereby provides the second PWM signal to the second control channel of first circuit board 10 to enable generation of output signal 19. As previously indicated, the first and second PWM signals may be generated by microcontroller 21 in dependence upon the voltage data read from EEPROM 12 at step 203. In the aforementioned manner, SCL 13 and SDA 15 are shared between two different operations of microcontroller 21, and the risk of inadvertently writing to EEPROM 12 is avoided.

[0032] Although the present invention has been described in relation to a television signal receiver, the invention is applicable to various systems, either with or without display devices, and the phrases “television signal receiver” or “receiver” as used herein are intended to encompass various types of apparatuses and systems including, but not limited to, television sets or monitors.
that include a display device, and systems or apparatuses such as a set-top box, video tape recorder (VTR), digital versatile disk (DVD) player, video game box, personal video recorder (PVR) or other apparatus that may not include a display device.

[0033] While this invention has been described as having a preferred design, the present invention can be further modified within the scope of this invention as defined in the appended claims.

Claims

1. A television signal receiver, comprising:

   - a first circuit board including a memory and control circuitry for controlling an operation of the receiver, the control circuitry controlling the operation of the receiver in response to data stored in the memory; and
   - a second circuit board operably coupled to the first circuit board via IIC bus lines, the second circuit board including a controller, coupled to the IIC bus lines, for generating first control signals in accordance with a first signal format in a first operational state and second control signals in accordance with a second signal format in a second operational state,
   - the controller placing the memory into an unpowered state during the second operational state, the memory being coupled to means for preventing the memory from keeping the control lines at a low state when the memory is in the unpowered state,

   wherein the memory and the control circuitry are coupled to the IIC bus lines, and the controller transmits the first control signals to the memory via the IIC bus lines without affecting the control circuitry, when the receiver is in a first operational state;

2. The television signal receiver according to claim 1, wherein the means for preventing the memory from keeping the control lines in the low state while the memory is in the unpowered state comprises a zener diode.

3. The television signal receiver according to claim 1, wherein the memory includes operational data for controlling deflection circuitry and the control circuitry controls the deflection circuitry in response to the operational data.

4. The television signal receiver according to claim 3, wherein the first operational state corresponds to an OFF state of the receiver, and the second operational state corresponds to an ON state of the receiver.

5. The television signal receiver according to claim 3, wherein the first control signal corresponds to IIC compliant signals and the second control signals are PWM signals.

6. The television signal receiver according to claim 3, wherein the control circuitry is coupled to the IIC bus lines via bipolar transistors.

7. A method of operating a television signal receiver, the method comprising steps of:

   - providing first and second circuit boards coupled via control lines, the first circuit board having a memory device and control circuitry included therein and coupled to the control lines, the second circuit board having a controller included therein and coupled to the control lines;
   - transmitting via the control lines, first control signals in accordance with a first signal format from the controller on the second circuit board to the memory device on the first circuit board, without affecting the control circuitry, when the receiver is in a first operational state;
   - transmitting via the control lines, second control signals in accordance with a second signal format from the controller to the control circuitry on the first circuit board, without affecting the memory device, when the receiver is in a second operational state; and
   - placing the memory device in an unpowered state during the step of transmitting the second control signals, the memory device being coupled to means for preventing the memory device from keeping the control lines in a low state when the memory device is placed in the unpowered state.

8. The method of claim 7, wherein the first operational state corresponds to the receiver being in the OFF state wherein the controller and the memory are supplied by a standby power supply, and the second operational state corresponds to the receiver being in an ON state.

9. The method of claim 8, wherein the first control signals enable the controller to read data from the memory.

10. The method of claim 9, further comprising the step of controlling deflection circuitry via the control circuitry in response to data read from the memory.

11. The method of claim 8, wherein the first transmitting step comprises transmitting the first control signals...
in accordance with the IIC standard.

12. The method of claim 8, wherein the second transmitting step comprises transmitting the second control signals as pulse width modulated signals.

13. The method of claim 8, wherein the providing step comprises providing the first circuit board having the control circuit coupled to the control lines via bipolar transistors.

Patentansprüche

1. Fernsehsignalempfänger, umfassend:

   eine erste Leiterplatte mit Speicher- und Steuerschaltkreisen zur Steuerung einer Arbeitsweise des Empfängers, wobei die Steuerschaltkreise die Arbeitsweise des Empfängers als Reaktion auf in dem Speicher gespeicherte Daten steuern; und

   eine wirksam über IIC-Busleitungen an die erste Leiterplatte angekoppelte zweite Leiterplatte, wobei die zweite Leiterplatte eine an die IIC-Busleitungen angekoppelte Steuerung zum Erzeugen von ersten Steuersignalen gemäß einem ersten Signalformat in einem ersten Betriebszustand und von zweiten Steuersignalen gemäß einem zweiten Signalformat in einem zweiten Betriebszustand enthält,

wobei die Steuerung den Speicher während des zweiten Betriebszustands in einen unversorgten Zustand versetzt, wobei der Speicher an Mittel angekoppelt ist, die verhindern, daß der Speicher die Steuerleitungen in einem Low-Zustand hält, wenn sich der Speicher in dem unversorgten Zustand befindet,

wobei der Speicher und die Steuerschaltkreise an die IIC-Busleitungen angekoppelt sind und die Steuerung in dem ersten Betriebszustand die ersten Steuersignale über die IIC-Busleitungen zu dem Speicher sendet, ohne die Steuerschaltkreise zu beeinflussen, und im zweiten Betriebszustand die zweiten Steuersignale über die Steuerleitungen zu den Steuerschaltkreisen sendet, ohne den Speicher zu beeinflussen.

2. Fernsehsignalempfänger nach Anspruch 1, wobei die Mittel zum Verhindern, daß der Speicher die Steuerleitungen in dem Low-Zustand hält, während sich der Speicher in dem unversorgten Zustand befindet, eine Zenerdiode umfassen.

3. Fernsehsignalempfänger nach Anspruch 1, wobei der Speicher operationale Daten zur Steuerung von Ablenkschaltkreisen enthält und die Steuerschaltkreise die Ablenkschaltkreise als Reaktion auf die operationalen Daten steuern.


5. Fernsehsignalempfänger nach Anspruch 3, wobei das erste Steuersignal IIC-kompatiblen Signalen entspricht und die zweiten Steuersignale PWM-Signale sind.

6. Fernsehsignalempfänger nach Anspruch 3, wobei die Steuerschaltkreise über Bipolartransistoren an die IIC-Busleitungen angekoppelt sind.

7. Verfahren zum Betrieb eines Fernsehsignalempfängers, mit den folgenden Schritten:

   Bereitstellen einer ersten und einer zweiten Leiterplatte, die über Steuerleitungen gekoppelt sind, wobei die erste Leiterplatte darauf vorgesehen eine Speichereinrichtung und Steuerschaltkreise aufweist, die an die Steuerleitungen angekoppelt sind, wobei auf der zweiten Leiterplatte eine Steuerung vorgesehen ist, die an die Steuerleitungen gekoppelt ist;

   Senden der Steuersignale gemäß einem ersten Signalformat aus der Steuerung auf der zweiten Leiterplatte über die Steuerleitungen, ohne die Steuerschaltkreise zu beeinflussen, wenn sich der Empfänger in einem ersten Betriebszustand befindet;

   Senden von zweiten Steuersignalen gemäß einem zweiten Signalformat von der Steuerung zu den Steuerschaltkreisen auf der ersten Leiterplatte über die Steuerleitungen, wenn sich der Empfänger in einem zweiten Betriebszustand befindet; und

   Versetzen der Speichereinrichtung in einen unversorgten Zustand während des Schritts des Sendens der Steuersignale, wobei die Speichereinrichtung an Mittel angekoppelt ist, die verhindern, daß die Speichereinrichtung die Steuerleitungen in einem Low-Zustand hält, wenn die Speichereinrichtung in den unversorgten Zustand versetzt ist.

8. Verfahren nach Anspruch 7, wobei der erste Betriebszustand entspricht, daß sich der Empfänger in dem AUS-Zustand befindet, wobei die Steuerung und der Speicher durch eine Standby-Stromversorgung versorgt werden, und der zweite Betriebszustand entspricht, daß sich der Empfänger in einem...
Revendications

1. Un récepteur de signaux de télévision comprenant :

une première carte de circuit comprenant une mémoire et un circuit de commande pour commander le fonctionnement du récepteur, le circuit de commande commandant le fonctionnement du récepteur en réponse aux données stockées dans la mémoire ; et

une deuxième carte de circuit coupée de manière opérationnelle à la première carte de circuit via les lignes omnibus IIC, la deuxième carte de circuit incluant un contrôleur, coupée aux lignes omnibus IIC, pour générer les premiers signaux de commande selon un premier format de signal dans un premier état de fonctionnement ; et
des deuxièmes signaux de commande selon un deuxième format de signal dans un deuxième état de fonctionnement ;

le contrôleur plaçant la mémoire dans un état non alimenté pendant le deuxième état de fonctionnement, la mémoire étant coupée à un moyen pour empêcher la mémoire de conserver les lignes de commande à un état bas lorsque la mémoire se trouve dans l'état non alimenté, où la mémoire et le circuit de commande sont couplés aux lignes omnibus IIC, et le contrôleur transmet les premiers signaux de commande à la mémoire via les lignes omnibus IIC sans affecter le circuit de commande dans le premier état de fonctionnement, et transmet les deuxième signaux de commande au circuit de commande via les lignes de commande sans affecter la mémoire dans le deuxième état de fonctionnement.

2. Le récepteur de signaux de télévision selon la revendication 1, où le moyen pour empêcher la mémoire de conserver les lignes de commande à l'état bas lorsque la mémoire se trouve dans l'état non alimenté, comporte une diode Zener.

3. Le récepteur de signaux de télévision selon la revendication 1, où la mémoire inclut des données de fonctionnement pour commander le circuit de déviation et le circuit de commande contrôle le circuit de déviation en réponse aux données de fonctionnement.

4. Le récepteur de signaux de télévision selon la revendication 3, où le premier état de fonctionnement correspond à un état OFF du récepteur, et le deuxième état de fonctionnement correspond à un état ON du récepteur.

5. Le récepteur de signaux de télévision selon la revendication 3, où le premier signal de commande correspond à des signaux conformes IIC et les deuxième signaux de commande sont des signaux PWM.

6. Le récepteur de signaux de télévision selon la revendication 3, où le circuit de commande est couplé aux lignes omnibus IIC à l'aide de transistors bipolaires.

7. Un procédé de mise en service d'un récepteur de signaux de télévision, le procédé comprenant les étapes de :

fourniture de la première et de la deuxième carte de circuit via les lignes de commande, la première carte de circuit possédant un dispositif de mémoire et un circuit de commande intégré et étant coupée aux lignes de commande, la deuxième carte de circuit possédant un contrôleur intégré et étant coupée aux lignes de commande;

transmission au moyen des lignes de commande, des premiers signaux de commande selon un premier format de signal du contrôleur sur la deuxième carte de circuit au dispositif de mémoire sur la première carte de circuit, sans affecter le circuit de commande, lorsque le récepteur se trouve dans un premier état de fonctionnement ;

transmission au moyen des lignes de commande, des deuxième signaux de commande selon un deuxième format de signal du contrôleur sur la deuxième carte de circuit à partir du contrôleur au circuit de commande de la première
carte de circuit, sans affecter le dispositif de mémoire lorsque le récepteur se trouve dans un deuxième état de fonctionnement ; et placement du dispositif de mémoire dans un état non alimenté pendant un état non alimenté pendant l’étape de transmission des deuxième signal de commande, le dispositif de mémoire étant couplé à un moyen destiné à empêcher le dispositif de mémoire de conserver les lignes de commande à un état faible lorsque le dispositif de mémoire est placé dans l’état non alimenté.

8. Le procédé de la revendication 7, où le premier état de fonctionnement correspond au récepteur placé dans l’état OFF, où le contrôleur et la mémoire sont alimentés par une alimentation de réserve, et le deuxième état de fonctionnement correspond au placement du récepteur dans l’état ON.

9. Le procédé de la revendication 8, où les premiers signaux de commande permettent au contrôleur de lire les données à partir de la mémoire.

10. Le procédé de la revendication 9, comprenant en outre l’étape de commande du circuit de déviation via le circuit de commande en réponse aux données lues à partir de la mémoire.

11. Le procédé de la revendication 8, où la première étape de transmission comprend la transmission des premiers signaux de commande selon la norme IIC.

12. Le procédé de la revendication 8, où la deuxième étape de transmission comprend la transmission des deuxième signaux de commande sous la forme de signaux à modulation d’impulsions en durée.

13. Le procédé de la revendication 8, où l’étape de fourniture comprend la fourniture de la première carte de circuit dont le circuit de commande est couplé aux lignes de commande à l’aide des transistors bipolaires.
FIG. 2

1. Receiver in unpowered state
2. Receiver connected to power source
3. Initialization; controller reads EEPROM via control lines
4. Receiver turned on
5. EEPROM disconnected from power source
6. Controller transmits PWM signals to control circuitry via control lines