METHOD AND APPARATUS FOR ISOLATING NOISE FROM A TUNER IN A TELEVISION SIGNAL RECEIVER

PROCEDE ET APPAREIL PERMETTANT L'ISOLATION DE BRUIT EN PROVENANCE D'UN SYNTONISEUR DANS UN RECEPTEUR DE SIGNAUX DE TELEVISION
Description

[0001] The present invention generally relates to a television signal receiver, and more particularly, to a method for reducing noise interference in a phase lock loop ("PLL") circuit in a tuner module of a television signal receiver while also permitting bi-directional communication between the tuner module and a controller unit.

[0002] A television system such as a high definition television ("HDTV") system typically employs a front end comprising a tuner, a digital intermediate frequency ("IF") circuit, and a digital demodulation integrated circuit ("IC"). The system may be controlled from a microprocessor using an inter-integrated circuit ("IIC" - typically pronounced "I-squared C") bus.

[0003] An IIC bus is a two line, bi-directional digital bus that permits two ICs to communicate on a bus path at a time. An IC serving in a "master" mode of operation, initiates a data transfer operation on the bus and generates clock signals that permit the data transfer. An IC serving in a "slave" mode of operation is the IC being operated and respective outputs coupled to the tuner module. Each IC has its own unique address and the master IC-initiates and terminates the communications.

[0004] A serial clock line ("SCL") propagates clock signals on the IIC bus from a master IC to a slave IC. Each master IC typically generates its own clock signals when transferring data on the bus. A second bi-directional line of the IIC bus is typically a serial data line ("SDA") that transfers data using serial digital transactions. Typically, one or more bits are used as acknowledgment bits. According to an exemplary design, when both the SCL and SDA are held in a logic high state, no data can be transferred between two ICs on the IIC bus. A transition from a logic high state to a logic low state on the SDA, while the SCL is in a logic high state, indicates a start condition for the exchange of digital data over the IIC bus. Conversely, a transition from a logic low state to a logic high state on the SDA, while the SCL is in a logic high state, indicates a stop condition. The master IC typically generates one clock pulse for each bit of digital data transferred on the SDA, and a logic state on the SDA can only change when the clock signal on the SCL is in a logic low state.

[0005] Multiple ICs typically share an IIC bus. For example, a microprocessor in a controller of a television signal receiver communicates with numerous ICs within the receiver using an IIC bus. This communication, however, can create operational problems within the television receiver. In particular, coincidental bus traffic by the microprocessor, which functions as a master IC, has been found to cause phase noise interference in a tuner of the television receiver. More specifically, phase noise interference may be introduced to a PLL of the tuner that is serially coupled to the IIC bus. The PLL operates as a frequency variable tone generator, and the microprocessor controls the oscillator frequency of the PLL via the IIC bus. The PLL is susceptible to bus traffic when the microprocessor sends commands to other ICs on the bus, so that instead of producing a tone locked at a specific desired frequency, a range of other frequencies around the desired tone frequency are produced.

[0006] For example, in a PLL having a 4 MHz oscillator, any incidental noise signals generated by the microprocessor may be received by other pins of the PLL IC connected to the IIC bus. This noise is added to the resultant frequency. Accordingly, in a situation where a user selects a channel at 701 MHz and the television system requires a down-converted IF signal at 44 MHz, then the PLL must generate a tone locked at a frequency of 745 MHz. Normally, the 701 MHz television signal and the 745 MHz tone signal are mixed to produce an IF signal locked at 44 MHz. However, additional noise will generate other harmonic frequencies around the tone frequency, thereby causing the IF signal to instead fluctuate in a range around 44 MHz.

[0007] As a result, the bus noise is added to the incoming digital video and/or audio signal and causes a degradation in bit error rate ("BER") performance of the television receiver. Ultimately, the bit errors can manifest themselves as additional or missing luminance and chrominance pixel components in the video the user is viewing, as well as cause "clicks and pops" in the audio output. Similarly, when processing an analog television signal, the IIC bus noise can cause distorted images and/or undesirable wow and/or flutter in the audio output.

[0008] Phase noise interference caused by the IIC bus traffic may be compensated somewhat by widening the bandwidth of the demodulation IC's carrier tracking loop, to allow it to "track out" the corruption. However, such a method may allow additional low frequency noise to combine with the video and/or audio signal, thereby degrading the BER of the television receiver.

[0009] An apparatus and method for isolating the noise caused by the IIC bus traffic is described in an international application entitled "Method and Apparatus for Isolating IIC Bus Noise from a Tuner in a Television Receiver" filed December 22, 1999, having application no. PCT/US99/30775. The apparatus described therein provides an isolation buffer that allows the receiver to only pass data to the tuner's phase-lock loop IC when a tune command is issued by a microprocessor. In one embodiment, the isolation buffer comprises a pair of OR gates having respective inputs coupled to the microprocessor and respective outputs coupled to the tuner module. Such an apparatus is suitable when the microprocessor is sending commands to the tuner module. However, there may be situations when it is desired to transmit data from the tuner module to the microprocessor. For example, the tuner module may be a part of a circuit board that includes a EEPROM that includes information required by the microprocessor during tuning events.

Accordingly, there is a need for an improved way to prevent the IIC bus noise from adversely influencing the PLL circuitry of the tuner. In fulfilling this need, however, it is desirable that the microprocessor be able to both transmit and receive signals to and from the tuner and its associated components. Such bi-directional communication capability can, for example, enable the microprocessor to control the operation of the television receiver in a more effective manner, and also allow for more effective placement of components since the components requiring noise isolation may be placed on the same circuit board with components that require bi-directional communications capability with the main processing unit. The present invention addresses these and other issues.

In accordance with the present invention, an apparatus and a method (claims 1 and 9) for isolating a tuner module having a noise intolerant device from a source of noise is provided. The apparatus comprises a digital bus. A processor outputs clock signals and first data signals and receives second data signals over the digital bus. A bi-directional buffer is coupled between the digital bus and the module, which includes the noise intolerant device and devices that need to be transferred to the processor. The apparatus operates such that, in dependence upon a control signal, the bi-directional buffer in a first mode of operation isolates the module from other components on the digital bus, and in a second mode of operation passes the clock signals and the data signals from the digital bus to the module, and passes data signals from the module to the digital bus.

The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become more apparent and the invention will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a diagram illustrating a relevant portion of a television signal receiver suitable for implementing the present invention;
FIG. 2 is a diagram illustrating further details of the tuner of FIG. 1; and
FIG. 3 is a flowchart illustrating exemplary steps for practicing the present invention.

The exemplifications set out herein illustrate preferred embodiments of the invention, and such exemplifications are not to be construed as limiting the scope of the invention in any manner.

Referring now to the drawings, and more particularly to FIG. 1, a diagram of a relevant portion of a television signal receiver 100 suitable for implementing the present invention is shown. In FIG. 1, the illustrated portion of television signal receiver 100 comprises a microprocessor 101, an input/output (“I/O”) port 102, an input unit 103, a serial clock line (“SCL”) 104, a serial data line (“SDA”) 105, a plurality of integrated circuits (“ICs”) 106 to 108, a bi-directional buffer 109, and a tuner module 110.

Microprocessor 101 is electrically connected to, and exchanges signals with, I/O port 102. I/O port 102 receives inputs from input unit 103, which may be embodied for example, as a hand-held remote control unit. Microprocessor 101 is also electrically connected to an inter-integrated circuit (“IIC”) bus comprising SCL 104 and SDA 105. Microprocessor 101 communicates with ICs 106 to 108 via SCL 104 and SDA 105. During this communication, microprocessor 101 operates as a master IC, and ICs 106 to 108 operate as slave ICs, as previously discussed herein. Although not expressly shown in FIG. 1, a pull-up resistor connected to a 5 volt supply is preferably included on both SCL 104 and SDA 105 adjacent to microprocessor 101. According to an exemplary embodiment, the value of both resistors is 2.2K ohms. The terms “microprocessor” and “processor” are considered interchangeable, for purposes herein.

As indicated in FIG. 1, SCL 104 is a line that carries clock signals generated by microprocessor 101. Conversely, SDA 105 is a bi-directional line, which exchanges data signals between microprocessor 101 and other components, such as ICs 106 to 108 and tuner module 110. For purposes of example and explanation, only three ICs, namely ICs 106 to 108, are shown in FIG. 1. However, in practice a greater or fewer number of such ICs may be connected to the IIC bus.

Bi-directional buffer 109 is electrically connected to microprocessor 101 and ICs 106 to 108 via the IIC bus, namely SCL 104 and SDA 105. Bi-directional buffer 109 comprises transistors Q1 to Q4, and resistors R1 to R6. Transistors Q1 to Q4 are each preferably embodied as an NPN-type bipolar junction transistor (“BJT”), such as a BC847B model transistor available from ST Microelectronics. The use of BJTs to implement bi-directional buffer 109 is particularly advantageous since BJTs provide a significant cost reduction over field effect transistors (“FETs”) or IC switches, while still enabling bi-directional capabilities. FETs may provide an advantage in terms of better rise and fall times. However, in applications where the improved rise and fall times are not necessary, the use of BJTs provides the required bi-directional functionality at a significantly lower cost.

Resistors R1 to R6 exhibit preferred impedance values shown in FIG. 1. That is, resistors R1 and R4 are each 51 K ohms, and resistors R2, R3, R5 and R6 are each 10K ohms. Of course, other impedance values could also be used. However, the values of resistors R1, R2, R4 and R5 must be selected carefully so that operation of the IIC bus is not adversely affected. In the present embodiment, the values of R1 and R4 are selected to maintain a desired voltage when the microprocessor 101 is communicating with module 110 and with other ICs 106-108. In this case, it is necessary to maintain the voltage at a level that allows the other ICs 106-108 to provide acknowledgements while maintaining the required rise and fall times.

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The cutoff control signal that isolates the module 110 is preferably provided from microprocessor 101, but may be provided from another source as necessary. The cutoff control signal is applied to the cutoff control terminals, which are operated to connect the base junctions of transistors Q2 and Q4. Bi-directional buffer 109 selectively passes signals between, for example, microprocessor 101 and tuner module 110 in dependence upon the control signal applied to the cutoff control terminals. That is, bi-directional buffer 109 functions as a switch, which enables communication between microprocessor 101 and tuner module 110, and also isolates tuner module 110 from traffic noise on the IIC bus (i.e., SCL 104 and SDA 105) when microprocessor 101 communicates with ICs 106 to 108.

In operation, transistors Q1 and Q3 of bi-directional buffer 109 are configured to operate in: (1) a saturation mode to enable signal passage between the IIC bus and tuner module 110, and in (2) a cut-off mode to prohibit signal passage and thereby isolate tuner module 110 from any traffic noise on the IIC bus. Signal passage between the IIC bus and tuner module 110 is enabled by supplying current to the base junctions of transistors Q1 and Q3 that is sufficient to enter the saturation mode. For both transistors Q1 and Q3, the emitter and collector junctions are pulled to a logic high state, and a logic low signal at either junction will cause a logic low signal at the other junction. Common emitter saturated switches are formed by transistor Q2 and resistor R2; and by transistor Q4 and resistor R4. Impedance values of resistors R2 and R4 are set just low enough to ensure that the saturation mode is entered, and good signal transitions are measured at the base junction of transistor 110, when bi-directional buffer 109 enables signal passage. Setting the impedance values of resistors R2 and R4 too low, however, can cause excessive amounts of current that must be sunk by devices (e.g., ICs 106 to 108) connected to the IIC bus. According to an exemplary embodiment, the control signal applied to the cutoff control terminals of bi-directional buffer 109 may be any digital signal that represents a logic low state under 600 millivolts, and a logic high state above 1.5 volts.

Tuner module 110 comprises a tuner 111, an electrically-erasable, programmable read-only memory ("EEPROM") 112, and an intermediate frequency ("IF") down-converter 113. According to an exemplary embodiment, tuner module 110 is embodied as a stand-alone module connected to a main board of a television signal receiver. Of course, the components of tuner module 110 may also be embodied as separate components. Tuner 111 receives and operates upon video and/or audio signals in digital and/or analog formats to thereby generate IF signals. Further details regarding tuner 111 will be provided later herein with reference to FIG. 2. Although tuner module 110 in the present embodiment includes tuner 111, EEPROM 112 and IF module 113, it is to be understood that other devices that require noise isolation, or bi-directional communications could be incorporated in module 110, which may comprise a plurality of components arranged on a particular circuit board.

EEPROM 112 stores data, such as electronic alignment data and/or other data, which may be used, for example, by microprocessor 101 to control operation of television signal receiver 100, particularly during a tuning event, for example, to set the tracking filter, set the AGC point, etc. According to the present embodiment, microprocessor 101 may selectively read stored data from EEPROM 112 via SDA 105 and bi-directional buffer 109. Based on this read data, microprocessor 101 controls various operations of television signal receiver 100.

IF down-converter 113 performs a frequency down-conversion operation upon the IF signals provided from tuner 111. According to an exemplary embodiment, IF down-converter 113 is capable of down-converting video and/or audio signals in digital and/or analog formats. Frequency down-converted outputs from IF down-converter 113 is provided to demodulation circuitry and/or additional audio and/or video processing circuitry (not shown), as indicated in FIG. 1. According to an exemplary embodiment, television signal receiver 100 includes circuitry for demodulating and processing video and/or audio signals in digital and/or analog formats.

Referring to FIG. 2, a diagram illustrating further details of tuner 111 of FIG. 1 is shown. As shown in FIG. 2, tuner 111 comprises a phase lock loop ("PLL") 121 having an oscillator (e.g., voltage-controlled oscillator) 122, and a frequency down-converter 123, which is connected to PLL 121 via a signal line 124. PLL 121 receives clock signals and data signals from microprocessor 101 via SCL 104 and SDA 105, respectively, as these signals are selectively passed to PLL 121 by bi-directional buffer 109. Among other things, these received signals may control the frequency of tones generated by oscillator 122. Because PLL 121 is sensitive to traffic noise over the IIC bus, tuner 111 and/or PLL 121 may be referred to herein as a “noise intolerant device.”

Frequency down-converter 123 of tuner 111 receives signals 120, such as video and/or audio signals (e.g., television signals) in digital and/or analog formats. These received signals may be provided, for example, via satellite, cable, terrestrial, wireless, fiber and/or other means. Frequency down-converter 123 converts the received signals to IF signals in accordance with the tone frequency generated by oscillator 122 of PLL 121, and provides the IF signals to IF down-converter 113.

Referring now to FIG. 3, a flowchart illustrating exemplary steps for practicing the present invention is shown. For purposes of example and explanation, the steps of FIG. 3 will be described in relation to television signal receiver 100 of FIGS. 1 and 2.

At step 301, a user provides an input via input unit 303 to select a particular signal 120. In response to the user input, microprocessor 101 controls bi-directional buffer 109 at step 302 to allow signal passage, and thereby enable communication with tuner 111. Once signal passage is allowed, microprocessor 101 transmits a sig-
nal to tuner 111 via the IIC bus and bi-directional buffer 109, thereby causing selected signal 120 to be coupled to frequency down-converter 123 of tuner 111 for further processing, at step 303. As previously indicated herein, selected signal 120 may be a video and/or audio signal (e.g., television signal) in a digital and/or analog format. Moreover, selected signal 120 may be provided to tuner 111, for example, via satellite, cable, terrestrial, wireless, fiber and/or other means known to those skilled in the art.

Next, at step 304, microprocessor 101 transmits a signal to PLL 121 of tuner 111 via the IIC bus and bi-directional buffer 109, thereby causing PLL 121 to generate a specific frequency tone. At step 305, microprocessor 101 then uses the bi-directional communication capabilities of the IIC bus and bi-directional buffer 109 to read data from EEPROM 112 of tuner module 110. According to an exemplary embodiment, microprocessor 101 reads control data from EEPROM 112 relating to filters of tuner 111. Here, microprocessor 101 controls filter settings of tuner 111 by transmitting an appropriate control signal to tuner 111 via the IIC bus and bi-directional buffer 109. However, it is recognized that other types of data may be read by microprocessor 101 and used to control television signal receiver 100.

At step 306, microprocessor 101 controls television signal receiver 100 based on the data read from EEPROM 112. Steps 305 and 306 may be performed separately or together with respect to steps 303 and 304, depending on whether it is necessary to read the data from EEPROM as the tuner 111 is accessed by microprocessor 101. In the present embodiment, EEPROM 112 includes data that is used by television 100 during a tuning event, and as such, the data is read from EEPROM 112 as the tuning commands are transmitted to tuner 111. At step 307, microprocessor 101 controls bi-directional buffer 109 to prohibit signal passage, thereby isolating tuner module 110 from the IIC bus, and any noise thereon.

At step 308, frequency down-converter 123 of tuner 111 combines selected signal 120 with the frequency tone produced by PLL 121 to generate an IF signal. Then, at step 309, the generated IF signal is further processed by IF down-converter 113 and other circuitry (not shown) to generate an output, such as a video and/or audio output. In the present embodiment, wherein it is desirable to enable communications between microprocessor 101 and tuning module 110 during tuning events, it is preferred to enable communications only during certain required times. For example, after a channel change event, it is desirable to enable communications between the processor and the tuning module, but after the tuning event is completed, or a predetermined time after the tuning event is initiated, it is desirable to place the bi-directional buffer in a mode of operation that isolates the processor and the tuner module.

As described herein, the present invention advantageously enables bi-directional communication between microprocessor 101 and tuner module 110, and also isolates tuner module 110 from traffic noise on the IIC bus when microprocessor 101 communicates with ICs 106 to 108 on the bus. By isolating tuner module 110 from traffic noise on the IIC bus, substantial noise is eliminated from PLL 121 of tuner module 110, thereby enabling PLL 121 to lock at a specific desired frequency. Accordingly, PLL 121 generates a clear tone for signal mixing, and a substantially noise free IF signal is produced.

Although the present invention has been described in relation to a television signal receiver, the invention is applicable to various systems, either with or without display devices, and the phrases “television signal receiver,” “television receiver” or “television system” as used herein are intended to encompass various types of apparatuses and systems including, but not limited to, television sets or monitors that include a display device, and systems or apparatuses such as a set-top box, video tape recorder (“VTR”), digital versatile disk (“DVD”) player, video game box, personal video recorder (“PVR”) or other apparatus that may not include a display device. Moreover, it will be appreciated by those skilled in the art that the present invention may be practiced in any system in which digital signals are communicated on an IIC bus. Other signals and systems may illustratively include, but are not limited to, isochronous information transmitted to a television receiver, or digitized data that is transmitted between computers through, for example, cable modems or other means.

While this invention has been described as having a preferred design, the present invention can be further modified within the scope of this disclosure. This application is therefore intended to cover any variations, uses, or adaptations of the invention using its general principles. Further, this application is intended to cover such departures from the present disclosure as come within known or customary practice in the art to which this invention pertains and which fall within the limits of the appended claims.

Claims

1. A television signal processing apparatus (100), comprising:

   a digital bus (104/105);
   a controller assembly including a processor (101), coupled to the digital bus, for outputting clock signals and first data signals and receiving second data signals over the digital bus (104/105);
   a front end assembly including a tuner module (110) having a noise intolerant device (111, 121) coupled to a down converter (113, 123) and a data storage device (112); and
   a bi-directional buffer (109) coupled between the digital bus (104/105) and the tuner module.
(110), wherein, in a first mode of operation the bi-directional buffer (109) isolates the tuner module from the processor, and in a second mode of operation passes the clock signals and the first data signals from the processor to the tuner module and also passes the second data signals from the tuner module to the processor.

2. The television signal processing apparatus of claim 1, wherein the bi-directional buffer (109) comprises:

- a first transistor (Q1) for selectively passing the clock signals from the digital bus (104/105) to the tuner module; and
- a second transistor (Q3) for selectively passing the first data signals from the digital bus to the noise intolerant device (110), and passing the second data signals from the tuner module to the digital bus.

3. The television signal processing apparatus of claim 2, wherein the first and second transistors (Q1/Q3) are bipolar junction transistors.

4. The television signal processing apparatus of claim 1, wherein the digital bus (104/105) is an inter-integrated circuit bus.

5. The television signal processing apparatus of claim 1, wherein the tuner module (110) comprises a phase lock loop (121) for generating frequency variable tones.

6. The television signal processing apparatus of claim 5, wherein the frequency down-converter (123) is coupled to the phase lock loop (121) for mixing one of a plurality of television signals (120) with one of the frequency variable tones to generate an intermediate frequency television signal.

7. The television signal processing apparatus of claim 6, wherein the bi-directional buffer (109) operates in the second mode of operation in response to a channel change command that causes a tuning event to occur.

8. The television signal processing apparatus of claim 7, wherein the bi-directional buffer (109) operates in the second mode of operation for a predetermined period of time upon receipt of the channel change command, and then automatically reverts to the first mode of operation.

9. A method for isolating a tuner module (110) from a source of noise in a television signal receiver, comprising the steps of:

- sending clock signals and first data signals from a processor (101) to a digital bus (104/105);
- receiving the clock signal and the first data signals at the tuner module via the digital bus;
- sending second data signals from the tuner module to a bi-directional buffer (109) that selectively couples the tuner module to the digital bus; and
- receiving the second data signals at the processor (101) via the digital bus and the bi-directional buffer (109), wherein, in a first mode of operation the bi-directional buffer isolates the tuner module from the processor, and in a second mode of operation passes the clock signals and the first data signals from the digital bus to the noise intolerant device (111, 121), and also passes the second data signals from the tuner module to the digital bus.

10. The method of claim 9, wherein:

- the receiving the clock signal step comprises selectively passing the clock signals from the digital bus to the tuner module via a first transistor (Q1); and
- the receiving the second data signals step comprises selectively passing the first data signals from the digital bus to the tuner module, and the second data signals from the tuner module to the digital bus via a second transistor (Q3).

11. The method of claim 10, wherein the first and second transistors (Q1/Q3) are bipolar junction transistors.

12. The method of claim 9, wherein the tuner module comprises a phase lock loop (121) for generating frequency variable tones.

13. The method of claim 12, wherein the tuner module further comprises a frequency down-converter (123) coupled to the phase lock loop (121) for mixing one of a plurality of television signals (120) with one of the frequency variable tones to generate an intermediate frequency television signal.

14. The method of claim 13, further comprising the steps of:

- receiving a channel change command that initiates a tuning event, the bi-directional buffer operating in the second mode of operation to allow the processor to send tuning commands to the tuner module in response to the tuning event.

15. The method of claim 14, wherein the receiving a channel change step comprises the bi-directional buffer reverting to the first mode of operation thereby
isolating the tuner module from the processor after a predetermined time has elapsed after the tuning event is initiated.

16. The method of claim 9, wherein the clock signals, the first data signals and the second data signals are transmitted via an inter-integrated circuit bus.

Patentansprüche

1. Vorrichtung zur Fernsehsignalverarbeitung (100), die umfasst:

-einen digitalen Bus (104/105);
-eine Controllerschaltung einschließlich eines Prozessors (101), die mit dem digitalen Bus verbunden ist, zur Ausgabe von Taktsignalen und ersten Datensignalen und zum Empfang von zweiten Datensignalen über den digitalen Bus (104/105);
-eine Ausgangsschaltung einschließlich eines Tunerbausteins (110) mit einer rauschempfindlichen Schaltung (111,121), der an einen Abwärtskonverter (113,123) und eine Datenspeichereinheit (112) gekoppelt ist; und
einen bidirektionalen Puffer (109), der zwischen dem digitalen Bus (104/105) und dem Tunerbaustein (110) eingekoppelt ist, wobei der bidirektionale Puffer (109) in einer ersten Betriebsart den Tunerbaustein von dem Prozessor trennt und in einer zweiten Betriebsart die Taktsignale und die ersten Datensignale von dem Prozessor zum Tunerbaustein und ebenso die zweiten Datensignale vom Tunerbaustein zum Prozessor weiterleitet.

2. Vorrichtung zur Fernsehsignalverarbeitung nach Anspruch 1, wobei der bidirektionale Puffer (109) umfasst:

-einen ersten Transistor (Q1), um die Taktsignale von dem digitalen Bus (104/105) selektiv zu dem Tunerbaustein weiterzuleiten; und
einen zweiten Transistor (Q3), um die ersten Datensignale von dem digitalen Bus zu der rauschempfindlichen Schaltung (110) weiterzuleiten und um die zweiten Datensignale von dem Tunerbaustein zu dem digitalen Bus weiterzuleiten.

3. Vorrichtung zur Signalverarbeitung nach Anspruch 2, wobei der erste und zweite Transistor (Q1/Q3) bipolare Verbindungstransistoren sind.

4. Vorrichtung zur Fernsehsignalverarbeitung nach Anspruch 1, wobei der digitale Bus (104/105) ein \textit{I}^2\textit{C}-Bus ist.

5. Vorrichtung zur Fernsehsignalverarbeitung nach Anspruch 1, wobei der Tunerbaustein (110) eine Phasenregelschleife (121) zur Erzeugung verschiedener Einzelfrequenzen umfasst.

6. Vorrichtung zur Fernsehsignalverarbeitung nach Anspruch 5, wobei der Abwärtskonverter (123) an die Phasenregelschleife (121) gekoppelt ist, um eine aus der Mehrzahl der Fernsehsignale mit einer der veränderlichen Einzelfrequenzen zu mischen, zur Erzeugung eines Zwisehenfrequenz - Fernsehsignals.

7. Vorrichtung zur Fernsehsignalverarbeitung nach Anspruch 6, wobei der bidirektionale Puffer (109) als Antwort auf einen Kanalwechselbefehl, der den Abstimmvorgang auslöst, in der zweiten Betriebsart arbeitet.

8. Vorrichtung zur Fernsehsignalverarbeitung nach Anspruch 7, wobei der bidirektionale Puffer (109) für eine vorbestimmte Zeitspanne nach dem Empfang des Kanalwechselbefehls in der zweiten Betriebsart arbeitet, und dann automatisch in die erste Betriebsart zurückkehrt.

9. Verfahren, um einen Tunerbaustein (110) von einer Rauschquelle in einem Fernsehsignalempfänger abzuschirmen, das folgende Schritte umfasst:

Senden von Takt - und ersten Datensignalen von einem Prozessor (101) zu einem digitalen Bus (104/105);

10. Verfahren nach Anspruch 9, wobei:

der Schritt das Taktsignal zu empfangen, das selektive Weiterleiten der Taktsignale von dem digitalen Bus zu dem Tunerbaustein über einen ersten Transistor (Q1) umfasst; und
der Schritt, die zweiten Datensignale zu emp-
fangen das selektive Weiterleiten der ersten Datensignale von dem digitalen Bus zu dem Tunerbaustein, und der zweiten Datensignale von dem Tunerbaustein zu dem digitalen Bus über einen zweiten Transistor (Q3) umfasst.

11. Verfahren nach Anspruch 10, wobei der erste und der zweite Transistor (Q1/Q3) bipolare Transistoren sind.

12. Verfahren nach Anspruch 9, wobei der Tunerbaustein eine Phasenregelschleife (121) zur Erzeugung verschiedener Einzelfrequenzen umfasst.

13. Verfahren nach Anspruch 12, wobei der Tunerbaustein außerdem einen an die Phasenregelschleife gekoppelten Abwärts-Frequenzkonverter (123) zur Mischung eines aus der Mehrzahl der Fernsehsignale (120) mit einer Einzelfrequenz zur Erzeugung eines Zwischenfrequenz-Fernsehsignals umfasst.

14. Verfahren nach Anspruch 13, das außerdem folgende Schritte umfasst:

Empfang eines Kanalwechselbefehls, der den Abstimmvorgang auslöst, Arbeiten des bidirektionalen Puffers in der zweiten Betriebsart, um dem Prozessor zu erlauben, als Reaktion auf den Abstimmvorgang, Abstimmbefehle zu dem Tunerbaustein zu senden.

15. Verfahren nach Anspruch 14, wobei der Schritt einen Kanalwechsel zu empfangen, die Rückkehr des bidirektionalen Puffers in die erste Betriebsart umfasst, wodurch der Tunerbaustein von dem Prozessor getrennt wird, nachdem eine vorbestimmte Zeitspanne nach dem Auslösen des Abstimmereignisses verstrichen ist.

16. Verfahren nach Anspruch 9, wobei die Taktsignale, die ersten Datensignale und die zweiten Datensignale über einen IC-Bus übertragen werden.

Revidications

1. Un appareil de traitement de signaux de télévision (100), comprenant :

un bus numérique (104/105) ;
un contrôleur comprenant un processeur (101), couplé au bus numérique, émettant des signaux d’horloge et des premiers signaux de données et recevant des seconds signaux de données sur le bus numérique (104/105) ;
une partie avant comprenant un module syntoniseur (110) ayant un dispositif intolérant au bruit (111; 121) coupé à un convertisseur abaissieur (113, 123) et un dispositif de stockage des données (112) ; et
une mémoire tampon bi-directionnelle (109) couplée entre le bus numérique (104/105) et le module syntoniseur (110), où, dans un premier mode de fonctionnement, la mémoire tampon bi-directionnelle (109) isole le module syntoniseur du processeur, et dans un second mode d’opération, transmet les signaux d’horloge et les premiers signaux de données du processeur au module syntoniseur et transmet également les seconds signaux de données du module syntoniseur au processeur.

2. L’appareil de traitement de signaux de télévision de la revendication 1, où la mémoire tampon bi-directionnelle (109) comprend :

un premier transistor (Q1) pour transmettre de façon sélective les signaux d’horloge du bus numérique (104/105) au module syntoniseur ; et un second transistor (Q3) pour transmettre de façon sélective les premiers signaux de données du bus numérique au dispositif intolérant au bruit (110), et transmettre les seconds signaux de données du module syntoniseur au bus numérique.

3. L’appareil de traitement de signaux de télévision de la revendication 2, où le premier et le second transistor (Q1/Q3) sont des transistors à jonctions bipolaires.

4. L’appareil de traitement de signaux de télévision de la revendication 1, où le bus numérique (104/105) est un bus de circuit inter-intégré.

5. L’appareil de traitement de signaux de télévision de la revendication 1, où le module syntoniseur (110) comprend un boucle à verrouillage de phase (121) pour générer des impulsions variables de fréquence.

6. L’appareil de traitement de signaux de télévision de la revendication 5, où le convertisseur abaissieur de fréquence (123) est couplé à la boucle de verrouillage de phase (121) pour mélanger un des signaux de la pluralité de signaux de télévision (120) à une des impulsions variables de fréquence pour générer un signal de télévision à fréquence intermédiaire.

7. L’appareil de traitement de signaux de télévision de la revendication 6, où la mémoire tampon bi-directionnelle (109) fonctionne dans la second mode de fonctionnement en réponse à une commande de changement de canal provoquant un événement de syntonisation.

8. L’appareil de traitement de signaux de télévision de
la revendication 7, où la mémoire tampon bi-directionnelle (109) fonctionne dans le second mode de fonctionnement pour une période de temps prédéterminée à la réception de la commande de changement de canal, puis revient automatiquement au premier mode de fonctionnement.

9. Un procédé pour isoler un module syntoniseur (110) d'une source de bruit dans un récepteur de signaux de télévision, comprenant les étapes :

d'envoi de signaux d'horloge et de premiers signaux de données d'un processeur (101) à un bus numérique (104/105) ;
de réception du signal d'horloge et des premiers signaux de données sur le module syntoniseur via le bus numérique ;
d'envoi de seconds signaux de données du module syntoniseur à une mémoire tampon bi-directionnelle (109) qui couple de façon sélective le module syntoniseur au bus numérique ;
de réception des seconds signaux de données sur le processeur (101) via le bus numérique et la mémoire tampon bi-directionnelle (109), où, dans un premier mode de fonctionnement, la mémoire tampon isole le module syntoniseur du processeur, et dans un second mode de fonctionnement, transmet les signaux d'horloge et les premiers signaux de données du bus numérique au dispositif intolérant au bruit (111, 121), et transmet également les seconds signaux de données du module syntoniseur au bus numérique.

10. Le procédé de la revendication 9, où :

l'étape de réception du signal d'horloge comprend la transmission de façon sélective des signaux d'horloge du bus numérique au module syntoniseur via un premier transistor (Q1) ; et
l'étape de réception des seconds signaux de données comprend la transmission de façon sélective des premiers signaux de données du bus numérique au module syntoniseur, et des seconds signaux de données du module syntoniseur au bus numérique via un second transistor (Q3).

11. Le procédé de la revendication 10, où le premier et le second transistor (Q1/Q3) sont des transistors à jonctions bipolaires.

12. Le procédé de la revendication 9, où le module syntoniseur comprend une boucle de verrouillage de phase (121) pour générer des impulsions variables de fréquence.

13. Le procédé de la revendication 12, où le module syntoniseur comprend également un convertisseur abaissieur de fréquence (123) couplé à la boucle de verrouillage de phase (121) pour mélanger un signal de la pluralité de signaux de télévision (120) à une des impulsions variables de fréquence pour générer un signal de télévision à fréquence intermédiaire.

14. Le procédé de la revendication 13, comprenant en outre les étapes de :

réception d'une commande de changement de canal qui initie un événement de syntonisation, la mémoire tampon bi-directionnelle fonctionnant dans le second mode de fonctionnement pour permettre au processeur d'envoyer des commandes de syntonisation au module syntoniseur en réponse à l'événement de syntonisation.

15. Le procédé de la revendication 14, où l'étape de réception d'un changement de canal comprend le retour de la mémoire tampon bi-directionnelle au premier mode de fonctionnement isolant ainsi la module syntoniseur du processeur après qu'une période de temps prédéterminée s'est écoulée après que l'événement de syntonisation a été initié.

16. Le procédé de la revendication 9, où les signaux d'horloge, les premiers signaux de données et les seconds signaux de données sont transmis via un bus de circuit inter-intégré.
FIG. 2

USER INPUT TO SELECT SIGNAL

CONTROL BI-DIRECTIONAL BUFFER TO ALLOW SIGNAL PASSAGE

COUPLE SELECTED SIGNAL TO DOWN-CONVERTER

CAUSE PLL TO GENERATE FREQUENCY TONE

READ DATA FROM EEPROM

CONTROL RECEIVER BASED ON READ DATA

CONTROL BI-DIRECTIONAL BUFFER TO PROHIBIT SIGNAL PASSAGE

COMBINE SELECTED SIGNAL WITH FREQUENCY TONE TO GENERATE IF SIGNAL

PROCESS IF SIGNAL TO GENERATE VIDEO AND/OR AUDIO OUTPUT

FIG. 3