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(54) THE SEMICONDUCTOR LED DEVICE AND PRODUCING METHOD
HALBLEITER-LED-BAUELEMENT UND HERSTELLUNGSVERFAHREN
LE DISPOSITIF DE DIODE LECTROLUMINESCENTE SEMI-CONDUCTEUR ET PROC D DE PRODUCTION

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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device with gallium nitride type crystal passivation layer and a manufacturing method thereof which improves the effectiveness for blocking leakage current and thermal emission efficiency by using InGaN crystal body instead of the conventional dielectric passivation layer.

BACKGROUND ART

[0002] As shown in FIG. 1, a GaN type Light Emitting Diode (LED) generally comprises a buffer layer 11 on a sapphire substrate 10, an n-type GaN layer 12, an InGaN (or GaN) activation layer 13, a p-type GaN layer 14, a transparent electrode 15, a dielectric passivation layer 16, an n-type metal electrode 17 and a p-type metal electrode 18. The method of forming a GaN type Light Emitting Diode (LED) comprises the steps of successively crystal growing of the buffer layer 11 on the sapphire substrate 10, the n-type GaN layer 12, the InGaN (or GaN) active layer 13, and a p-type GaN layer 14 according to the Metal Organic Chemical Vapor Deposition (MOCVD) method; partly etching up to the n-type GaN layer 12 in order to form the n-type metal electrode 17; forming the transparent electrode 15; coating the surface with a dielectric passivation layer 16 except the electrode region: and depositing the n-type metal electrode 17 and the p-type metal electrode 18.

[0003] FIG. 2 is a cross-section diagram which illustrates the principle of leakage current occurrence for a GaN type optical semiconductor device in the absence of a dielectric passivation layer.

[0004] As shown in FIG. 2, the leakage current flows through the surfaces and boundaries when a voltage is applied to the electrode terminals and has significant effects on the performance of the device and sometimes causes destruction of the device.

[0005] For the case of GaN type semiconductor devices, boundaries for electrode deposition of a device are formed by Reactive Ion Etching (RIE). At this instance, the boundaries are damaged due to high energy ion bombardments and leakage current occurs along the damaged boundaries. Also, during the breaking or sawing of a device into individual chips after the completion of the process, too much stress exist on the cleavage boundary of the crystal growth layer and generally the boundaries become very rough due to the cleave not coinciding with the crystal faces. A large amount of leakage current flows along these rough boundaries.

[0006] Accordingly, at the conventional GaN type semiconductor, as shown in FIG. 1, the leakage current is prevented by coating the surface between the p-type metal electrode 18 and the n-type GaN layer 12 with the dielectric passivation layer 16.

[0007] The dielectric passivation layer 16 cuts off the passage of the leakage current that flows on the boundaries through the semiconductor surface and protects the surface of the device from external damages. This is an essential process in order to protect the device from surface damages and also secure the reliability of the device as well as improving the assembly yield. This process is also a final stage process which requires an extreme caution.

[0008] According to a construction method of the conventional dielectric passivation layer, a dielectric passivation layer such as SiO2 or Si3N4 is deposited using the PECVD or Sputtering process after forming a transparent electrode and the n-type & p-type metal electrodes. In this case, generally plasma is used for the deposition instead of a simple CVD method or thermal deposition method each of which has a weak adhesion strength between the dielectric passivation layer and the semiconductor surface. The plasma deposition method can improve the adhesion among the dielectric passivation layer, the metal surface (transparent electrode) and the semiconductor surface.

[0009] However, the deposition of a dielectric passivation layer under a plasma environment might cause damage on the performance of the device since RF power and DC bias, which are necessary for formation of plasma, are directly applied to the surface of the semiconductor. Sometimes this damage on the performance of the device might cause an eventual failure of the whole semiconductor process or a remarkable drop of the performance of the device.

[0010] Also, since the dielectric passivation layer deposition process is the final process of the device manufacturing, the total yield and performance of the devices can be significantly affected by a small process variable. If an optical semiconductor device is to be operated at a high output mode due to high voltage and high current, the light emission efficiency of the device is lowered due to the thermal resistance characteristic (very low thermal resistance) of the dielectric which reduces the amount of thermal emission generated by the InGaN activation layer 13.

[0011] Especially, in case of the junction-side down method which bonds a metal frame (or submount 19) with the upper face of the device for thermal emission as shown in FIG. 3, an inconsistent device, where the dielectric passivation layer 16 blocks is between the semiconductor device and metal frame 19, is constructed.

[0012] Also, the amount of leakage current on the p-n diode junction boundary is not negligible and this significantly affects the reliability of the device. It is difficult to sufficiently recognize the leakage current at the initial stage since it affects device yield after assembling and a long term reliability. Hence, it is required to fundamentally block the leakage current between a p metal electrode and n-GaN layer.
DETAILED DESCRIPTION OF THE INVENTION

[0013] The present invention is designed to overcome the above problems of prior art. The object of the invention is to provide a new structural semiconductor device and a manufacturing method therefor which effectively blocks the leakage current between the surface and boundary of the device and the pn-junction boundary, and enhances the light emission efficiency by removing the conventional dielectric passivation layer accompanying several problems and using an InxGal-xN crystal layer instead.

[0014] This object is achieved by the invention as defined in claim 1 and claim 5.

[0015] Namely, the GaN type optical semiconductor device with a pn junction diode structure comprising an n-type electrode, a transparent electrode and p-type electrodes according to the present invention is constructed first by sequentially forming a buffer layer on a substrate, an n-type GaN layer, an InGaN/GaN activation layer, a p-type GaN layer and an n-type InxGal-xN crystal layer, afterwards forming an n-type InxGal-xN (0 ≤ x ≤ 1) crystal passivation layer with a specified thickness (t) and width (w) only at the edge of the upper surface of the p-type GaN layer.

[0016] The n-type InxGal-xN (0 ≤ x ≤ 1) crystal passivation layer is grown with a thickness around 0.1 nm ≤ t < 5,000 nm. The value of n-doping concentration is 10^{15} \text{unit/cm}^3 < n < 10^{22} \text{unit/cm}^3 and the width is 0.1 \text{µm} < w < 300 \text{µm}.

[0017] The present invention constructed as explained so far is to provide a semiconductor device and manufacturing method therefor with gallium nitride (GaN) type crystal passivation layer having a new structural semiconductor in order to be used as a leakage current block and a device passivation layer. by using an InxGal-xN crystal body which is deposited at the initial crystal formation stage of the device instead of the conventional dielectric passivation layer which is deposited at the final process of the device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 is a cross section diagram which shows the structure of a conventional GaN type optical semiconductor device.

FIG. 2 is a cross-section diagram which illustrates the principle of leakage current occurrence for a GaN type optical semiconductor device.

FIG. 3 is a cross section diagram which shows a junction-side drawn type assembly structure for a high output operation of the conventional GaN type optical semiconductor device.

FIG. 4 is a cross section diagram which shows an embodiment of the construction of optical semiconductor device with an n-type InxGal-xN crystal passivation layer according to the present invention.

FIG. 5a and 5b are cross-section diagrams of the main parts which illustrate the principle of cutting off the leakage current and pinch-off phenomenon for the optical semiconductor device according to the present invention.

FIG. 6a to FIG. 6e are cross section diagrams which illustrate the manufacturing process of the optical semiconductor device with an n-type InxGal-xN crystal passivation layer according to the present invention.

FIG. 7 is a cross section diagram which shows the principle of the photo electrochemical etching method adopted by the present invention.

FIG. 8 is a cross section diagram which shows another embodiment of the construction of optical semiconductor device with an n-type InxGal-xN crystal passivation layer according to the present invention.

[Description of the numeric on the main parts of the drawings]

10, 40 : Substrate
11, 41 : Buffer Layer
12, 42 : n-type GaN Layer
13, 43 : InGaN (or GaN) Activation Layer
14, 44 : p-type GaN Layer
15, 46 : Transparent Electrode
16 : Dielectric Passivation Layer
17, 47 : n-type Metal Electrode
18, 48 : p-type Metal Electrode
45-a : n-type InxGal-xN Crystal Layer
45 : n-type InxGal-xN Crystal Passivation Layer

BEST MODE FOR CARRYING OUT THE INVENTION

[0020] In order to achieve the stated object, a semiconductor device which comprises the gallium nitride type crystal passivation layer according to the present invention having GaN type semiconductor device with a p-n junction diode structure comprises an InxGal-xN crystal layer which is at the upper most layer of the semiconductor device with a specified thickness and a width as a passivation layer on the top edge region of a p-GaN layer.

[0021] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0022] FIG. 4 shows an embodiment of the construc-
As shown in FIG. 4, the GaN type optical semiconductor device with a p-n junction diode structure comprising an n-type metal electrode 47, a transparent electrode 46 and a p-type metal electrode 48 according to the present invention is constructed first by sequentially forming a buffer layer 41 on a substrate 40, an n-type GaN layer 42, a lnGaN/GaN active layer 43, a p-type GaN layer 44 and an n-InxGaN-xN crystal layer 45. Afterwards forming an n-InxGaN-xN (0 ≤ x ≤ 1) crystal passivation layer 45 with a specified thickness (t) and width (w) only at the edge of the upper surface of the p-type GaN layer 44.

The n-type InxGaN-xN (0 ≤ x ≤ 1) crystal passivation layer 45 is grown with a thickness around 0.1 nm and is deposited at the initial crystal formation stage of the device instead of the conventional dielectric passivation layer 16 which is deposited at the final process of the device.

Hence, it is effective for cutting off the leakage current and is able to solve many problems that come with depositing a dielectric passivation layer at the final stage. FIG. 5a and 5b illustrate the principle of cutting off the leakage current for the optical semiconductor device according to the present invention.

As shown in FIG. 5a, if a voltage (+V) is applied, the device center region (region (I)), where the n-type InxGaN-xN passivation layer 45 is formed, becomes a p-n junction diode structure and operates normally, however, the edge of device surface region (region (II)), where the n-type InxGaN-xN passivation layer is formed, becomes an n-p-n junction diode structure with n-type InxGaN-xN/p-type GaN/n-type InxAuxxGaN and no current flows.

Also, as shown in FIG. 5b, if a voltage (+V) is applied to a part on the top n-type InxGaN-xN passivation layer, it takes a n-type InxGaN-xN/p-type GaN/n-type InxGaN/n-type GaN structure and becomes a reverse direction n-p-n junction. Also, a depletion region forms in the junction of the p-type GaN layer 44 due to the influence of n-type layers with high doping concentration at the top and the bottom and thus a pinch-off phenomenon occurs where no hole current flows in the horizontal direction of the p-type GaN layer 44 hence the leakage current in the horizontal direction can be completely blocked.

Also, since the interface section between the p-type GaN layer 44 and n-type InxGaN-xN passivation layer 45 has a complete crystal structure such as a single crystal, the leakage current can more completely be blocked in comparison to the conventional dielectric passivation layer deposition.

Especially, in comparison to the dielectric passivation layer 16, the n-type InxAuxxGaN-xN passivation layer 45 has a much better heat transfer characteristic and is a good quality crystal layer which is identical to the construction layer of the device, hence, the n-type InxGaN-xN passivation layer 45 is a very effective structure for thermal emission for the junction-side down type.

While, FIG. 6a to FIG. 6e are cross section diagrams which illustrate the manufacturing process of the optical semiconductor device with an n-type InxAuxxGaN-xN crystal passivation layer according to the present invention. As shown in FIG. 6a, the manufacturing method of the optical semiconductor device with an n-type InxAuxxGaN-xN crystal passivation layer according to the present invention comprises the steps of successively crystal growing of a buffer layer 41 on a substrate (sapphire, SiC, GaN, Si, etc) 40, an n-type GaN layer 42, an InGaN/GaN activation layer 43, a p-type GaN layer 44 and an n-type InxAuxxGaN-xN crystal layer 45 according to the Metal Organic Chemical Vapor Deposition (MOCVD) method.
by exposing the subjected etching part to a light with bigger energy value than the band gap of the n-type InxGa1-xN crystal layer 45-a and reacts with an electrolytic solution (KOH + H2O) in order to etch rapidly the hole generated part.

[0040] Also, according to the polarity of voltage applied to the electrolytic solution and the crystal layer, either n-type or p-type can be selectively etched.

[0041] Accordingly, by selecting the polarity of voltage and exposing the subjected etching part to a light, only the n-type In(x)Ga(1-x)N crystal layer 45-a can be selectively etched against the p-GaN layer 44 and the etched semiconductor surface can remain in very good state without any damage or stress.

[0042] Also, as shown in FIG. 6d, if necessary, the manufacturing process of the optical semiconductor device according to the present invention is completed by depositing a transparent electrode 46 or front face electrode on the upper section of the n-type InxGa1-xN passivation layer 45 and p-type GaN layer 44 and forming a metal electrode 47 and p-type metal electrode 48 as shown in FIG. 6e.

[0043] If necessary, the n-type In(x)Ga(1-x)N crystal layer 45-a on the p-type GaN layer 44 can form a passivation layer 45 as an insulator which does not conduct electricity by intentionally dropping the doping process or undergoing a slight p-type doping.

[0044] FIG. 8 is a cross section diagram which shows another embodiment of the construction of the optical semiconductor device with the n-type InacGal-xN crystal passivation layer according to the present invention.

[0045] As shown in FIG. 8, the optical semiconductor device can be constructed in the form where the p-type metal electrode 48 is not applied to the n-type InxGa1-xN passivation layer 45 by coating the transparent electrode 46 only on the p-type GaN layer 44.

[0046] It should be understood, however, that the detailed description and specific examples are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

INDUSTRIAL APPLICABILITY

[0047] According to the present invention constructed as explained so far, by forming an InxGa1-xN on the top surface edge region of a p-type GaN layer during crystal growing stage, leakage current from the surface edge region of a p-type GaN layer, hence the reliability and the yield of the devices can be improved very greatly.

[0048] Also, the InxGa1-xN passivation layer of the present invention has a very excellent thermal conductivity hence, to be operated at a high output mode the light emission efficiency and reliability of the device can be improved.

[0049] Also, due to n-type InxGa1-xN passivation layer of the present invention being formed at the initial crystal formation stage of the device, the conventional dielectric deposition process which is performed at the final process of the device is omitted, hence, the simplification of the process and the yield of the devices can be improved very greatly.

Claims

1. A semiconductor device with gallium nitride type crystal passivation layer, wherein the semiconductor device has a p-n junction diode construction and comprises an InxGa1-xN (0≤x<1) crystal layer (45) which is the top layer of the semiconductor device as a passivation layer with a specified thickness and a width at the edge of the upper surface of p-type GaN layer (44).

2. The semiconductor device as claimed in claim 1, wherein the InxGa1-xN crystal passivation layer (45) is grown with a thickness around 0.1 nm - 5,000 nm and a width around 0.1 μm - 300 μm and the value of n-doping concentration is 10^{15} - 10^{22} unit/cm^3.

3. The semiconductor device as claimed in claim 1, wherein the InxGa1-xN crystal passivation layer (45) is either not doped or slightly p-type doped.

4. The semiconductor device as claimed in claim 1, wherein an electrode face is not coated on the upper section of the InxGa1-xN crystal passivation layer (45).

5. A manufacturing method for a semiconductor device with a gallium nitride type crystal passivation layer and a p-n junction diode construction comprising the steps of:

   a) growing an InxGa1-xN (0≤x<1) crystal passivation layer (45-a) which is the top layer of the semiconductor device on the surface of a p-type GaN layer (44); and
   b) forming an InxGa1-xN crystal passivation layer (45) at the edge of the upper surface of p-type GaN layer (44) by removing the center section of the InxGa1-xN crystal layer (45) through an etching process.

6. The method as claimed in claim 5, wherein the InxGa1-xN crystal layer (45) is grown in a N2 gas environment according to the MOCVD crystal growing method.

7. The method as claimed in claim 5, wherein the InxGa1-xN crystal passivation layer (45) is formed by
4. Verfahren nach Anspruch 5, wobei die In$_x$Ga$_{1-x}$N-Kristallschicht (45) in einer N$_2$-Gaszusammensetzung gemäß einem MOCVD-Kristallwachstumsverfahren aufwächst.

7. Verfahren nach Anspruch 5, wobei die In$_x$Ga$_{1-x}$N-Passivierungskristallschicht (45) durch Wählen eines der folgenden Ätzverfahren gebildet wird: RIE-Ätzen, chemisches Ätzen oder elektrochemisches Ätzen.

Photoätzen.

Revendications

1. Composant semi-conducteur avec une couche de passivation en cristal de type nitreux de gallium, dans lequel le composant semi-conducteur possède une structure de diode à jonction p-n et comprend une couche de cristal In$_x$Ga$_{1-x}$N (0 ≤ x < 1) (45) qui est la couche supérieure du composant semi-conducteur à titre de couche de passivation avec une épaisseur spécifiée et une largeur spécifiée à la bordure de la surface supérieure de la couche de GaN de type p (44).

2. Composant semi-conducteur selon la revendication 1, dans lequel la couche de passivation en cristal In$_x$Ga$_{1-x}$N (45) est produite par croissance avec une épaisseur d’environ 0,1 nm à 5000 nm et une largeur d’environ 0,1 μm à 300 μm, et la valeur de la concentration du dopage n est de 10$^{15}$ - 10$^{22}$ unités/cm$^3$.

3. Composant semi-conducteur selon la revendication 1, dans lequel la couche de passivation en cristal In$_x$Ga$_{1-x}$N (45) est soit non dopée soit légèrement dopée de type p.

4. Composant semi-conducteur selon la revendication 1, dans lequel une face d’éléctrode n’est pas revêtue sur la section supérieure de la couche de passivation en cristal In$_x$Ga$_{1-x}$N (45).

5. Procédé de fabrication pour un composant semi-conducteur avec une couche de passivation en cristal de type nitreux de gallium et une structure de diode à jonction p-n, comprenant les étapes consistant à :

a) faire croître une couche de passivation en cristal In$_x$Ga$_{1-x}$N (45) qui est la couche supérieure du composant semi-conducteur sur la surface d’une couche GaN de type p (44) ; et
b) former une couche de passivation en cristal In$_x$Ga$_{1-x}$N (45) à la bordure de la surface supérieure de la couche de GaN de type p (44) en supprimant la portion centrale de la couche en cristal In$_x$Ga$_{1-x}$N (45) par un processus d’attaque chimique.
d'attaque parmi l'attaque RIE, l'attaque chimique, ou des procédés d'attaque photo-électrochimique.