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(54) Transmitter and radio communication terminal using the same
Sender und Funkkommunikationsendgerät damit
Emetteur et terminal de communication radio comportant un tel émetteur

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The present invention relates to a transmitter including a frequency synthesizer and a PLL frequency conversion circuit and to a wireless communication terminal apparatus using the same used in a wireless communication system such as the GSM, the DCS1800, or the like.

Generally, the following three types are considered as a configuration of a transmitter used in a wireless communication terminal apparatus. (1) An architecture for mixing a base band signal with a local signal having the same frequency as a transmission frequency in a modulator. (2) An architecture for, after temporarily upconverting a base band signal to an intermediate frequency in a modulator, upconverting it to a transmission frequency by using a mixer. (3) An architecture for, after temporarily upconverting a base band signal to an intermediate frequency in a modulator, converting it to a transmission frequency in a PLL frequency conversion circuit.

In the architecture (3), since only a constant envelope modulation can be handled as a modulation architecture, architectures (1) and (2) have been mainstream as the architecture of the transmitter. However, since the GSM and the DCS1800 system rapidly widespread in recent years employ the constant envelope modulation as the modulation architecture, the architecture (3) having various advantages has been started to widely use. The advantages of the architecture (3) include: (1) that an expensive filter having a high Q value is not required in the transmitter according to filter characteristics which the PLL has, (2) that, since a VCO output signal is a constant envelope signal, a bias design of a power amplifier at the next stage of the PLL frequency conversion circuit becomes easy, and the like.

Here, the present inventors have investigated the transmitter according to the aforementioned architecture (3). The following is not a well-known technique, but a technique investigated by the present inventors, an outline thereof will be described with reference to FIGS. 6 to 9. FIG. 6 shows a transmitter of the architecture (3) according to a comparative example which is an assumption of the present invention. This transmitter is configured with a first frequency synthesizer 38, a second frequency synthesizer 39, a crystal oscillator 40 for giving reference signals to the first and second frequency synthesizers, a PLL frequency conversion circuit 41, a divider 47, a modulator 54, and a base band circuit 42.

The first frequency synthesizer 38 is configured with a first counter 42, a second counter 43, a phase comparator 50, a low pass filter 51, and a VCO 52, where an output signal of the VCO 52 which is a frequency fRF is input into the divider 47. The second frequency synthesizer 39 is configured with a third counter 48, a fourth counter 49, a phase comparator 50, a low pass filter 51, and a VCO 52, where an output signal of the VCO 52 which is a frequency fRF is input into a mixer 53.

On the basis of information signals such as a sound, various data, and the like, the base band circuit 42 is a circuit for generating a waveform of a base band signal or generating various data for controlling this transmitter. Assuming a local signal output from the first frequency synthesizer 38 to be an input signal, the divider 47 divides this local signal into a frequency fIF, and inputs it into the modulator 54.

The modulator 54 mixes the signal of the frequency fIF supplied from the divider 47 into a base band signal from the base band circuit 42, and upconverts it to an intermediate frequency (for example, 270 MHz). The PLL frequency conversion circuit 41 is configured with a phase comparator 55, a low pass filter 56, an intermediate frequency (IF) VCO 57, and the mixer 53. Two signals are input into the phase comparator 55. A first input signal is an output signal of the modulator 54, and a second input signal is an output signal of the mixer 53. The output signal of the phase comparator 55 is output to the low pass filter 56, where undesired noises are eliminated, and is then input into the VCO 57. The output frequency of the VCO 57 is an IF VCO, which is used as an output signal of this transmitter and is input into the mixer 53. Two signals are input into the mixer 53. A first input signal is an output signal of the VCO 57, and a second input signal is a local signal of the frequency fRF supplied from the second frequency synthesizer 39. The output frequency of the mixer 53 is an absolute value of a difference between the two input frequencies, which becomes |fRF-fVCO|. The output signal of the mixer 53 becomes the second input signal of the phase comparator 55. Since, when the PLL frequency conversion circuit 41 is in a locked state, the two input frequencies of the phase comparator 55 are equal to each other, |fIF|=|fRF-fVCO| is obtained. Therefore, the output frequency IF VCO of the VCO 57 is given as |fRF-fIF|. In other words, the output frequency |fIF| of the modulator 54 is frequency converted to fVCO=|fRF-fIF| in the output of the transmitter. In order to change the output frequency of the transmitter, the output frequency fRF of the second frequency synthesizer 39 is changed while the output frequency of the first frequency synthesizer 38 remains fixed.

Next, an example of closed-loop characteristics of the PLL frequency conversion circuit 41 is shown in FIG. 7.
A flat portion of 0 dB is a bandpass. Since the frequency of the horizontal axis denotes an offset frequency from the output frequency fVCO, it is found that the PLL frequency conversion circuit 41 has bandpass filter characteristics around the output frequency. In other words, when the bandpass width is set to be wider than the bandwidth in the modulation architecture prescribed in the system such as the GSM or the like, the PLL frequency conversion circuit 41 can hold an output spectrum of the modulator 54, and convert the center frequency. Actually, in view of the phase difference and the noise level at the output of the PLL frequency conversion circuit 41, the bandpass width is designed to be about 1 to 2 MHz.

[0012] Needs for low cost, small capacity, and the like have been remarkably required for the wireless communication terminal apparatus, and an integration of a circuit structuring a terminal has been advanced year after year. However, a problem of a crosstalk of signals or harmonics between circuits has occurred along with an enhancement of the integration. Further, an improvement of a semiconductor process in recent years is being advanced in a direction of decreasing a parasitic capacitance, which also promotes the problem of the crosstalk between circuits. Further, a problem of the crosstalk through a mounting substrate has occurred due to a high density mounting such as an IC in a terminal.

[0013] FIG. 8 shows measurement results of the transmitter in which circuits surrounded by solid lines 58 and 59 in FIG. 6 are integrated in the same IC. The GSM is assumed as the system, and a GMSK modulation signal is used as the base band signal. The first frequency synthesizer 38 oscillates at 1080 MHz, is quadrant divided in the divider 47, where the fIF is assumed to be 270 MHz. Further, the IRF (fRF-fVCO) is set so that the fVCO becomes a GSM (including EGSM) transmission frequency (880 MHz to 915 MHz). The horizontal axis denotes the transmission frequency fVCO of the transmitter, and the vertical axis denotes a worst value of a difference between a signal level at the transmission frequency and a signal level at 400 MHz to 1.8 MHz offset and 6 MHz to 25 MHz offset from the transmission frequency by dB. A spectrum analyzer is used to measure the output of the VCO 57, and the measurement conditions thereof are RBW=VBW=30 kHz at 400 kHz to 1.8 MHz offset, and RBW=VBW=100 at 6 MHz to 25 MHz. The specifications with respect to spurious emissions of the GSM are not more than -60 dB and not more than -71 dB at 400 kHz to 1.8 MHz offset and at not less than 6 MHz offset, respectively. When the transmission frequency is in the vicinity of 900 MHz at 400 kHz to 1.8 MHz offset, it is found that, when the transmission frequency is in the vicinity of 898 MHz and in the vicinity of 902 MHz at 6 MHz to 25 MHz offset, the transmission spectrum is degraded, which does not meet the GSM specification. This is because undesired spurs occur in the offset frequency shown in formula 1 from the transmission frequency due to an intermodulation of harmonics of the fIF, the fRF and the fVCO.

\[ \pm |3 \times f_{\text{VCO}} - 10 \times f_{\text{IF}}| \quad \text{(Formula 1)} \]

Here, a relationship of fVCO=fRF-fIF is present between the fIF, the fRF and the fVCO. The undesired spurs occur as the result that the circuits surrounded by the solid lines 58 and 59 in FIG. 6 are integrated in the same IC so that influences due to the harmonics of the output signals of the first frequency synthesizer 38 and the second frequency synthesizer 39 are increased. Even when the circuits surrounded by the solid lines 58 and 59 are integrated in another IC, there is a possibility that the undesired spurs occur depending on the characteristics of the integrated IC, a semiconductor process to be used, or a method for mounting on a substrate.

[0014] Next, FIG. 9 shows an output spectrum of the transmitter in which the circuits surrounded by the solid lines 58 and 59 and the VCO 46 in FIG. 6 are integrated in the same IC. The GSM is assumed as the system, and the GMSK modulation signal is used as the base band signal. The first frequency synthesizer 38 oscillates at 1080 MHz, and is quadrant divided in the divider 47, where the fIF is assumed to be 270 MHz. The IRF is set at 1150 MHz so that the fVCO becomes 880 MHz. Further, the output frequency of the crystal oscillator 40 is 13 MHz. The horizontal axis denotes a frequency, and the vertical axis denotes a signal level by dBm. The measurement is performed by the spectrum analyzer, and the measurement condition is RBW=VBW=30 kHz. The undesired spurs occur at 1 MHz offset from the transmission frequency, and the level thereof is -58.2 dB. As described above, in the GSM specification, the level is prescribed to be not more than -60 dB at 400 kHz to 1.8 MHz offset, and the measurement result in FIG. 9 does not meet the GSM specification. The occurrence process of the undesired spurs is as follows. Harmonics of 1079 MHz which is 83 times the output signal of the crystal oscillator 40 occur in the first frequency synthesizer 38 or the second frequency synthesizer 39. This 1079 MHz signal is mixed into the VCO 46 due to the crosstalk. When the VCO is regarded as a positive feedback circuit, this 1079 MHz signal is amplified in the VCO 46, and at the same time, the undesired spurs also occur at 1081 MHz due to a folded operation around the oscillation frequency 1080 MHz by odd-order nonlinearity characteristics of the amplifier. Details of the folded operation of the noises in the VCO are described in chapter 7.4.3 in Prentice Hall PTR Prentice-Hall, Inc. Press, Behzad Razavi, "RF MICROELECTRONICS" (ISBN0-13-887571-5).

[0015] As a result that the present inventors have investigated the transmitter according to the comparative example which is the assumption of the present invention, the followings have become apparent. The transmitter according to
the aforementioned comparative example has the problems of the undesired spurs described later due to a progress of the integration of a circuit, a deterioration of the parasitic capacitance due to the improvement of the semiconductor process, or the high density mounting of a terminal.

[0016] A first problem (1) is in that the undesired spurs occur at a specific transmission frequency due to the harmonics of the output signal of the frequency synthesizer.

[0017] A second problem (2) is in that, when the harmonics of the output signal of the crystal oscillator are present in the vicinity of the oscillation frequency of the VCO, the undesired spurs occur in the VCO output due to the folded operation of the VCO.

[0018] Further, since it is difficult to predict the crosstalk between circuits or the crosstalk through a mounting substrate on designing the circuit of the mounting substrate so that it is required that improvements are added after actual manufacture and measurement have been performed, and a large amount of labor and cost has been required.

[0019] EP-A-0964523 discloses a transmitter in which a modulator receives an input signal from a frequency synthesiser formed by a VCO, which is controlled by a phase comparator. The modulator generates a signal which is fed to a second phase comparator which also receive an input from another frequency source.

DISCLOSURE OF THE INVENTION

[0020] According to the present invention there is provided a transmitter comprising:

- a first frequency synthesizer;
- a second frequency synthesizer;
- a base band circuit for outputting a base band signal and a control signal on the basis of an information signal;
- a control circuit for changing output frequencies of the first frequency synthesizer and the second frequency synthesizer on the basis of the control signal;
- a divider for dividing an output signal from the first frequency synthesizer;
- a modulator for assuming an output signal from the first frequency synthesizer to be a carrier signal and modulating the carrier signal on the basis of the base band signal;
- a frequency conversion circuit for using an output signal from the modulator and an output signal from the second frequency synthesizer to upconvert a carrier frequency of the output signal from the modulator; and
- an output for providing an output signal of the transmitter at an output frequency (fVCO),

wherein:

- the frequency conversion circuit comprises a first phase comparator, a first low pass filter, a first VCO and a mixer, and the frequency conversion circuit is a PLL frequency conversion circuit in which the first phase comparator is adapted to output a signal proportional to a phase difference between an output signal from the modulator and an output signal from the mixer;
- the first low pass filter is connected to an output of the first phase comparator;
- the first VCO is connected to an output of the first low pass filter and is adapted to provide the output frequency (fVCO);
- the mixer is adapted to mix a further output signal from the first VCO and an output signal from the second frequency synthesizer;
- the first frequency synthesizer comprises a first counter; a second counter; a second phase comparator; a second low pass filter and a second VCO, in which the second phase comparator is arranged to output a signal proportional to a phase difference between an output signal from the first counter and an output signal from the second counter;
- the first counter is connected to an output of a reference oscillator; the second counter is connected to an output of the second VCO; the second low pass filter is connected to an output of the second phase comparator; the second VCO is connected to an output of the second low pass filter, and a frequency divide ratio of the second counter is changeable by first frequency divide ratio data transmitted from the control circuit
- the second frequency synthesizer comprises a third counter; a fourth counter; a third phase comparator, a third low pass filter and a third VCO, the third phase comparator being arranged to output a signal proportional to a phase difference between an output signal from the third counter and an output signal from the fourth counter, the third counter is connected to an output of the reference oscillator, the fourth counter is connected to an output of the third VCO; the third low pass filter is connected to an output of the third phase comparator, the third VCO is connected to an output of the third low pass filter, and a frequency divide ratio of the fourth counter is changeable by second frequency divide ratio data transmitted from the control circuit,
- the base band circuit stores a relationship between the output frequency of the transmitter and output frequencies of the first frequency synthesizer and the second frequency synthesizer, and is arranged to generate the control signal corresponding to the output frequency of the frequency conversion circuits on the basis of the relationship, and the control circuit stores at least first and second predetermined first frequency divide ratio data and is adapted to select for a given output frequency (fVCO) of the transmitter that one of the at least first and second predetermined
first frequency divide ratio data, for which undesired spurs due to harmonics of the output signal of the frequency conversion circuit are farther offset from the output frequency (fVCO) of the transmitter.

[0021] The present invention may thus solve the problem of the undesired spurs due to the harmonics of the output signal of the frequency synthesizer occurring in the transmitter according to the aforementioned comparative example, and facilitates the design of a circuit or a mounting substrate.

[0022] Preferably the control circuit comprises a first register for holding the first predetermined first frequency divide ratio data; a second register for holding the second predetermined first frequency divide ratio data; a third register for holding the second frequency divide ratio data; and a selector for selecting one of the first and second predetermined first frequency divide ratio data on the basis of information included in the control signal.

[0023] It is desirable that at least the first counter, the second counter, the second phase comparator, the third counter, the fourth counter, the third phase comparator, and the second VCO are formed in the same IC.

[0024] Moreover, it is possible that the present invention may be incorporated in a wireless communication terminal apparatus

[0025] Further, the present invention may also solve the problem of undesired spurs occurring when the harmonics of the output signal of the crystal oscillator are mixed into the VCO, and to facilitate to design a circuit or a mounting substrate.

[0026] According to the present invention, even when the undesired spurs occur in the output of the transmitter including the frequency synthesizer and the PLL frequency conversion circuit due to the crosstalk between circuits or the crosstalk on the substrate which is difficult to predict at the design, the output frequency of the frequency synthesizer is appropriately changed according to the output frequency of the PLL frequency conversion circuit so that the undesired spurs can be suppressed. Thereby, an effect can be obtained in which time and cost for redesigning the circuit or the substrate can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027]

FIG. 1 is a functional block diagram showing an embodiment of a transmitter according to the present invention;
FIG. 2 is a characteristic diagram showing effects of the embodiment of the transmitter according to the present invention;
FIG. 3 is a functional block diagram showing another embodiment of the transmitter according to the present invention;
FIG. 4 is a characteristic diagram showing effects of another embodiment of the transmitter according to the present invention;
FIG. 5 is a functional block diagram showing an example of a wireless communication terminal apparatus using the transmitter according to the present invention;
FIG. 6 is a functional block diagram showing a transmitter according to a comparative example which is an assumption of the present invention;
FIG. 7 is a characteristic diagram showing closed-loop characteristics of a PLL frequency conversion circuit; and
FIGS. 8 and 9 are characteristic diagrams showing measurement results of the transmitter according to the comparative example.

BEST MODE FOR CARRYING OUT THE INVENTION

[0028] Hereinafter, embodiments according to the present invention will be described in detail with reference to the drawings. Throughout the drawings for describing the embodiments, like numerals are denoted to like parts, and repeated descriptions thereof will be omitted.

[0029] FIG. 1 is a configuration diagram showing a first embodiment of a transmitter according to the present invention, which solves the first object (1).

[0030] The transmitter according to the present invention is configured with a first frequency synthesizer 1, a second frequency synthesizer 2, a crystal oscillator 3 for giving reference signals to the first and second frequency synthesizers 1 and 2, a control circuit 4 for the first and second frequency synthesizers 1 and 2, a PLL frequency conversion circuit 5, a divider 12, a modulator 18, and a base band circuit 6.

[0031] The first frequency synthesizer 1 is configured with a first counter 7, a second counter 8, a phase comparator 9, a low pass filter 10, and a VCO 11, where an output signal of the VCO 11 is input into the divider 12.

[0032] The second frequency synthesizer 2 is configured with a third counter 12, a fourth counter 13, a phase comparator 14, a low pass filter 15, and a VCO 16, where an output signal of the VCO 16 which is a frequency IRF is input into a mixer 17.
On the basis of information signals such as a sound, various data, and the like, the base band circuit 6 is a circuit for generating a waveform of a base band signal or generating various data for controlling the transmitter.

The control circuit 4 is configured with a first register 22, a second register 23, a third register 24, a fourth register 25, a decoder 26, and a selector 27. A clock signal CLK and a data signal DATA are input into the first register 22 from the base band circuit 6, where this DATA is synchronized with this CLK and is stored as serial data. Part of the stored data (for example, higher 3 bits) is input into the decoder 26, and the remaining thereof is input into the second, third and fourth registers 23, 24, and 25. Data from the first register 22 is stored only in one register selected from among the second, third, and fourth registers 23, 24, and 25 by the output signal of the decoder 26. A timing with which the data is stored is determined by a trigger signal (for example, a fall edge) transmitted to the LE. The outputs of the second and third registers 23 and 24 are input into the selector 27. The selector 27 inputs either one of the outputs from the second and third registers 23 and 24 into the counter 8 according to selector data 28 from the fourth register 25. Part of the data (for example, higher 1 bit) stored in the fourth register 25 is output to the selector 27, and the remaining thereof is input into the counter 13 of the second frequency synthesizer 2.

Assuming a local signal output from the first frequency synthesizer 1 to be an input signal, the divider 12 divides this local signal into a frequency fIF, and inputs it into the modulator 18. The modulator 18 mixes a signal of the frequency fIF supplied from the divider 12 into the base band signal from the base band circuit 6, and upconverts it to an intermediate frequency (for example, 270 MHz).

The PLL frequency conversion circuit 5 is configured with a phase comparator 19, a low pass filter 20, a VCO 21, and a mixer 17. Two signals are input into the phase comparator 19. A first input signal is an output signal of the modulator 18, and a second input signal is an output signal of the mixer 17. In the phase comparator 19, the first and second input signals are phase-compared with each other, and a signal proportional to a phase difference is output. The output signal of the phase comparator 19 is output to the low pass filter 20, where undesired noises are eliminated, and is input into the VCO 21. An output frequency of the VCO 21 is an fVCO, which is used as an output signal of this transmitter and is input into the mixer 17. Two signals are input into the mixer 17. A first input signal is an output signal of the VCO 21, and a second input signal is a signal of the frequency fRF supplied from the second frequency synthesizer 2. The output frequency of the mixer 17 is an absolute value of a difference between the two input frequencies, which is |fRF-fVCO|. The output signal of the mixer 17 becomes the second input signal of the phase comparator 19. A frequency conversion operation and an operation as a band-pass filter of the PLL frequency conversion circuit 5 are similar to a PLL frequency conversion circuit shown in a comparative example which is an assumption of the present invention.

In the transmitter according to the present invention, circuits surrounded by a solid line 29 in FIG. 1 are incorporated in a single IC.

Next, an operation of the transmitter in FIG. 1 will be described.

At first, at an initial operation of this transmitter (for example, when a power supply is turned from OFF to ON), the data is stored in the second register 23, and the data is next stored in the third register 24. For example, the data of the counter 8 where the fIF becomes 270 MHz is stored in the second register 23, and the data of the counter 8 where the fIF becomes 272 MHz is stored in the third register 24. Once the data are stored in the second and third registers 23 and 24, updating of the data will not be performed thereafter. When the output frequency fVCO of this transmitter is updated, the data is input into the fourth register 25 and the data of the counter 13 is updated in each case so that the output frequency fRF of the second frequency synthesizer 2 is updated, and, at the same time, the selector data 28 is given to the selector 27 so that a value of the second or third register 23 or 24 is input into the counter 8 and the output frequency of the first frequency synthesizer 1 is updated.

Next, a description will be given to that a problem of undesired spurs due to harmonics of the output signal of the frequency synthesizer shown in the comparative example which is the assumption of the present invention can be solved by the transmitter in FIG. 1.

In the comparative example, the undesired spurs have occurred with an offset frequency prescribed by formula 1. For example, when fIf=270 MHz, fRF=1168 MHz, and fVCO=898 MHz are assumed, the undesired spurs occur with \pm 6 MHz offset. As described in the description of the comparative example, since the PLL frequency conversion circuit 5 has band-pass filter characteristics with a transmission frequency as a center frequency, a level of the undesired spurs can be suppressed by increasing the offset frequency of the undesired spurs. For example, when the fIF and the fRF are assumed to be 272 MHz and 1170 MHz, respectively with the fVCO remained at 898 MHz, the offset frequency of the undesired spurs becomes \pm 26 MHz offset from formula 1. In FIG. 2, the measurement results of the transmitter when 270 MHz and 272 MHz are used as fIF are shown. Since quadrant dividing is performed in the divider 12, the first frequency synthesizer 1 oscillates at 1080 MHz when fIF=270 MHz is assumed, and oscillates at 1088 MHz when fIF=272 MHz is assumed. Other measurement conditions are similar to the measurement conditions in the comparative example in FIG. 8. The undesired spurs occur in the vicinity of fVCO=900 MHz when fIF=270 MHz is assumed so that the GSM specification cannot be met, however, since the fVCO where the undesired spurs occur is shifted when fIF=272 MHz is assumed, it is found that the undesired spurs are suppressed in the vicinity of fVCO=900 MHz so that the GSM specification can be met. Therefore, for example, when the data of the counter 8 where the fIF becomes 270 MHz is stored in the
FIG. 3 is a configuration diagram showing a second embodiment of the transmitter according to the present invention, which simultaneously solves the first problem (1) and the second problem (2).

The present embodiment is a transmitter characterized in that the VCO 11 is added to an IC circuit (portion surrounded by a solid line (31) and further a fifth register 30 is added between the first register 22 and the selector 27 in FIG. 1. Circuits surrounded by a solid line 31 are incorporated in a single IC.

In the aforementioned comparative example, since the harmonics 1079 MHz of the output signal of the crystal oscillator is mixed in the vicinity of the oscillation frequency 1080 MHz of the VCO, the undesired spurs have occurred in this VCO output. Generally, the VCO employed in the wireless communication has a resonator, and the resonator has bandpass filter characteristics. Therefore, the oscillation frequency of this VCO is made far from 1079 MHz so that the level of the undesired spurs can be suppressed. FIG. 4 shows an output spectrum of the transmitter when the oscillation frequency of the VCO 11 is assumed to be 1088 MHz, that is, fIF=272 MHz, and fVCO=880 MHz is assumed in the same measurement conditions as the comparative example in FIG. 9. The undesired spurs are suppressed as compared with the comparative example, the level thereof is -66.4 dB. This value meets not more than -60 dB of the GSM specification.

According to the above results, the transmitter according to the present embodiment will be used as follows.

At the initial operation of this transmitter (for example, the power supply is turned from OFF to ON), the data of the counter 8 where the fIF becomes 272 MHz is stored in the second register 23, the data of the counter 8 where the fIF becomes 268 MHz is stored in the fifth register 30. Once the data are stored in the second, third, and fifth registers 23, 24, and 30, the updating of the data will not be performed thereafter. Since the GSM system is the TDMA (Time Division Multiple Access) architecture, transmission and reception cannot occur at the same time. Therefore, on the transmission, the selector 27 is appropriately switched according to the transmission frequency fVCO, and the data of this third or fifth register 24 or 30 is input into the counter 8. On the reception, the second register 23 is selected by the selector 27, and the data thereof is input into the counter 8.

Next, an embodiment of a wireless communication terminal apparatus using the transmitter according to the present invention will be described.

FIG. 5 is a diagram showing the embodiment of the wireless communication terminal apparatus using the transmitter according to the present invention.

The wireless communication terminal apparatus according to the present invention is configured with the base band circuit 6, a transmitting circuit 33, a power amplifier 34, an antenna switch 35, an antenna 36, a receiving circuit 37, and the crystal oscillator 3.

The transmitting circuit 33 is configured with the first frequency synthesizer 1, the second frequency synthesizer 2, the PLL frequency conversion circuit 5, the divider 12, the modulator 18, and the control circuit 4 in FIG. 1, where the circuits surrounded by the solid line 29 are incorporated in a single IC. Alternatively, the transmitting circuit 33 is configured with the first frequency synthesizer 1, the second frequency synthesizer 2, the PLL frequency conversion circuit 5, the divider 12, the modulator 18, and the control circuit 4 in FIG. 3, where the circuits surrounded by the solid line 31 are incorporated in a single IC.

The clock signal CLK, the data signal DATA, the trigger signal LE, and a base band signal 32 are input from the base band circuit 6 into the transmitting circuit 3.

The output signal from the crystal oscillator 3 is input into the transmitting circuit 33 and used as reference signals for the first frequency synthesizer 1 and the second frequency synthesizer 2 both provided in the transmitting circuit 33.

There are three signals output from the transmitting circuit 33. A first output signal is an output signal from the PLL frequency conversion circuit 5, and the frequency thereof is the fVCO. A second output signal is an output signal from the divider 12, and the frequency thereof is the fIF. A third output signal is an output signal from the second frequency

FIG. 6 is a diagram showing the embodiment of the wireless communication terminal apparatus using the transmitter according to the present invention.

The transmitting circuit 33 is configured with the first frequency synthesizer 1, the second frequency synthesizer 2, the PLL frequency conversion circuit 5, the divider 12, the modulator 18, and the control circuit 4 in FIG. 2, where the circuits surrounded by the solid line 37 are incorporated in a single IC. Alternatively, the transmitting circuit 33 is configured with the first frequency synthesizer 1, the second frequency synthesizer 2, the PLL frequency conversion circuit 5, the divider 12, the modulator 18, and the control circuit 4 in FIG. 3, where the circuits surrounded by the solid line 31 are incorporated in a single IC.

The output signal from the crystal oscillator 3 is input into the transmitting circuit 33 and used as reference signals for the first frequency synthesizer 1 and the second frequency synthesizer 2 both provided in the transmitting circuit 33.

There are three signals output from the transmitting circuit 33. A first output signal is an output signal from the PLL frequency conversion circuit 5, and the frequency thereof is the fVCO. A second output signal is an output signal from the divider 12, and the frequency thereof is the fIF. A third output signal is an output signal from the second frequency
synthesizer 2, and the frequency thereof is the fRF. The first output signal from the transmitting circuit 33 is input into
the power amplifier 34, where the power is amplified. The output signal from the power amplifier 34 is input into the
antenna switch 35. The antenna 36, an output of the transmitting circuit 33, and an input of the receiving circuit 37 are
connected to the antenna switch 35. In this wireless communication terminal apparatus, the antenna 36 and the output
of the transmitting circuit 33 are electrically connected on the transmission, and the antenna 36 and the input of the
receiving circuit 37 are electrically connected on the reception. In addition, a duplexer may be employed in place of the
antenna switch 35.

[0056] A receiving signal received in the antenna 36 is input into the receiving circuit 37 through the antenna switch
35. The receiving circuit 37 uses the second and third output signals of the transmitting circuit 33 to downconvert this
receiving signal up to the frequency which can be processed in the base band circuit 6 and to input it into the base band
circuit 6. The circuits structuring the receiving circuit 37 may be manufactured in another IC from the IC structuring the
transmitting circuit 33, further at least one circuit structuring the receiving circuit 37 may be incorporated in this IC.

[0057] Hereinbefore, the invention made by the present inventor is specifically described on the basis of the embod-
iments, but it goes without saying that the present invention is not limited to the above embodiments and various
modifications can be made without departing from the scope thereof.

INDUSTRIAL APPLICABILITY

[0058] As described above, the transmitter according to the present invention is useful for a transmitter including a
frequency synthesizer and a PLL frequency conversion circuit, and can be widely used in a wireless communication
terminal apparatus using this transmitter, and the like, used in a wireless communication system such as the GSM, the
DCS1800, or the like.

Claims

1. A transmitter comprising:

   a first frequency synthesizer (1);
   a second frequency synthesizer (2);
   a base band circuit (6) for outputting a base band signal and a control signal on the basis of an information signal;
   a control circuit (4) for changing output frequencies of the first frequency synthesizer (1) and the second frequency
   synthesizer (2) on the basis of the control signal;
   a divider (12) for dividing an output signal from the first frequency synthesizer (1);
   a modulator (18) for assuming an output signal from the first frequency synthesizer (1) to be a carrier signal
   and modulating the carrier signal on the basis of the base band signal;
   a frequency conversion circuit (5) for using an output signal from the modulator (18) and an output signal from
   the second frequency synthesizer (2) to upconvert a carrier frequency of the output signal from the modulator
   (18);

   an output for providing an output signal of the transmitter at an output frequency (fVCO),

   wherein

   the frequency conversion circuit (5) comprises a first phase comparator (19), a first low pass filter (20), a first
VCO (21) and a mixer (17), and the frequency conversion circuit (5) is a PLL frequency conversion circuit in
which the first phase comparator (19) is adapted to output a signal proportional to a phase difference between
an output signal from the modulator (18) and an output signal from the mixer (17);

   the first low pass filter (20) is connected to an output of the first phase comparator (19);

   the first VCO (21) is connected to an output of the first low pass filter (20) and is adapted to provide the output
frequency (fVCO);

   the mixer (17) is connected to an output of the first low pass filter (20) and the mixer (17) is adapted to provide the output
frequency (fVCO);

   the first frequency synthesizer (1) comprises a first counter (7), a second counter (8), a second phase comparator
(9), a second low pass filter (10) and a second VCO (11), and in which the second phase comparator (9) is arranged
to output a signal proportional to a phase difference between an output signal from the first counter (7) and an
output signal from the second counter (8), the first counter (7) is connected to an output of a reference oscillator
(3), the second counter (8) is connected to an output of the second VCO (11), the second low pass filter (10)
is connected to an output of the second phase comparator (9), the second VCO (11) is connected to an output
of the second low pass filter (10), and a frequency divide ratio of the second counter (8) is changeable by first
frequency divide ratio data transmitted from the control circuit (4)
the second frequency synthesizer (2) comprises a third counter (12), a fourth counter (13), a third phase comparator (14), a third low pass filter (15) and a third VCO (16), the third phase comparator (14) being arranged to output a signal proportional to a phase difference between an output signal from the third counter (12) and an output signal from the fourth counter (13), the third counter (12) is connected to an output of the reference oscillator (3), the fourth counter (13) is connected to an output of the third VCO (16), the third low pass filter (15) is connected to an output of the third phase comparator (14), the third VCO (16) is connected to an output of the third low pass filter (15), and a frequency divide ratio of the fourth counter (13) is changeable by second frequency divide ratio data transmitted from the control circuit (4),

the base band circuit (6) stores a relationship between the output frequency of the transmitter and output frequencies of the first frequency synthesizer (1) and the second frequency synthesizer (2), and is arranged to generate the control signal corresponding to the output frequency of the frequency conversion circuits (1, 2) on the basis of the relationship, and

the control circuit (4) stores at least first and second predetermined first frequency divide ratio data and is adapted to select for a given output frequency (fVCO) of the transmitter that one of the at least first and second predetermined first frequency divide ratio data, for which undesired spurs due to harmonics of the output signal of the frequency conversion circuit are farther offset from the output frequency (FVCO) of the transmitter.

2. The transmitter according to claim 1, wherein the control circuit (4) comprises a first register (23) for holding the first predetermined first frequency divide ratio data; a second register (24) for holding the second predetermined first frequency divide ratio data; a third register (25) for holding the second frequency divide ratio data; and a selector (27) for selecting one of the first and second predetermined first frequency divide ratio data on the basis of information included in the control signal.

3. The transmitter according to claim 2, wherein the first counter (7), the second counter (8), the second phase comparator (9), the third counter (12), the fourth counter (13), the third phase comparator (14), the modulator (18), the divider (12), the first phase comparator (19), the mixer (17), and the control circuit (4) are formed in the same IC.

4. The transmitter according to claim 1, wherein the control circuit (4) comprises a first register (23) for holding the first predetermined first frequency divide ratio data; a second register (24) for holding the second predetermined first frequency divide ratio data; a third register (30) for holding third predetermined first frequency divide ratio data; a fourth register (25) for holding the second frequency divide ratio data; and a selector (27) for selecting one of the first, second or third predetermined first frequency divide ratio data on the basis of information included in the control signal.

5. The transmitter according to claim 4, wherein at least the first counter (7), the second counter (8), the second phase comparator (9), the third counter (12), the fourth counter (13), the third phase comparator (14), and the second VCO (11) are formed in the same IC.

6. The transmitter according to claim 5, wherein the modulator (18), the divider (12), the first phase comparator (19), the mixer (17), and the control circuit (4) are further formed in the same IC.

7. A wireless communication terminal apparatus comprising a transmitting circuit (33) connected to an output of a receiving circuit (37); to which a first output signal and a second signal from the transmitting circuit (33) are input; a power amplifier (34) to which a third output signal from the transmitting circuit (33) is input; an antenna switch (35) connected to an input of the receiving circuit (37) and to an output of the power amplifier (34); and an antenna (36) connected to the antenna switch (35), wherein:

the transmitting circuit is the transmitter according to any one of claims 1 to 6, the first output signal and the second output signal are an output signal from the second frequency synthesizer (2) and an input signal to the modulator (18) of the transmitting circuit, respectively, the third output signal is an output signal from the first VCO (21) of the transmitting circuit, and an output signal from the receiving circuit (37) is input into the base band circuit (6) of the transmitting circuit, where an information signal is output.

8. The wireless communication terminal apparatus according to claim 7, wherein a duplexer is used in place of the antenna switch.
Patentansprüche

1. Sender, umfassend:
   einen ersten Frequenzsynthesizer (1);
   einen zweiten Frequenzsynthesizer (2);
   eine Basisbandschaltung (6) zur Ausgabe eines Basisbandsignals und eines Steuersignals basierend auf einem Informationssignal;
   eine Steuerschaltung (4) zur Änderung der Ausgangsfrequenzen des ersten Frequenzsynthesizers (1) und des zweiten Frequenzsynthesizers (2) basierend auf dem Steuersignal;
   einen Teiler (12) zum Teilen eines Ausgangssignals des ersten Frequenzsynthesizers (1);
   einen Modulator (18), um ein Ausgangssignal des ersten Frequenzsynthesizers (1) als Trägersignal anzunehmen und das Trägersignal basierend auf dem Basisbandsignal zu modulieren;
   eine Frequenzwandlungsschaltung (5), um ein Ausgangssignal des Modulators (18) und ein Ausgangssignal des zweiten Frequenzsynthesizers (2) zu verwenden, um eine Trägerfrequenz des Ausgangssignals des Modulators (18) aufwärtszuwandeln; und
   einen Ausgang zur Bereitstellung eines Ausgangssignals des Senders mit einer Ausgangsfrequenz (fVCO), wobei die Frequenzwandlungsschaltung (5) einen ersten Phasenkomparator (19), einen ersten Tiefpassfilter (20), einen ersten VCO (21) und einen Mischer (17) umfasst und die Frequenzwandlungsschaltung (5) eine PLL-Frequenzwandlungsschaltung ist, in der der erste Phasenkomparator (19) ausgebildet ist, um ein Signal auszugeben, das proportional zu einer Phasendifferenz zwischen einem Ausgangssignal des Modulators (18) und einem Ausgangssignal des Mischers (17) ist;
   wobei der erste Phasenkomparator (19) mit einem Ausgang des ersten Phasenkomparators (19) verbunden ist;
   wobei der erste VCO (21) mit einem Ausgang des ersten Tiefpassfilters (20) verbunden ist und ausgebildet ist, um die Ausgangsfrequenz (fVCO) bereitzustellen;
   wobei der Mischer (17) ausgebildet ist, um ein weiteres Ausgangssignal des ersten VCO (21) und ein Ausgangssignal des zweiten Phasenfreisynthesizers (2) zu mischen;
   wobei der erste Frequenzsynthesizer (1) einen ersten Zähler (7), einen zweiten Zähler (8), einen zweiten Phasenkomparator (9), einen zweiten Tiefpassfilter (10) und einen zweiten VCO (11) umfasst, in welchem der zweite Phasenkomparator (9) so angeordnet ist, dass er ein Signal ausgibt, das proportional zu einer Phasendifferenz zwischen einem Ausgangssignal des ersten Zählers (7) und einem Ausgangssignal des zweiten Zählers (8) ist, wobei der erste Zähler (7) mit einem Ausgang eines Referenzoszillators (3) verbunden ist, der zweite Zähler (8) mit einem Ausgang des zweiten VCO (11) verbunden ist, der zweite Tiefpassfilter (10) mit einem Ausgang des zweiten Phasenkomparators (9) verbunden ist, der zweite VCO (11) mit einem Ausgang des zweiten Tiefpassfilters (10) verbunden ist und das Frequenzteilungsverhältnis des zweiten Zählers (8) durch erste durch die Steuerschaltung (4) übertragene Frequenzteilungsverhältnisdaten veränderbar ist,
   wobei der zweite Frequenzsynthesizer (2) einen dritten Zähler (12), einen vierten Zähler (13), einen dritten Phasenkomparator (14), einen dritten Tiefpassfilter (15) und einen dritten VCO (16) umfasst, wobei der dritte Phasenkomparator (14) derart angeordnet ist, dass er ein Signal ausgibt, dass proportional zu einem Phasenunterschied zwischen einem Ausgangssignal des dritten Zählers (12) und einem Ausgangssignal des vierten Zählers (13) ist, wobei der dritte Zähler (12) mit einem Ausgang des Referenzoszillators (3) verbunden ist, der vierte Zähler (13) mit einem Ausgang des dritten VCO (16) verbunden ist, der dritte Tiefpassfilter (15) mit einem Ausgang des dritten Phasenkomparators (14) verbunden ist, der dritte VCO (16) mit einem Ausgang des dritten Tiefpassfilters (15) verbunden ist und das Frequenzteilungsverhältnis des vierten Zählers (13) durch zweite durch die Steuerschaltung (4) übertragene Frequenzteilungsverhältnisdaten veränderbar ist,
   wobei die Basisbandschaltung (6) das Verhältnis zwischen der Ausgangsfrequenz des Senders und den Ausgangsfrequenzen des ersten Frequenzsynthesizers (1) und des zweiten Frequenzsynthesizers (2) speichert und so angeordnet ist, dass sie das der Ausgangsfrequenz der Frequenzwandlungsschaltungen (1, 2) entsprechende Steuersignal basierend auf dem Verhältnis erzeugt, und
   wobei die Steuerschaltung (4) zumindest erste und zweite vorbestimmte erste Frequenzteilungsverhältnisdaten speichert und ausgebildet ist, um als bestimmte Ausgangsfrequenz (fVCO) des Senders eine Frequenz der zumindest ersten und zweiten vorbestimmten ersten Frequenzteilungsverhältnisdaten auszuwählen, bei der unerwünschten Störungen aufgrund von Oberschwingungen des Ausgangssignals der Frequenzwandlungsschaltung in Bezug auf die Ausgangsfrequenz (fVCO) des Senders am weitesten versetzt sind.

2. Sender nach Anspruch 1, worin die Steuerschaltung (4) Folgendes umfasst: ein erstes Register (23) zum Halten der ersten vorbestimmten ersten Frequenzteilungsverhältnisdaten; ein zweites Register (24) zum Halten der zweiten vorbestimmten ersten Frequenzteilungsverhältnisdaten; ein drittes Register (25) zum Halten der zweiten Frequenz-
teilungsverhältnisdaten und einen Wähler (27) zum Auswählen eines Satzes aus den ersten und zweiten vorbe-stimmten ersten Frequenzteilungsverhältnisdaten basierend auf Informationen, die im Steuersignal enthalten sind.

3. Sender nach Anspruch 2, worin der erste Zähler (7), der zweite Zähler (8), der zweite Phasenkomparator (9), der dritte Zähler (12), der vierte Zähler (13), der dritte Phasenkomparator (14), der Modulator (18), der Teiler (12), der erste Phasenkomparator (19), der Mischer (17) und die Steuerschaltung (4) in derselben IS ausgebildet sind.

4. Sender nach Anspruch 1, worin die Steuerschaltung (4) Folgendes umfasst: ein erstes Register (23) zum Halten der ersten vorbestimmten ersten Frequenzteilungsverhältnisdaten; ein zweites Register (24) zum Halten der zweiten vorbestimmten ersten Frequenzteilungsverhältnisdaten; ein drittes Register (30) zum Halten der dritten vorbestimmten ersten Frequenzteilungsverhältnisdaten; ein viertes Register (25) zum Halten der zweiten Frequenzteilungsverhältnisdaten und einen Wähler (27) zum Auswählen eines Satzes aus den ersten, zweiten oder dritten vorbestimmten ersten Frequenzteilungsverhältnisdaten basierend auf Informationen, die im Steuersignal enthalten sind.

5. Sender nach Anspruch 4, worin zumindest der erste Zähler (7), der zweite Zähler (8), der zweite Phasenkomparator (9), der dritte Zähler (12), der vierte Zähler (13), der dritte Phasenkomparator (14) und der zweite VCO (11) in derselben IS ausgebildet sind.

6. Sender nach Anspruch 5, wobei der Modulator (18), der Teiler (12), der erste Phasenkomparator (19), der Mischer (17) und die Steuerschaltung (4) weiters in derselben IS ausgebildet sind.

7. Drahtloses Kommunikationsendgerät, umfassend:

   eine Sendeschaltung (33), die mit einem Ausgang einer Empfangsschaltung (37) verbunden ist, in die ein erstes Ausgangssignal und ein zweites Signal der Sendeschaltung (33) eingegeben werden; einen Leistungsverstärker (34), in den ein drittes Ausgangssignal der Sendeschaltung (33) eingegeben wird; einen Antennenschalter (35), der mit einem Eingang der Empfangsschaltung (37) und einem Ausgang des Leistungsverstärkers (34) verbunden ist; und eine Antenne (36), die mit dem Antennenschalter (35) verbunden ist, wobei:

   wobei die Sendeschaltung ein Sender nach einem der Ansprüche 1 bis 6 ist, wobei das erste Ausgangssignal und das zweite Ausgangssignal ein Ausgangssignal des zweiten Frequenzsynthesizers (2) bzw. ein Eingangssignal des Modulators (18) der Sendeschaltung sind, wobei das dritte Ausgangssignal ein Ausgangssignal des ersten VCO (21) der Sendeschaltung ist und wobei ein Ausgangssignal der Empfangsschaltung (37) in die Basisbandschaltung (6) der Sendeschaltung eingegeben wird, wobei ein Informationssignal ausgegeben wird.


Revendications

1. Emetteur comprenant:

   un premier synthétiseur de fréquence (1);
   un deuxième synthétiseur de fréquence (2);
   un circuit de bande de base (6) pour émettre un signal de bande de base et un signal de commande sur la base d’un signal d’information;
   un circuit de commande (4) pour changer les fréquences de sortie du premier synthétiseur de fréquence (1) et du deuxième synthétiseur de fréquence (2) sur la base du signal de commande;
   un diviseur (12) pour diviser un signal de sortie du premier synthétiseur de fréquence (1);
   un modulateur (18) pour accepter un signal de sortie du premier synthétiseur de fréquence (1) soit un signal porteur et moduler le signal porteur sur la base du signal de bande de base;
   un circuit de conversion de fréquence (5) pour utiliser un signal de sortie du modulateur (18) et un signal de sortie du deuxième synthétiseur de fréquence (2) pour une conversion ascendante d’une fréquence porteuse du signal de sortie du modulateur (18); et
   une sortie pour fournir un signal de sortie de l’émetteur à une fréquence de sortie (fVCO),
où
le circuit de conversion de fréquence (5) comprend un premier comparateur de phase (19), un premier filtre passe-bas (20), une première VCO (21) et un mélangeur (17), et le circuit de conversion de fréquence (5) est un circuit de conversion de fréquence PLL dans lequel le premier comparateur de phase (19) est apte à émettre un signal proportionnel à une différence de phase entre un signal de sortie du modulateur (18) et un signal de sortie du mélangeur (17);
le premier filtre passe-bas (20) est connecté à une sortie du premier comparateur de phase (19);
là première VCO (21) est reliée à une sortie du premier filtre passe-bas (20) et est apte à fournir la fréquence de sortie (fVCO);
le mélangeur (17) est apte à mélanger un autre signal de sortie de la première VCO (21) et un signal de sortie du deuxième synthétiseur de fréquence (2);
le premier synthétiseur de fréquence (1) comprend un premier compteur (7), un deuxième compteur (8), un deuxième comparateur de phase (9), un deuxième filtre passe-bas (10) et une deuxième VCO (11), où le deuxième comparateur de phase (9) est agencé pour émettre un signal proportionnel à une différence de phase entre un signal de sortie du premier compteur (7) et un signal de sortie du deuxième compteur (8), le premier compteur (7) est relié à une sortie d’un oscillateur de référence (3), le deuxième compteur (8) est relié à une sortie de la deuxième VCO (11), le deuxième filtre passe-bas (10) est relié à une sortie du deuxième comparateur de phase (9), la deuxième VCO (11) est relié à une sortie du deuxième filtre passe-bas (10) et un rapport de division de fréquence du deuxième compteur (8) peut être changé par des premières données de rapport de division de fréquence transmises par le circuit de commande (4),
le deuxième synthétiseur de fréquence (2) comprend un troisième compteur (12), un quatrième compteur (13), un troisième comparateur de phase (14), un troisième filtre passe-bas (15) et une troisième VCO (16), le troisième comparateur de phase (14) étant agencé pour émettre un signal proportionnel à une différence de phase entre un signal de sortie du troisième compteur (12) et un signal de sortie du quatrième compteur (13), le troisième compteur (12) est relié à une sortie de l’oscillateur de référence (3), le quatrième compteur (13) est relié à une sortie de la troisième VCO (16), le troisième filtre passe-bas (15) est relié à une sortie du troisième comparateur de phase (14), la troisième VCO (16) est reliée à une sortie du troisième filtre passe-bas (15), et un rapport de division de fréquence du quatrième compteur (13) peut être changé par des deuxième données de rapport de division de fréquence transmises par le circuit de commande (4),
le circuit de bande de base (6) stocke une relation entre la fréquence de sortie de l’émetteur et les fréquences de sortie du premier synthétiseur de fréquence (1) et de deuxième synthétiseur de fréquence (2) et est agencé pour produire le signal de commande correspondant à la fréquence de sortie des circuits de conversion de fréquence (1, 2) sur la base de la relation, et
le circuit de commande (4) stocke au moins des premières et deuxième données de rapport de division de première fréquence prédéterminées et est apte à sélectionner pour une fréquence de sortie donnée (fVCO) de l’émetteur celle parmi les au moins premières et deuxième données de rapport de division de première fréquence prédéterminées pour lesquelles une réponse parasite non souhaitée due aux harmoniques du signal de sortie du circuit de conversion de fréquence sont décalées plus loin de la fréquence de sortie (fVCO) de l’émetteur.

2. Emetteur selon la revendication 1, où le circuit de commande (4) comprend un premier registre (23) pour retenir les premières données de rapport de division de première fréquence prédéterminées; un deuxième registre (24) pour retenir les deuxième données de rapport de division de première fréquence prédéterminées; un troisième registre (25) pour retenir les deuxième données de rapport de division de fréquence; et un sélecteur (27) pour sélectionner l’une parmi les premières et deuxième données de rapport de division de première fréquence prédéterminées sur la base des informations incluses dans le signal de commande.

3. Emetteur selon la revendication 2, où le premier compteur (7), le deuxième compteur (8), le deuxième comparateur de phase (9), le troisième compteur (12), le quatrième compteur (13), le troisième comparateur de phase (14), le modulateur (18), le diviseur (12), le premier comparateur de phase (19), le mélangeur (17) et le circuit de commande (4) sont formés dans le même CI.

4. Emetteur selon la revendication 1, où le circuit de commande (4) comprend un premier registre (23) pour retenir les premières données de rapport de division de première fréquence prédéterminées; un deuxième registre (24) pour retenir les deuxième données de rapport de division de première fréquence prédéterminées; un troisième registre (30) pour retenir les deuxième données de rapport de division de première fréquence prédéterminées; un quatrième registre (25) pour retenir les deuxième données de rapport de division de fréquence; et un sélecteur (27) pour sélectionner l’une parmi les premières, deuxième ou troisièmes données de rapport de division de
première fréquence prédéterminées sur la base des informations incluses dans le signal de commande.

5. Emetteur selon la revendication 4, où au moins le premier compteur (7), le deuxième compteur (8), le deuxième comparateur de phase (9), le troisième compteur (12), le quatrième compteur (13), le troisième comparateur de phase (14) et la deuxième VCO (11) sont formées dans le même CI.

6. Emetteur selon la revendication 5, où le modulateur (18), le diviseur (12), le premier comparateur de phase (19), le mélangeur (17) et le circuit de commande (4) sont formés en outre dans le même CI.

7. Appareil terminal de communication sans fil comprenant un circuit émetteur (33) connecté à une sortie d’un circuit de réception (37); auquel un premier signal de sortie et un deuxième signal du circuit émetteur (33) sont entrés; un amplificateur de puissance (34) dans lequel un troisième signal de sortie du circuit de transmission (33) est entré; un commutateur d’antenne (35) connecté à une entrée du circuit de réception (37) et à une sortie de l’amplificateur de puissance (34); et une antenne (36) connectée au commutateur d’antenne (35), où:

le circuit émetteur est l’émetteur selon l’une quelconque des revendications 1 à 6,
le premier signal de sortie et le deuxième signal de sortie sont un signal de sortie du deuxième synthétiseur de fréquence (2) et un signal d’entrée au modulateur (18) du circuit émetteur, respectivement,
le troisième signal de sortie est un signal de sortie de la première VCO (21) du circuit de transmission, et
un signal de sortie du circuit de réception (37) est entré dans le circuit de bande de base (6) du circuit émetteur, où un signal d’information est émis.

8. Appareil terminal de communication sans fil selon la revendication 7, où un duplexeur est utilisé à la place d’un commutateur d’antenne.
FIG. 1
FIG. 2

- 400k~1.8MHz offset
- 6M~25MHz offset
- 400k~1.8MHz offset
- 6M~25MHz offset

solid line: fIF = 270MHz
dotted line: fIF = 272MHz
FIG. 8

- ◇ 400kHz~1.8MHz offset
- □ 6MHz~25MHz offset

Difference between transmitting signal and undistorted output (dB)

Frequency of transmitting signal (MHz)

FIG. 9

RL 3.1dBm 10dB/RL

RBW=30kHz, VBW=30kHz
REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 0964523 A [0019]

Non-patent literature cited in the description