Method and circuit for controlling baseband gain
Verfahren und Schaltkreis zum Regeln der Basisbandverstärkung
Méthode et circuit pour commander le gain en bande de base

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BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

[0001] The present invention relates to a baseband gain control and particularly to a baseband gain control method and circuit capable of effectively preventing problems derived from a DC offset in the gain control of a direct conversion baseband circuit or the like.

2. Description of the Prior Art

[0002] A receiver utilizing direct conversion is advantageous over conventional super-heterodyne type receiver in the following respects and, therefore, expected to be widely used in the future:

1) A high frequency circuit section is simplified and the number of parts such as a filter can be reduced.
2) Since most of the functions including band limitation and AGC (automatic gain control) are executed at a baseband frequency, they can be realized by a CMOS analog circuit suited for LSI.

[0003] FIG. 6 is a view showing the concrete constitution of a direct conversion receiver. FIG. 6 shows a baseband gain control system for controlling the gain of a direct conversion baseband circuit, e.g., a system which has a wide dynamic range in the reception signals of a receiver of such a type as W-CDMA (Wide Band Code Division Multiple Access).

[0004] A high frequency signal received by an antenna 201 is subjected to band-limitation by a high frequency band-pass filter 202 and a received band is taken out. The signal thus band-limited is amplified by a low noise amplifier LNA 203 and directly inputted into a quadrature demodulator 204. The quadrature demodulator 204 is driven by a local signal generated by a local oscillator 225. The frequency of this local signal is the same as the central frequency of the received high frequency signal.

[0005] The quadrature demodulator 204 consists of multiplication circuits 222 and 223 and a phase circuit 224. The balanced outputs of the low noise amplifier LNA 203 are multiplied by the multiplication circuits 222 and 223 through an amplifier 221 in response to the balanced outputs of an orthogonal signal having a phase of 0° and that of 90° of the local signal, respectively, a baseband signal is directly generated from the high frequency signal, and two types of signals, i.e., baseband signals I and Q, are outputted as demodulated outputs. These baseband signals I and Q are subjected to band-limitation by baseband filters 205 and 206, respectively, and then amplified by an AGC circuit 207 so as to have a constant average amplitude.

[0006] The dynamic range of the AGC circuit 207 has characteristics of reaching several tens of decibels (about 80dB for CDMA). The outputs of the AGC circuit 207 are outputted to the next stage as signals 215 and 216, respectively. It is noted that a circuit controlling the gain of this circuit and the algorithm thereof are unrelated to the present invention and, therefore, not described herein.

[0007] FIG. 7 is a view showing that the baseband circuit for I or Q shown in FIG. 6 is taken out. The baseband circuit consists of a plurality of gain control amplifiers having C-cut structures. To simplify description, FIG. 7 shows the baseband circuit as a single-end circuit. A baseband filter 101 and variable gain amplifiers 102, 103 and 104 (which amplifiers may...
be also referred to as "VGA1", "VGA2" and "VGA3", respectively) correspond to the baseband filter 205 (206) and the variable gain amplifiers 208 (211), 209 (212) and 210 (213), respectively.

[0012] According to this structure, for the purpose of preventing the propagation of a DC offset and the saturation of a signal due to the propagation thereof, high-pass filters 109 to 111 corresponding to C-cuts are inserted between the input section of the circuit and the VGA 102, the VGA 102 and VGA 103, the VGA 103 and the VGA 104 and the VGA 104 and the output section, respectively. The gains of the VGA 1, VGA2 and VGA 3 are controlled by gain control data distributed from the gain distribution circuit 112 based on gain data inputted from externally.

[0013] As stated above, by inserting the high-pass filters into the baseband circuit in appropriate units of the circuit, the propagation of a direct current is prevented in a static state in which gains have no change. In addition, the saturation of a signal due to the DC offset can be prevented.

[0014] However, according to the conventional method for eliminating a DC offset in the baseband circuit of the direct conversion receiver, a transient phenomenon due to the DC offset occurs in a dynamic control state in which gains have great change, which often has an adverse effect on reception characteristics.

[0015] Assuming that offset voltages $V_{of1}$, $V_{of2}$ and $V_{of3}$ are added to the input sides of the VGA1, VGA2 and VGA3, respectively, based on the circuit of FIG. 7, it is considered what type of a transient phenomenon occurs to an output if the respective gains $g_1$, $g_2$ and $g_3$ are changed.

[0016] It is assumed here that the transfer functions of the high-pass filters 109 to 111 inserted as shown in FIG. 7 are the same and represented by the following expression for brevity.

$$B(s) = \frac{s}{s + \alpha} \quad \ldots (1).$$

[0017] It is assumed that the gains of the VGA1, VGA2 and VGA3 (not as dB values but as true values) are $g_1$, $g_2$ and $g_3$, respectively, and that these gains are changed to $g'_1$, $g'_2$ and $g'_3$, respectively. For brevity, the following conditions are set:

a) The gains $g_1$, $g_2$ and $g_3$ are 1 time to 16 times as high as inputs;

b) The gains $g_1$, $g_2$ and $g_3$ are not changed simultaneously; and

c) The gains $g_1$, $g_2$ and $g_3$ are changed instantaneously.

1) If the gain of the VGA3 is changed from $g_3$ to $g'_3$:

Since being cut by the high-pass filters 109 and 110, respectively, the offset voltages $V_{of1}$ and $V_{of2}$ have no effect on the output and only the offset voltage $V_{of3}$ has an effect on the output. At the input of the high-pass filter 111, a step-like voltage change $\Delta V_3$ occurs as follows.

$$\Delta V_3 = (g'_3 - g_3) \cdot V_{of3} \quad \ldots (2).$$

This step-like change influences an output $V_{out}$ through the high-pass filter 111. A contribution thereof is described using Laplace transform as follows.

$$V_{out(s)} = B(s) \cdot \frac{\Delta V_3}{s} = (g'_3 - g_3) \cdot V_{of3} \cdot \frac{1}{s + \alpha} \quad \ldots (3).$$

Assuming that $g_3$ is changed at $t = 0$, a time response is obtained as follows.

$$V_{out(t)} = (g'_3 - g_3) \cdot V_{of3} \cdot e^{-\alpha t} \quad \ldots (4).$$
2) If the gain of the VGA2 is changed from $g_2$ to $g_2'$:

Because of the high-pass filter 110, the offset of the output of the VGA2 is cut by the filter 110 in a steady state. Then, it is assumed that $g_2$ is changed to $g_2'$. At this moment, the following step-like voltage change $\Delta V_2$ occurs to the input of the high-pass filter 110.

$$\Delta V_2 = (g_2' - g_2) \cdot V_{qf2} \quad \ldots (5).$$

This step-like change influences the output $V_{out}$ through two stages of the high-pass filters. A contribution thereof is described using Laplace transform as follows.

$$V_{out}(s) = g_3 \cdot B(s)^2 \cdot \frac{\Delta V_2}{s} = g_3 \cdot \Delta V_2 \cdot \frac{s}{s + \alpha} \cdot \frac{1}{s + \alpha} \quad \ldots (6).$$

Assuming that $g_2$ is changed at $t = 0$, a time response is obtained as follows:

$$V_{out}(t) = g_3 \cdot \Delta V_2 \cdot (1 - \alpha \cdot t) \cdot e^{-\alpha t}$$

$$= g_3 \cdot (g_2' - g_2) \cdot V_{qf2} \cdot (1 - \alpha \cdot t) \cdot e^{-\alpha t} \quad \ldots (7).$$

3) If the gain of the VGA1 is changed from $g_1$ to $g_1'$:

Because of the high-pass filter 109, the offset of the output of the VGA1 is blocked by the filter 109 in a steady state. Then, it is assumed that $g_1$ is changed to $g_1'$. At this moment, the following step-like voltage change $\Delta V_1$ occurs to the input of the high-pass filter 109.

$$\Delta V_1 = (g_1' - g_1) \cdot V_{qf1} \quad \ldots (8).$$

This step-like change influences the output $V_{out}$ through three stages of the high-pass filters. A contribution thereof is described using Laplace transform as follows.

$$V_{out}(s) = g_3 \cdot g_2 \cdot B(s)^3 \cdot \frac{\Delta V_1}{s} = g_3 \cdot g_2 \cdot \Delta V_1 \cdot \frac{s}{s + \alpha} \cdot \frac{s}{s + \alpha} \cdot \frac{1}{s + \alpha} \quad \ldots (9).$$

Assuming that $g_1$ is changed at $t = 0$, a time response is obtained as follows.

$$V_{out}(t) = g_3 \cdot g_2 \cdot \Delta V_1 \cdot (1 - 2 \cdot \alpha \cdot t + \alpha^2 \cdot t^2) \cdot e^{-\alpha t}$$

$$= g_3 \cdot g_2 \cdot (g_1' - g_1) \cdot V_{qf1} \cdot (1 - 2 \cdot \alpha \cdot t + \alpha^2 \cdot t^2) \cdot e^{-\alpha t} \quad \ldots (10).$$
According to the direct conversion type receiver, it is necessary to control gains almost in a baseband frequency. Therefore, the saturation of amplifiers disadvantageously occurs due to the DC offset which occurs to the respective sections of the baseband circuit. To prevent this, a method for blocking the propagation of a DC component by providing high-pass filters at appropriate places of a circuit may be considered. In this case, however, a transient voltage occurs and deteriorates characteristics by changing the gain of each stage inadvertently.

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As is obvious from FIGS. 8 to 10, even if a direct current component can be blocked by the high-pass filters, a high transient voltage occurs to the outputs and deteriorates characteristics by changing the gain of each stage inadvertently.

An object of the present invention is to provide a baseband gain control method and circuit capable of suppressing the generation of a transient voltage in the setting of the gains of a plurality of variable gain amplifiers in a baseband circuit.

The present invention is defined in independent claims 1 and 4. The dependent claims define further embodiments of the invention.

Gain control is carried out so that the upper limit of the quantity of the change of the gains of a plurality of variable gain amplifiers for a baseband signal is set. Further, if the gain is to be increased, the gains of the variable gain amplifiers starting at the variable gain amplifier close to an input are sequentially increased. Further, if the gain is to be decreased, the gains of the variable gain amplifiers starting at the variable gain amplifier farthest to the input are sequentially decreased. Thus, it is possible to effectively suppress the generation of a transient voltage caused by a DC offset during the gain control.

The combination of the gain control for providing the upper limit of the quantity of the change of a gain and the distribution control for distributing different gains to a plurality of variable gain amplifiers according to the increase and decrease of the gain enables, in particular, suppressing the generation of a transient voltage caused by a DC offset more effectively.

If the present invention is applied to the gain control of a direct conversion baseband circuit, e.g., the baseband gain control of a direct conversion baseband circuit having a wide dynamic range of a reception signal such as a receiver of a W-CDMA (Wide Band Code Division Multiple Access) type, the present invention exhibits considerably great advantage.
BRIEF EXPLANATION OF THE DRAWINGS

[0032]

FIG. 1 is a view showing one mode for carrying out a baseband gain control circuit of the present invention. FIG. 2 is a flow chart showing the operation of a gain converting circuit in this mode for carrying out the invention. FIG. 3 shows a manner in which the gain of a variable gain amplifier follows gain control data. FIG. 4 is a flow chart showing the operation of a gain distribution circuit. FIG. 5 is a view showing an example in which the gain distribution circuit is constituted out of an ROM. FIG. 6 is a view showing the constitution of a conventional direct conversion receiver. FIG. 7 is a view showing the baseband circuit of the circuit shown in FIG. 6 as a single-end circuit for brevity. FIG. 8 shows the waveform of an expression (4) if V_{of3} is 1 mV and g3 is changed from 1 time to 16 times as high as an input. FIG. 9 shows the waveform of an expression (7) if V_{of2} is 1 mV and g3 is 16 times as high as the input and g2 is changed from 1 time to 16 times as high as the input. FIG. 10 shows the waveform of an expression (10) if V_{of1} is 1 mV and g3 and g2 are 16 times as high as the input and g1 is changed from 1 time to 16 times as high as the input. PREFERRED EMBODIMENT OF THE INVENTION

[0033] FIG. 1 is a block diagram showing the basic constitution of a baseband gain control circuit of the present invention. A signal path shown therein has, similarly to the conventional circuit shown in FIG. 7, a constitution of the reception signal baseband gain control system of a receiver such as a W-CDMA (Wide Band Code Division Multiple Access) system. The block diagram of FIG. 1 shows a single-end circuit as in the case of the description of the conventional circuit.

(First Mode of the Invention)

[0034] The first mode for carrying out the present invention is characterized by comprising a gain distribution circuit 112 and a gain converting circuit 113 as shown in FIG. 1 and in that an upper limit of the gain control is set to the gain control circuit 113. [0035] The gain converting circuit 113 is a circuit converting inputted gain data (Gain Data: corresponding to dB) into gain output data (Gain Output: corresponding to dB) actually set to variable gain amplifiers. [0036] Also, the gain distribution circuit 112 is a circuit having a function of distributing the gain output data inputted from the gain converting circuit 113 to a plurality of variable gain amplifiers as gain control data and controlling the data. In this mode for carrying out the invention, the circuit is constituted so that that the gain output data (Gain Output), either as it is or uniformly amplified/attenuated, is distributed and supplied to a plurality of variable gain amplifiers. [0037] Here, if the Gain Input has a large change, e.g., 48 dB is changed by 24 dB to 72 dB and this change is reflected on the set values of the variable gain amplifiers, respectively, a high transient voltage is generated by a DC offset as already described in detail in “Problems that the Invention is to Solve” part. [0038] Taking this into consideration, in this mode for carrying out the invention, the upper limit or the maximum step of a gain (MAXSTEP) which can be changed once is set. For example, MAXSTEP is set at 2 dB. By setting so, the quantity of the change of a gain of 24 dB is attained from 12 quantities of change each of 2 dB at intervals of predetermined periods (Pre-Determined Periods). As a result, the generation of a transient voltage can be effectively suppressed. [0039] For example, FIG. 8 shows the transient voltage if V_{of3} is 1 mV and the gain g3 of the VGA3 is changed from 1 times (0 dB) to 16 times (24 dB) as high as the input. The transient voltage at a peak of 1 mV × (16-1) = 15 mV is generated. [0040] If the gain g3 is changed from 22 dB by 2 dB to 24 dB, a voltage X (dBm) at 1 mV and 22 dB can be obtained as 1 mV × 10^{(22/20)} from 20log_{10}X = 22dB. Therefore, to change the gain by 2 dB, it suffices that the voltage is 1 mV × (16-10^{(22/20)}) = 3.4 mV [0041] The gain converting circuit 113 outputs such gain output data, as gain set value, to the gain distribution circuit 112 and the gain distribution circuit 112 distributes the gain set value to the respective variable gain amplifiers 102, 103 and 104 either as it is or while amplifying/attenuating the value. [0042] As stated above, the gains of the respective variable gain amplifiers are controlled a plurality of times at intervals of predetermined periods based on the upper limit of the maximum quantity of change or MAXSTEP, whereby the peak value of a transient voltage can be greatly reduced. [0043] FIG. 2 is a flow chart showing the operation of the gain converting circuit 113 in the first mode for carrying out the invention. If the inputted Gain Input value is higher than the Gain Output currently set to the variable gain amplifiers...
by MAXSTEP dB or more (‘YES’ in a step s1), then the MAXSTEP dB is added to the currently set Gain Output to obtain a newly set Gain Output (in a step s4). Conversely, if the inputted Gain Input value is lower than the currently set Gain Output by MAXSTEP dB or more (‘NO’ in the step s1 and ‘YES’ in the step s2), then MAXSTEP dB is subtracted from the currently set Gain Output to obtain a newly set Gain Output (in a step s6). In the other case (‘NO’ in the step s1 and ‘NO’ in the step s2), the currently set Gain Input becomes a newly set Gain Output (in a step s3). This operation is carried out in each pre-determined period (Pre-Determined Period) (in steps s5 and s7) until the Gain Output becomes equal to the Gain Input.

As a result, the quantity of the change of the Gain Output in each pre-determined period is limited to MAXSTEP dB or lower.

It is also possible to determine the maximum number of times for circulating the flow in the flow chart of FIG. 2 so as not to change the Gain Output if the number of times exceed the maximum number.

FIG. 3 shows a manner in which the Gain Output follows the Gain Input. In the example shown in FIG. 3, the Gain Input greatly increases compared with the Gain Output at a time t = 0 and, therefore, the Gain Output increases by MAXSTEP in each Pre-Determined Period. At a time t = t1, the Gain Input and the Gain Output satisfy Gain Input \(\leq\) Gain Output + MAXSTEP. In this case, they also satisfy Gain Input \(\geq\) Gain Output - MAXSTEP. Thus, the Gain Output is set to be Gain Input (Gain Output = Gain Input). Thereafter, the Gain Input decreases to lower level, so that after the time t = t1, the Gain Output decreases by MAXSTEP in each Pre-Determined Period and at a time t = t2, the Gain Output is set to be Gain Input (Gain Output = Gain Input).

As can be seen, if the limiting value is set for the quantity of the change of a gain which can be changed once and the change of a gain exceeding the limiting value is controlled, then control is carried out for attaining a required gain change as a plurality of times of changes of the gain each equal to or lower than the limiting value of the gain change. That is, a plurality of quantities of the change of the gain and the quantity of the change of the last gain equal to or lower than the limit value are controlled.

According to the gain control in this mode for carrying out the invention, therefore, even if the Gain Input is greatly changed, the change of a gain is gradually made for a long period of time and the change of the Gain Output can be, therefore, decreased. Due to this, even if there is an offset in a plurality of variable gain amplifiers, it is possible to suppress the generation of a sudden transient voltage.

(Second Mode)

In the mode for carrying out the invention stated above, description has been given to a case where the gain distribution circuit 113 uniformly distributes gain control data to a plurality of variable gain amplifiers. It is also possible to greatly suppress the generation of a transient voltage by a distribution method by the gain distribution circuit 113.

The gain distribution circuit 112 exercises control so as to supply different gain control data to a plurality of variable gain amplifiers.

Assume that the gain converting circuit 113 outputs gain data as gain control data as it is. The example shown in FIG. 10, for example, shows the transient voltage if \(V_{of1}\) is 1 mV, the gain \(g_1\) of the VGA1 is changed from 1 time (i.e., 0 dB) to 16 times (24 dB) as high as the input and the gains \(g_2\) and \(g_3\) are the maximum gain of 24 dB, respectively. The transient voltage at a peak as high as

\[
1 \text{ mV} \times (16-1) \times 16 \times 16 = 3840 \text{ mV}
\]

is generated.

This is because the gains \(g_3\) and \(g_2\) are the maximum gain of 24 dB, respectively. To prevent this, the gain distribution circuit 113 distributes a gain as follows.

For example, if the gain of a certain VGA is changed, the gains of all the VGA’s provided right of the VGA are set at a minimum gain, respectively.

According to the example, the minimum gain is 0 dB. By so controlling, a transient voltage is limited to

\[
1 \text{ mV} \times (16-1) \times 1 \times 1 = 15 \text{ mV}.
\]

FIG. 4 is a flow chart showing the operation of the gain distribution circuit 112. In the control conducted by the gain distribution circuit 112 in this mode, a control algorithm that the gains of variable gain amplifiers starting at a variable gain amplifier close to an input are sequentially increased and that, if the gain is decreased, the gains of variable gain
amplifiers starting at a variable gain amplifier farthest to the input are sequentially decreased is utilized. The gain distribution circuit 112 exercises control so that the maximum value of the amplification gains of the variable gain amplifiers in this mode becomes, for example, 24 dB, threshold values are set at 24 dB and 48 dB for the input gain data (Gain) of the gain distribution circuit and that the respective variable gain amplifiers have different gains according to the state of the input gain data.

[0056] In a step s11, it is judged whether or not the Gain inputted to the gain distribution circuit 112 is higher than 48 dB. If the Gain is higher than 48 dB, then the VGA1, VGA2 and VGA 3 are set at 24 dB, 24 dB and (Gain-48 dB), respectively and the operation returns to the step s11. If it is judged that the Gain is equal to or lower than 48 dB in the step s11, it is then judged whether or not the Gain is higher than 24 dB in a step s12. If the Gain is higher than 24 dB, then the VGA1, VGA2 and VGA3 are set at 24 dB, (Gain-24 dB) and 0 dB, respectively and the operation returns to the processing of the step s11. If the Gain is lower than 24 dB, then the VGA1, VGA2 and VGA3 are set at Gain, 0 dB and 0 dB, respectively and the operation returns to the processing of the step s11.

[0057] If gain is distributed to the VGA1, VGA2 and VGA3 as the respective gain control data of a plurality of variable gain control amplifiers as shown in FIG. 4 and a certain VGA is changed, data is controlled so that the gains of the VGA’s on the output side relative to the certain VGA become a minimum gain, respectively.

[0058] In the examples of gain distribution to the VGA1, VGA2 and VGA3 in this mode, the gain distribution circuit exercises control based on the control algorithm that if the gain control data from the gain converting circuit 113 or Gain is high (higher than the threshold value of 48 dB), the gains of the VGA1 and the VGA2 closer to an input are increased to 24 dB and the gain of the VGA3 is the remaining gain of (Gain - 48 dB) to satisfy VGA1, VGA2 > VGA3, that if the Gain is an intermediate (higher than the threshold value of 24 dB and equal to or lower than the threshold value of 48 dB), the VGA1, VGA2 and VGA3 are set to satisfy VGA1 (= 24 dB) > VGA2 (= Gain - 24 dB) > VGA3 (= 0dB) and that if the Gain is low (lower than 24 dB), the VGA1, VGA2 and VGA3 are set to satisfy VGA1 (= Gain) > VGA2 (= 0 dB), VGA3 (= 0 dB). In short, if the gain is to be increased, the gains of variable gain amplifiers starting from the variable gain amplifier close to an input are sequentially increased. If the gain is to be decreased, those of variable gain amplifiers starting from the variable gain amplifier farthest to the input are sequentially decreased.

(Third Mode of the Invention)

[0059] As a mode for carrying out the invention for suppressing a transient voltage more effectively in the gain control of the present invention, the first mode and the second mode are combined. A combination of gain control while setting an upper limit for the quantity of gain change and distribution control for distributing different gains to a plurality of variable gain amplifiers according to the increase and decrease of the gain are conducted, thereby making it possible to realize the effect of suppressing a transient voltage in a multiplied manner.

[0060] In this mode for carrying out the invention, a gain converting circuit 113 is constituted to carry out an operation with a maximum step provided at the circuit 113 as in the case of the first mode for carrying out the invention. A gain distribution circuit 112 is constituted to distribute gain control data as in the case of the second mode.

[0061] While a transient voltage is suppressed down to 1 mV×(16-1)×1×1 = 15 mV in the second mode, a transient voltage can be further decreased to

\[ 1 \text{ mV} \times (16-10^{(22/20)}) \times 1 \times 1 = 3.4 \text{ mV} \]

in this mode for carrying out the invention.

[0062] While description has been given using flow charts so far, the function of the flow charts can be realized by a hardware by describing the function as it is with a functional description language such as VHDL.

(Another Mode of the Invention)

[0063] As another mode for carrying out the present invention, a gain distribution circuit 112 can be constituted out of an ROM while the basic constitution of the circuit is the same as those described above.

[0064] FIG. 5 shows an example in which the gain distribution circuit is constituted out of an ROM. As shown in FIG. 5, while a gain set value from a gain converting circuit 113 is set as an address input, the gains of respective variable gain amplifiers corresponding to the address input are read from the ROM and thereby set. Data written to the ROM is predetermined so as to satisfy the algorithm of FIG. 4, whereby the gain distribution circuit can operate in the same manner as that in the preceding modes for carrying out the invention.
Claims

1. A gain control method for controlling a total amplifying gain of an output from a baseband amplifier including a plurality of series-connected variable gain amplifiers (102, 103, 104), by using a gain output value output from a gain converting circuit (113) the method comprising the steps of:

- setting a prescribed gain change limit (MAXSTEP) for the total amplifying gain of said output from said baseband amplifier;
- comparing a received gain input value with a gain output value currently set;
- adding said prescribed gain change limit (MAXSTEP) to said currently set gain output value when said gain input value is higher than said currently set gain output value by said prescribed gain change limit (MAXSTEP) or more, or subtracting said prescribed gain change limit (MAXSTEP) from said currently set gain output value when said gain input value is lower than said currently set gain output value by said prescribed gain change limit (MAXSTEP) or more;
- waiting a predetermined time period; and
- repeating the comparing step, the adding step or the subtracting step, and the waiting step until a difference between said gain input value and said currently set gain output value is smaller than said prescribed gain change limit (MAXSTEP), and then setting the gain output value to be equal to the gain input value.

2. The gain control method according to claim 1, wherein the repeating step is limited to a prescribed number.

3. The gain control method according to claim 1, wherein said total amplifying gain is distributed in such a manner that the gains of said variable gain amplifiers (102, 103, 104) are increased in serial order from the input to the output of said baseband amplifier when said total amplifying gain is to be increased, while the gains of the variable gain amplifiers (102, 103, 104) are decreased in serial order from the output to the input of said baseband amplifier when said total amplifying gain is to be decreased.

4. A baseband amplifier including a plurality of series-connected variable gain amplifiers (102, 103, 104) adapted to control a total amplifying gain, comprising:

- a gain converting circuit (113) adapted to generate and output a gain output value for controlling the total amplifying gain by
  - setting a prescribed gain change limit (MAXSTEP) for the total amplifying output from said baseband amplifier;
  - comparing a received gain input value with a gain output value currently set;
  - adding the prescribed gain change limit (MAXSTEP) to said currently set gain output value when said gain input value is higher than said currently set gain output value by said prescribed gain change limit or more, or subtracting said prescribed gain change limit from said currently set gain output value when said gain input value is lower than said currently set gain output value by said prescribed gain change limit or more;
  - waiting a predetermined time period; and
  - repeating the comparing step, the adding step or the subtracting step, and the waiting step until a difference between said gain input value and said currently set gain output value is equal to or smaller than said prescribed gain change limit (MAXSTEP) and then setting the gain output value to be equal to the gain input value; and
  - a gain distribution circuit (112) for distributing the gain output value output from said gain converting circuit among the plurality of series-connected variable gain amplifiers (102, 103, 104).

5. The baseband amplifier according to claim 4, wherein said gain distribution circuit (112) equally distributes a total amplifying gain set by said gain converting circuit (113) among said variable gain amplifiers (102, 103, 104).

6. The baseband amplifier according to claim 4, wherein the repeating step is limited to a prescribed number.

7. The baseband amplifier according to claim 4, wherein said gain distribution circuit (112) distributes said total amplifying gain in such a manner that the gains of said variable gain amplifiers (102, 103, 104) are increased in serial order from the input to the output of said baseband amplifier when said total amplifying gain is to be increased, while the gains of said variable gain amplifiers (102, 103, 104) are decreased in serial order from the output to the input of said baseband amplifier when said total amplifying gain is to be decreased.
Patentansprüche

1. Verstärkungssteuerverfahren zum Steuern einer Gesamtverstärkung einer Ausgabe eines Basisbandverstärkers, der eine Mehrzahl von in Reihe geschalteten Verstärkern mit variabler Verstärkung (102, 103, 104) enthält, mittels eines von einer Verstärkungsumwandlungsschaltung (113) ausgegebenen Verstärkungsausgabewertes, wobei das Verfahren die Schritte umfasst:

   Festsetzen einer vorgeschriebenen Verstärkungsänderungsgrenze (MAXSTEP) für die Gesamtverstärkung der Ausgabe von dem Basisbandverstärker;
   Vergleichen eines empfangenen Verstärkungseingabewertes mit einem gegenwärtig festgesetzten Verstärkungsausgabewert;
   Addieren der vorgeschriebenen Verstärkungsänderungsgrenze (MAXSTEP) zu dem gegenwärtig festgesetzten Verstärkungsausgabewert, wenn der Verstärkungseingabewert um die vorgeschriebene Verstärkungsänderungsgrenze (MAXSTEP) oder mehr größer als der gegenwärtig festgesetzte Verstärkungsausgabewert ist, oder Subtrahieren der vorgeschriebenen Verstärkungsänderungsgrenze (MAXSTEP) von dem gegenwärtig festgesetzten Verstärkungsausgabewert, wenn der Verstärkungseingabewert um die vorgeschriebene Verstärkungsänderungsgrenze (MAXSTEP) oder mehr kleiner als der gegenwärtig festgesetzte Verstärkungsausgabewert ist;
   Warten einer vorbestimmten Zeitperiode; und
   Wiederholen des Vergleichsschrittes, des Addierschrittes oder des Subtrahierschrittes bis eine Differenz zwischen dem Verstärkungseingabewert und dem gegenwärtig festgesetzten Verstärkungsausgabewert kleiner als die vorgeschriebene Verstärkungsänderungsgrenze (MAXSTEP) ist, und danach Festsetzen des Verstärkungsausgabewerts derart, dass er gleich dem Verstärkungseingabewert ist.

2. Verstärkungssteuerverfahren nach Anspruch 1, wobei der Wiederholschritt auf eine vorgeschriebene Anzahl begrenzt ist.

3. Verstärkungssteuerverfahren nach Anspruch 1, wobei die Gesamtverstärkung auf eine solche Weise verteilt ist, dass die Verstärkungen der Verstärkern mit variabler Verstärkung (102, 103, 104) der Reihe nach von dem Eingang zu dem Ausgang des Basisbandverstärkers erhöht werden, wenn die Gesamtverstärkung zu erhöhen ist, während die Verstärkungen der Verstärker mit variabler Verstärkung (102, 103, 104) der Reihe nach von dem Ausgang zu dem Eingang des Basisbandverstärkers verringert werden, wenn die Gesamtverstärkung zu verringern ist.

4. Basisbandverstärker, der eine Mehrzahl von in Reihe geschalteten Verstärkern mit variabler Verstärkung (102, 103, 104) enthält, der dazu ausgelegt ist, eine Gesamtverstärkung zu steuern, umfassend:

   eine Verstärkungsumwandlungsschaltung (113), die dazu ausgelegt ist, einen Verstärkungsausgabewert zum Steuern der Gesamtverstärkung zu erzeugen und auszugeben durch

   Festsetzen einer vorgeschriebenen Verstärkungsänderungsgrenze (MAXSTEP) für die Gesamtverstärkung der Ausgabe von dem Basisbandverstärker;
   Vergleichen eines empfangenen Verstärkungseingabewertes mit einem gegenwärtig festgesetzten Verstärkungsausgabewert;
   Addieren der vorgeschriebenen Verstärkungsänderungsgrenze (MAXSTEP) zu dem gegenwärtig festgesetzten Verstärkungsausgabewert, wenn der Verstärkungseingabewert um die vorgeschriebene Verstärkungsänderungsgrenze (MAXSTEP) oder mehr größer als der gegenwärtig festgesetzte Verstärkungsausgabewert ist, oder Subtrahieren der vorgeschriebenen Verstärkungsänderungsgrenze (MAXSTEP) von dem gegenwärtig festgesetzten Verstärkungsausgabewert, wenn der Verstärkungseingabewert um die vorgeschriebene Verstärkungsänderungsgrenze (MAXSTEP) oder mehr kleiner als der gegenwärtig festgesetzte Verstärkungsausgabewert ist;
   Warten einer vorbestimmten Zeitperiode; und
   Wiederholen des Vergleichsschrittes, des Addierschrittes oder des Subtrahierschrittes bis eine Differenz zwischen dem Verstärkungseingabewert und dem gegenwärtig festgesetzten Verstärkungsausgabewert kleiner als die vorgeschriebene Verstärkungsänderungsgrenze (MAXSTEP) ist, und danach Festsetzen des Verstärkungsausgabewerts derart, dass er gleich dem Verstärkungseingabewert ist; und

   eine Verstärkungsverteilungsschaltung (112) zum Verteilen des von der Verstärkungsumwandlungsschaltung
ausgegebenen Verstärkungsausgabewerts auf die Mehrzahl von in Reihe geschalteten Verstärkern mit variabler Verstärkung (102, 103, 104).

5. Basisbandverstärker nach Anspruch 4, wobei die Verstärkungsverteilungsschaltung (112) eine durch die Verstärkungsumwandlungsschaltung (113) festgesetzte Gesamtverstärkung gleich auf die Verstärker mit variabler Verstärkung (102, 103, 104) verteilt.

6. Basisbandverstärker nach Anspruch 4, wobei der Wiederholschritt auf eine vorgeschriebene Anzahl begrenzt ist.

7. Basisbandverstärker nach Anspruch 4, wobei die Verstärkungsverteilungsschaltung (112) die Gesamtverstärkung auf eine solche Weise verteilt, dass die Verstärkungen der Verstärkern mit variabler Verstärkung (102, 103, 104) der Reihe nach von dem Eingang zu dem Ausgang des Basisbandverstärkers erhöht werden, wenn die Gesamtverstärkung zu erhöhen ist, während die Verstärkungen der Verstärker mit variabler Verstärkung (102, 103, 104) der Reihe nach von dem Ausgang zu dem Eingang des Basisbandverstärkers verringert werden, wenn die Gesamtverstärkung zu verringern ist.

Revendications

1. Procédé de commande de gain permettant de commander un gain d’amplification total d’une sortie provenant d’un amplificateur de bande de base incluant une pluralité d’amplificateurs de gain variable connectés en série (102, 103, 104), en utilisant une valeur de sortie de gain délivrée par un circuit convertisseur de gain (113), le procédé comprenant les étapes de :

   établissement d’une limite de modification de gain prescrite (MAXSTEP) pour le gain d’amplification total de ladite sortie provenant dudit amplificateur de bande de base ;
   comparaison d’une valeur d’entrée de gain reçue avec une valeur de sortie de gain actuellement établie ;
   addition de ladite limite de modification de gain prescrite (MAXSTEP) à ladite valeur de sortie de gain actuellement établie lorsque ladite valeur d’entrée de gain est plus élevée que ladite valeur de sortie de gain actuellement établie ;
   soustraction de ladite limite de modification de gain prescrite (MAXSTEP) de ladite valeur de sortie de gain actuellement établie lorsque ladite valeur d’entrée de gain est plus basse que ladite valeur de sortie de gain actuellement établie ;
   attente d’une durée prédéterminée ; et
   répétition de l’étape de comparaison, de l’étape d’addition ou de l’étape de soustraction, et de l’étape d’attente jusqu’à ce qu’une différence entre ladite valeur d’entrée et ladite valeur de sortie de gain actuellement établie soit plus petite que ladite limite de modification de gain prescrite (MAXSTEP), puis établissement de la valeur de sortie de gain pour qu’elle soit égale à la valeur d’entrée de gain.

2. Procédé de commande de gain selon la revendication 1, dans lequel l’étape de répétition est limitée à un nombre prescrit.

3. Procédé de commande de gain selon la revendication 1, dans lequel ledit gain d’amplification total est distribué de telle manière que les gains desdits amplificateurs de gain variable (102, 103, 104) soient augmentés en ordre sériel de l’entrée à la sortie dudit amplificateur de bande de base lorsque ledit gain d’amplification total doit être augmenté, alors que les gains des amplificateurs de gain variable (102, 103, 104) sont diminués en ordre sériel de la sortie à l’entrée dudit amplificateur de bande de base lorsque ledit gain d’amplification total doit être diminué.

4. Amplificateur de bande de base incluant une pluralité d’amplificateurs de gain variable connectés en série (102, 103, 104) adaptés pour commander un gain d’amplification total, comprenant :

   un circuit convertisseur de gain (113) adapté pour générer et délivrer une valeur de sortie de gain permettant de commander le gain d’amplification total par

   l’établissement d’une limite de modification de gain prescrite (MAXSTEP) pour la sortie d’amplification totale provenant dudit amplificateur de bande de base ;
   la comparaison d’une valeur d’entrée de gain reçue avec une valeur de sortie de gain actuellement établie ;
   l’addition de la limite de modification de gain prescrite (MAXSTEP) à ladite valeur de sortie de gain actuel-
lement établie lorsque ladite valeur d’entrée de gain est plus élevée que ladite valeur de sortie de gain actuellement établie de ladite limite de modification de gain prescrite ou plus, ou la soustraction de ladite valeur d’entrée de gain actuellement établie lorsque ladite valeur d’entrée de gain est plus basse que ladite valeur de sortie de gain actuellement établie de ladite limite de modification de gain prescrite ou plus ;
l’attente d’une durée prédéterminée ; et
la répétition de l’étape de comparaison, de l’étape d’addition ou de l’étape de soustraction, et de l’étape d’attente jusqu’à ce qu’une différence entre ladite valeur d’entrée et ladite valeur de sortie de gain actuellement établie soit plus petite que ladite limite de modification de gain prescrite (MAXSTEP), puis établissement de la valeur de sortie de gain pour qu’elle soit égale à la valeur d’entrée de gain ; et

un circuit de distribution de gain (112) permettant de distribuer la valeur de sortie de gain délivrée par ledit circuit convertisseur de gain parmi la pluralité d’amplificateurs de gain variable connectés en série (102, 103, 104).

5. Amplificateur de bande de base selon la revendication 4, dans lequel ledit circuit de distribution de gain (112) distribue de manière égale un gain d’amplification total établi par ledit circuit convertisseur de gain (113) parmi lesdits amplificateurs de gain variable (102, 103, 104).

6. Amplificateur de bande de base selon la revendication 4, dans lequel l’étape de répétition est limitée à un nombre prescrit.

7. Amplificateur de bande de base selon la revendication 4, dans lequel ledit circuit de distribution de gain (112) distribue ledit gain d’amplification total de telle manière que les gains desdits amplificateurs de gain variable (102, 103, 104) soient augmentés en ordre sériel de l’entrée à la sortie dudit amplificateur de bande de base lorsque ledit gain d’amplification total doit être augmenté, alors que les gains desdits amplificateurs de gain variable (102, 103, 104) diminuent en ordre sériel de la sortie à l’entrée dudit amplificateur de bande de base lorsque ledit gain d’amplification total doit être diminué.
FIG. 2

START

S1

Gain Input > Gain Output + MAXSTEP

Yes

S4

Gain Output = Gain Output + MAXSTEP

No

S2

Gain Input < Gain Output - MAXSTEP

Yes

S6

Gain Output = Gain Output - MAXSTEP

No

S3

Wait for a pre-determined period

S7

Wait for a pre-determined period

End
FIG. 3

Gain(dB)

Gain Input

Gain Output

MAXSTEP

Pre-determined Period

0 \quad t_1 \quad t_2
FIG. 4

START

 Gain > 48 dB

 S11

Yes

Gain > 24 dB

No

S12

VGA1 = 24 dB
VGA2 = Gain - 24 dB
VGA3 = Gain - 48 dB

S14

VGA1 = Gain
VGA2 = 0 dB
VGA3 = 0 dB

S15

VGA1 = 24 dB
VGA2 = Gain - 24 dB
VGA3 = 0 dB

Yes

No

S13

Yes

No
FIG. 5

Gain → ADDRESS

ROM

DATA OUTPUT

→ VGA1

→ VGA2

→ VGA3
FIG. 6 (PRIOR ART)

Quadrature Demodulator

RX Frequency

RFBPF

LNA

0°/90°

BBBPF

VGA

Gain Control Circuit

I

Q

IB

QB

1st LO = RX Frequency
FIG. 8 (PRIOR ART)
FIG. 9 (PRIOR ART)
FIG. 10 (PRIOR ART)
REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

• US 5298868 A [0026]