EUROPEAN PATENT SPECIFICATION

Date of publication and mention of the grant of the patent: 13.07.2005 Bulletin 2005/28

Application number: 99109526.6

Date of filing: 12.05.1999

Bi-directional shift register without stage to stage signal attenuation suitable as driving circuit for a display device and associated image sensing apparatus

Bidirektionales Schieberegister ohne zwischenstufige Signalabschwächung, geeignet als Steuerschaltung für eine Anzeigevorrichtung und zugehöriges Bildaufnahmegerät

Registre à décalage bidirectionnel sans atténuation de signaux entre les étages utilisable comme circuit de commande pour un dispositif d'affichage et appareil de prise d'image associé

Designated Contracting States: DE FR NL


Date of publication of application: 17.11.1999 Bulletin 1999/46

Proprietor: Casio Computer Co., Ltd. Shibuya-ku, Tokyo (JP)

Inventor: Kanbara, Minoru, c/o Pat. Dept., Hamura R&D Center Hamura-shi, Tokyo 205-8555 (JP)

Representative: Grünecker, Kinkeldey, Stockmair & Schwanhäusser Anwaltssozietät Maximilianstrasse 58 80538 München (DE)

References cited:


Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).
Description

[0001] The present invention relates to a shift register, a display device having a driver including the shift register, and an image sensing apparatus.

[0002] In recent years, digital still cameras for recording still images are popularly used. Such a digital still camera has a liquid crystal display device functioning as a viewfinder for displaying an image sensed by an image sensing element and also functioning as a display for displaying an image recorded on an image memory.

[0003] As the liquid crystal display devices, active matrix type devices are generally used because of their wide angles of field and good response characteristics. To drive an active matrix type liquid crystal display device, a gate driver for selecting any one of gate lines formed in units of rows of pixels arranged in a matrix on a liquid crystal panel, and a drain driver for receiving a pixel signal in units of gate lines and supplying the received pixel signal to the pixel corresponding to the selected gate line through drain lines are required. Each of the gate and drain drivers is generally formed from a plurality of TFTs. Each TFT outputs a signal supplied to its drain to the source on the basis of a gate signal. The output voltage value changes depending on the voltage value of the gate signal.

[0004] Each of the gate and drain drivers is generally constituted by a multistage shift register in which a signal is sequentially transmitted from a preceding stage to the subsequent stage. However, in such a shift register, a circuit immediately before a portion where a signal is output to the next stage must have a so-called EE structure. Thus a perfect OFF resistance can hardly be obtained, so that the output voltage from each stage gradually attenuates.

[0005] Some digital still camera can arbitrarily change the direction of an image sensing lens with respect to a camera body. For example, there are cameras capable of rotating a lens unit with an image sensing lens with respect to the main body to photograph an image on the photographer side. In this case, for example, the face of a photographer can be displayed on the liquid crystal display device as a mirror image (vertically inverted image or horizontally inverted image). Conventionally, however, to display a mirror image, complex control must be performed by a controller for supplying an image to the liquid crystal display device to change the read order of image data.

[0006] In addition, to display an image freely inverted in the vertical or horizontal direction in accordance with the photographing situation on the liquid crystal display device of a digital still camera, complex control must be performed by a controller for supplying an image to change the read order of image data.

[0007] It is an object of the present invention to provide a shift register which can transmit a signal input to each stage to the next stage without attenuating the signal level and also output an output signal having a high S/N ratio, and is suitable as a driving circuit of a display device.

[0008] This is achieved by the features of the independent claims.

[0009] In particular, according to the first aspect of the present invention, there is provided a shift register having a plurality of stages, each of the stages comprising:

- a first switching circuit which has a control terminal for receiving a first or second control signal and outputs a driving signal in accordance with the first or second control signal;
- a second switching circuit which has a control terminal for receiving the driving signal and discharges a power supply voltage input through a load in accordance with input of the driving signal to this control terminal; and
- a third switching circuit which has a control terminal for receiving the driving signal and outputs a third or fourth control signal in accordance with input of the driving signal to this control terminal, or
- a first switching circuit which has a control terminal for receiving a first or second control signal and outputs a driving signal to a line in accordance with the first or second control signal;
- a second switching circuit which has a control terminal connected to the line and sets a power supply voltage input through a load to a low potential in accordance with input of the driving signal to this control terminal; and
- a third switching circuit which has a control terminal connected to the line and outputs a third or fourth control signal in accordance with input of the driving signal to this control terminal.

[0010] According to the first aspect, as the transistor characteristics (when a transistor is used as the third switching circuit), the magnitude of the voltage output from the third switching circuit is determined in accordance with the magnitude of the voltage of the driving signal input to the third control terminal of the third switching circuit. When the driving signal is input to the third switching circuit through the third control terminal, the voltage of the third or fourth control signal is stored in the accumulation capacitance between the control terminal of the third switching circuit and the terminal for outputting the third or fourth control signal. Accordingly, the potential at the control terminal increases. Hence, the potential of the third or fourth control signal output from the third switching circuit increases, and a constant voltage can be continuously held without any attenuation in shift to the next stage.

[0011] The register may comprise a fourth switching circuit for, in accordance with the power supply voltage input through the load of a predetermined stage, discharging the driving signal input to a next stage of the predetermined stage through the first switching circuit.
of the next stage. The level of the third or fourth control signal is inverted at a predetermined period. When the level of one of the first and second control signals is inverted in only part of every half period of the level inversion period of the third or fourth control signal, the fourth switching circuit can be turned off in the shift register even if one of the third and fourth control signals as the output signal from each stage goes high, so the third or fourth signal of high level can be almost directly output as the output from each stage. For this reason, the S/N ratio of the output signal can be made high.

[0012] The shift register further comprises a selection control circuit for selectively supplying an externally supplied start signal to one of a first stage and a final stage, a first driving circuit for inputting a Kth driving signal from the third switching circuit of a (K-1)th stage to the first switching circuit of a Kth stage and outputting a (K+1)th driving signal from the third switching circuit of the Kth stage to a (K-1)th stage, a second driving circuit for outputting a (K+2)th driving signal from the third switching circuit of the (K+1)th stage to the Kth stage and outputting the (K+1)th driving signal from the third switching circuit of the Kth stage to the (K-1)th stage, and a shift direction control circuit for selectively driving the first and second driving circuits. With this arrangement, a forward or reverse direction can be selected as the direction in which the third or fourth control signal is output in the shift register.

[0013] The third or fourth control signal to be output from the shift register to the display element can be sequentially output without any attenuation. Especially, a display element having a large number of scanning lines (a large number of pixels) can perform satisfactory display.

[0014] The selection driving circuit (control circuit) comprises first selection control means for selectively supplying the start signal to one of a first stage and a final stage, and second selection control means for selecting whether a selection signal received by each stage is to be shifted to an input side or an output side. With this arrangement, an image inverted with respect to a forward-direction image can be displayed without inverting output of a display signal based on an image signal input from the image sensing element or the like to the display element.

[0015] As the display element, an arbitrary display panel with pixels arranged in a matrix, e.g., a liquid crystal display panel, an electroluminescence display panel, a plasma display panel, or a field emission display panel can be selected.

[0016] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0017] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a perspective view showing the outer appearance of a digital still camera according to the first embodiment of the present invention;
FIG. 2 is a block diagram showing the circuit arrangement of the digital still camera shown in FIG. 1;
FIG. 3 is a block diagram showing the arrangement of a display section shown in FIGS. 1 and 2;
FIG. 4 is a block diagram showing the arrangement of a drain driver shown in FIG. 3;
FIG. 5 is a circuit diagram of a gate driver shown in FIG. 3;
FIG. 6 is a timing chart showing the operation of the gate driver according to the first embodiment of the present invention;
FIG. 7 is a timing chart showing the operation of a gate driver according to the second embodiment of the present invention;
FIG. 8 is a circuit diagram showing the arrangement of the gate driver of a digital still camera according to the third embodiment of the present invention;
FIG. 9 is a timing chart showing the forward-direction operation of the gate driver according to the third embodiment of the present invention;
FIG. 10 is a timing chart showing the reverse-direction operation of the gate driver according to the third embodiment of the present invention;
FIG. 11A and 11B are views showing examples of the forward-direction operation of the digital still camera according to the third embodiment of the present invention, in which FIG. 11A shows a photographing state, and FIG. 11B shows the display state of a display section according to the scanning procedure in a photographing mode and that in a display mode;
FIGS. 12A and 12B are views showing examples of the reverse-direction operation of the digital still camera according to the third embodiment of the present invention, in which FIG. 12A shows the photographing state, and FIG. 12B shows the display state of the display section according to the scanning procedure in the photographing mode and that in the display mode;
FIG. 13 is a block diagram showing the arrangement of a drain driver according to the fourth embodiment of the present invention;
FIG. 14 is a circuit diagram showing a shift register according to the fourth embodiment of the present invention;
FIG. 15 is a timing chart showing the forward-direction operation of the shift register of the drain driver according to the fourth embodiment of the present invention;
FIG. 16 is a timing chart showing the reverse-direction operation of the shift register of the drain driver according to the fourth embodiment of the present invention;
FIGS. 17A to 17D are views showing examples of
the operation of a digital still camera according to the fourth embodiment of the present invention, in which FIG. 17A shows the display state of the display section when both the gate and drain drivers operate in the forward direction, FIG. 17B shows the display state of the display section according to the scanning procedure in a photographing mode and that in a display mode when the gate driver operates in the forward direction, and the drain driver operates in the reverse direction, FIG. 17C shows the display state of the display section when both the gate and drain drivers operate in the reverse direction, and FIG. 17D shows the display state of the display section according to the scanning procedure in a photographing mode and that in the display mode when the gate driver operates in the reverse direction, and the drain driver operates in the forward direction;

FIG. 18 is a circuit diagram showing a gate driver according to the fifth embodiment of the present invention;

FIG. 19 is a circuit diagram showing a gate driver according to the sixth embodiment of the present invention;

FIG. 20 is a timing chart showing the operation of the gate driver according to the sixth embodiment of the present invention;

FIG. 21 is a circuit diagram showing a gate driver according to the seventh embodiment of the present invention;

FIG. 22 is a circuit diagram showing a shift register according to the eighth embodiment of the present invention;

FIG. 23 is a circuit diagram showing a shift register of a modification of the present invention;

FIG. 24 is a circuit diagram showing a shift register of a modification of the present invention;

FIG. 25 is a circuit diagram showing a shift register of a modification of the present invention;

FIG. 26 is a view showing an image sensing element of a modification of the embodiments of the present invention and a driving system thereof.

[0018] The embodiments of the present invention will be described below with reference to the accompanying drawings.

[0019] In the first to eighth embodiments to be described below, the present invention is applied to a digital still camera.

First Embodiment

[0020] FIG. 1 is a perspective view showing the outer appearance of a digital still camera according to the first embodiment.

[0021] As shown in FIG. 1, this digital still camera comprises a camera body 1 and a lens unit 2.

[0022] The camera body 1 has a display section 10 and a mode setting key 12a on its front side. The mode setting key 12a is used to switch between a photographing mode for photographing an image and recording it on an image memory (to be described later) and a reproduction mode for reproducing the recorded image. The display section 10 is formed from a liquid crystal display device. In the photographing mode (monitoring mode), the display section 10 functions as a viewfinder for displaying an image formed by a lens before photographing. In the reproduction mode, the display section 10 functions as a display for displaying a recorded image. The arrangement of the display section 10 will be described later in detail.

[0023] The camera body 1 has, on its upper surface, a power key 11, a shutter key 12b, a "+" key 12c, a "-" key 12d, and a serial input/output terminal 29. The power key 11 is slidably operated to power on/off the digital still camera.

[0024] The shutter key 12b is used to instruct image recording in the photographing mode and instruct determination of selected contents in the reproduction mode. The "+" and "-" keys 12c and 12d are used to select image data to be displayed on the display section 10 from image data recorded in an image memory in the reproduction mode or set recording/reproduction conditions. The serial input/output terminal 29 receives a cable for transmitting/receiving data to/from an external device (e.g., a personal computer or a printer).

[0025] The lens unit 2 has, on its back side, a lens for forming an image to be photographed. The lens unit 2 is mounted on the camera body 1 to pivot through 360° in the vertical direction about its horizontal axis.

[0026] FIG. 2 is a block diagram showing the circuit arrangement of the digital still camera shown in FIG. 1.

[0027] As shown in FIG. 2, the digital still camera comprises the display section 10, a key input section 12, a CCD (Charge Coupled Device) 21, a sample-hold circuit 22, an A/D (Analog/Digital) converter 23, a vertical driver 24, a timing generator 25, a color process circuit 26, a DMA (Direct Memory Access) controller 27, a DRAM (Dynamic Random Access Memory) 28, the serial input/output terminal 29, a recording memory 30, a CPU (Central Processing Unit) 31, an image compression/expansion circuit 32, a VRAM controller 33, a VRAM (Video Random Access Memory) 34, a digital video encoder 35, and a ROM (Read Only Memory) 36.

[0028] Of these elements, the DMA controller 27, recording memory 30, CPU 31, image compression/expansion circuit 32, VRAM controller 33, and ROM 36 are connected through a data bus 40.

[0029] The key input section 12 has the above-described mode setting key 12a, shutter key 12b, "+" key 12c, and "-" key 12d, and inputs a command according to the operations of these keys to the CPU 31.

[0030] The CCD 21 receives an image of light, which is formed by the lens, at each of a plurality of pixels arranged in a matrix and stores charges corresponding to the intensity of received light. The CPU 31 executes programs stored in the ROM 36 and controls the respective portions of the circuit. The serial input/output terminal
The image compression/expansion circuit 32 com-
ments the YUV data on the basis of, e.g., JPEG (Joint
Photographic Experts Group) and stores it in the record-
ing memory 30.

After the compressed data is stored in the re-
cording memory 30, the CPU 31 starts the timing gen-
erator 25 and color process circuit 26 again. With this
operation, the mode of the digital still camera automatic-
ally returns from the image recording mode to the mon-
itoring mode.

In the reproduction mode, in accordance with
the operations of the keys 12a to 12d of the key input
section 12, the CPU 31 causes the image compression/
expansion circuit 32 to expand compressed image data
stored in the recording memory 30. The CPU 31 also
controls the DMA controller 27 to transfer the YUV data
of one frame, which is expanded by the image compres-
sion/expansion circuit 32, from the image compression/
expansion circuit 32 to the VRAM controller 33 and write
the YUV data in the VRAM 34.

The digital video encoder 35 line-sequentially
reads out YUV data of one frame written in the VRAM
34 and generates the analog video signal Sa on the ba-
sis of the readout YUV data. The digital video encoder
35 supplies the generated analog video signal Sa to the
display section 10. When an image is photographed in
the image recording mode, compressed data is record-
ed on the recording memory 30, and the operation mode
of the digital still camera switches from the image re-
cording mode to the monitoring mode, the photo-
graphed image may be displayed on the display section
10.

The arrangement of the display section 10 shown in FIGS. 1 and 2 will be described below in detail
with reference to the block diagram of FIG. 3.

The display section 10 is constructed by a liq-
uid crystal display device and comprises a chroma cir-
cuit 111, a phase comparator 112, a level shifter 113, a
liquid crystal controller 101, a liquid crystal panel 102, a
gate driver 103, and a drain driver 104, as shown in FIG. 3.

In both the monitoring and image recording
modes, the chroma circuit 111 generates analog RGB
signals SR1, SG1, and SB1 on the basis of the analog
video signal Sa output from the digital video encoder 35.
The analog RGB signals SR1, SG1, and SB1 are sub-
ject to gamma correction in accordance with the vis-
ual characteristics of the liquid crystal panel 102. The
chroma circuit 111 also generates a common voltage
Vcom (to be described later). The chroma circuit 111 al-
so performs sync separation processing to separate a
vertical sync signal VD and a horizontal sync signal HD
from the analog video signal Sa and supplies the signals
to the phase comparator 112 and liquid crystal controller
101, respectively.

To AC-drive the liquid crystal of the liquid crys-
tal panel 102 and adjust the brightness of the image to
be displayed, the level shifter 113 inverts the polarities
of the analog RGB signals SR1, SG1, and SB1 gener-
bated by the chroma circuit 111, in units of lines or frames,
and also controls the amplitudes and outputs level-shift-

ed analog RGB signals SR2, SG2, and SB2.

[0044] The liquid crystal controller 101 incorporates an oscillation circuit and establishes vertical synchronization on the basis of the vertical sync signal VD supplied from the chroma circuit 111. The liquid crystal controller 101 forms a PLL (Phase Locked Loop) using the output from the phase comparator 112 based on a phase comparison signal CKH and establishes horizontal synchronization on the basis of the formed PLL and horizontal sync signal HD. The liquid crystal controller 101 outputs a polarity inversion control signal CKF to the level shifter 113, a control signal group DCNT to the drain driver 104, and a control signal group GCNT to the gate driver 103.

[0045] The control signal group GCNT supplied to the gate driver 103 contains signals $\Phi_1$, $\Phi_2$, $\Phi_1$, and $\Phi_2$. The control signal group DCNT contains signals $\Phi_1$, $\Phi_2$, $\Phi_1$, and $\Phi_2$. The control signal group $\Phi_1$, $\Phi_2$, $\Phi_1$, and $\Phi_2$ ($\Phi_1$ represents a logical NOT) and a start signal IN.

[0046] The liquid crystal panel 102 is an active matrix type liquid crystal panel having $(m \times n)$ pixels and formed by sealing a liquid crystal between a pair of substrates. A common electrode to which the common voltage $V_{com}$ (the value of the common voltage $V_{com}$ may be changed over time) generated by the chroma circuit 111 and subjected AC level amplification and DC level amplification is applied, is formed on one substrate.

[0047] On the other substrate of the liquid crystal panel 102, pixel electrodes corresponding to the pixels and thin-film transistors (TFTs) 102a each having a semiconductor layer formed from amorphous silicon are formed in a matrix. On the other substrate of the liquid crystal panel 102, $n$ gate lines GL1 to GLn extending between the pixel electrodes, $m$ drain lines DL1 to DLm perpendicular to the gate lines GL1 to GLn, and capacitor lines CL1 to CLn parallel to the gate lines GL1 to GLn are respectively formed. In addition, red (R), green (G), and blue (B) color filters corresponding to the analog RGB signals SR2, SG2, and SB2, respectively, are arrayed in a predetermined order on the other substrate of the liquid crystal panel 102.

[0048] FIG. 3 shows an equivalent circuit diagram of the liquid crystal panel 102. The gates, drains, and sources of the TFTs 102a are connected to the gate lines GL, drain lines DL, and pixel electrodes, respectively. A pixel capacitance 102b is formed by a pixel electrode, a common electrode, and the liquid crystal sealed between the electrodes. Display signals from drain lines DL are written in the pixel capacitances 102b through the TFTs 102a corresponding to the selected gate lines GL. The aligned states of the liquid crystal molecules forming the pixel capacitances 102b are controlled in accordance with the display signals written in the pixel capacitances 102b.

[0049] Capacitors 102c are formed by the capacitor lines CL1 to CLn, and a gate insulating film and pixel electrodes sequentially stacked on the capacitor lines CL1 to CLn. A capacitor voltage $V_{com}$ is always applied to the capacitor lines CL1 to CLn. The common voltage $V_{com}$ changeable in units of lines is always applied to all common electrodes.

[0050] The gate driver 103 is formed from a shift register having $n$ stages corresponding to the number of pixels in the vertical direction of the liquid crystal panel. The gate driver 103 sequentially selects one of the gate lines GL1 to GLn in accordance with the signals $\Phi_1$, $\Phi_2$, $\Phi_1$, and $\Phi_2$ and start signal IN contained in the control signal group GCNT supplied from the liquid crystal controller 101 and sets the selected gate line in an active state (high level). The arrangement of the gate driver 103 will be described later in detail.

[0051] As shown in FIG. 4, the drain driver comprises a shift register 104a, a level shifter 104b, a sample-hold buffer 104c, and a multiplexer 104d.

[0052] The shift register 104a has $m$ stages corresponding to the number of pixels of the liquid crystal panel 102 in the horizontal direction. The shift register 104a receives a clock signal CLK, an inverted clock signal $\overline{CLK}$, and a start signal IN contained in the control signal group DCNT and generates a sampling signal for sampling the analog RGB signals. The level shifter 104b converts the sampling signal into the operation level of the sample-hold buffer 104c.

[0053] The multiplexer 104d aligns the analog video signals SR2, SG2, and SB2 from the level shifter 104b in an order corresponding to the RGB alignment of pixels of the respective lines on the basis of an alignment signal AR contained in the control signal group DCNT and outputs the analog video signals SR2, SG2, and SB2. The sample-hold buffer 104c samples/holds the analog video signals SR2, SG2, and SB2 on the basis of the sampling signal from the level shifter 104b, amplifies the signals with the buffer, and outputs the signals to the drain lines DL1 to DLm.

[0054] The gate driver 103 shown in FIG. 3 will be described below in detail with reference to the circuit diagram of FIG. 5.

[0055] Each stage $RS1(i)$ ($i = 1, 2, ..., n$; $n$ is a positive integer) of the gate driver 103 has five n-channel MOS field effect thin film transistors (to be referred to as transistors hereinafter) 201, 202, 203, 205, and 206. Each of the transistors 201, 202, 203, 205, and 206 has a gate, a gate insulating film, a semiconductor layer, a source, and a drain. The semiconductor layer is formed from amorphous silicon or polysilicon and has n-type impurity regions at portions connected to the source and drain. The transistors 201, 202, 203, 205, and 206 may be formed simultaneously with the TFTs 102a of the display section 10.

[0056] Signals applied to the gate of the transistor 201 and the drain of the transistor 205 in an odd-numbered stage $RS1(i)$ ($i = 1, 3, ...$) of the gate driver 103 are different from those in an even-numbered stage $RS1(i)$ ($i = 2, 4, ...$). More specifically, in an odd-numbered stage, the signal $\Phi_1$ is applied to the gate of the transistor 201,
and the signal CK1 is applied to the drain of the transistor 205. In an even-numbered stage, the signal Φ2 is applied to the gate of the transistor 201, and the signal ¬CK1 is applied to the drain of the transistor 205.

[0057] The signal Φ1 rises when signal CK1 is at low level. The signal Φ2 rises when the signal CK1 is at high level (i.e., the signal ¬CK1 is at low level). The signals Φ1 and Φ2 alternately rise and are applied to the gate of the transistor 201 of each odd-numbered stage and the gate of the transistor 201 of each even-numbered stage, respectively.

[0058] The arrangement and function of an odd-numbered stage RS1(i) using the first stage RS1(1) as an example will be described below.

[0059] In the first stage RS1(1) of the shift register, the signal Φ1 is applied to the gate of the transistor 201, and the start signal Sd is applied to the drain of the transistor 201. A current flowing between the drain and source of the transistor 201 when the gate is ON charges line capacitances C2 and C5 formed on lines between the source of the transistor 201 and the gates of the transistors 202 and 205, respectively. The line capacitances C2 and C5 are kept at high level after the transistor 201 is turned off and until the signal Φ1 is applied to turn on the transistor 201 again.

[0060] A reference voltage Vdd is applied to the gate and drain of the transistor 203, so the transistor 203 is always ON. When the line capacitance C2 is not charged, and the transistor 202 is OFF, the reference voltage Vdd charges a line capacitance C6 formed on a line between the sources of the transistors 202 and 203 and the gate of the transistor 206. When the line capacitance C2 is charged, the transistor 202 is turned on, and a current flows between the drain and source of the transistor 202. Since the transistors 202 and 203 have an EE structure, no perfect OFF resistance is formed on the transistor 203. As a consequence, the line capacitance C6 may not be completely discharged but has a voltage sufficiently lower than a threshold voltage Vth of the transistor 206.

[0061] The signal CK1 is supplied to the gate of the transistor 205. When the signal CK1 is at high level, a line capacitance C1 formed on a line between the source of the transistor 205 and the drain of the transistor 201 of the second stage is charged. Hence, an output signal OUT1 of high level is output from an output terminal OT1 of the first stage RS1(1).

[0062] Since the signal Φ1 is at low level, and the transistor 201 is OFF, the line capacitance C5 is kept charged by the start signal Sd. When the transistor 205 outputs the signal OUT1 to the output terminal OT1, the charge in the accumulation capacitance between the gate and source of the transistor 205 increases in accordance with voltage of the signal OUT1. Along with this increase, the gate voltage of the transistor 205 rises until the current flowing between the drain and source may be saturated. As the gate voltage of the transistor 205 rises, the potential of the output signal OUT1 rises, and the transistor 205 obtains a perfect ON resistance. Hence, the level of the signal CK1 is directly output as the level of the output signal OUT1 with little attenuation. While the output signal OUT1 is being output, the signal Φ2 is applied to the gate of the transistor 201 of the next stage to charge the line capacitances C2 and C5 of the next stage. When the signal CK1 changes from high level to low level, the output signal OUT1 output from the output terminal OT1 of the first stage also goes low.

[0063] The arrangement of an even-numbered stage RS1(i) is substantially the same as that of the odd-numbered stage RS1(1) except that the signals Φ1 and CK1 are replaced with the signals Φ2 and ¬CK1, respectively. In the stages RS1(i) (both even- and odd-numbered stages) from the second stage, the output signals OUT1 to OUT(n-1) from the preceding stages are supplied to the transistors 201. As described above, since the gate voltage of the transistor 205 of each stage is saturated by the line capacitance C5 held between the transistors 201 and 205 and the signal CK1 or ¬CK1, the output signals OUT1 to OUTn do not attenuate.

[0064] The line capacitances C2 and C5 are charged through the transistor 201 of the same stage and the transistor 206 of the preceding stage when the signal Φ1 (in an odd-numbered stage) or Φ2 (in an even-numbered stage) goes high again. The discharged line capacitances C2 and C5 of each stage RS(i) are not charged again unless the signal Φ1 or Φ2 goes high in the same horizontal period in the next vertical period. Since the transistor 206 in the preceding stage is kept ON during the transistor 201 in the stage is turned on again by the signal Φ1 or Φ2 with the second high level, the line capacitance C1 between the stage and the preceding stage is kept low level state even when the signal CK1 or ¬CK1 goes high, and the output signals OUT1, OUT2, ..., output from the output terminals OT1, OT2, ..., respectively, go high one time in one vertical period 1V.

[0065] The operation of the digital still camera according to the first embodiment will be described next.

[0066] When the digital still camera is set in the photographing mode (monitoring mode or image recording mode) by the mode setting key 12a, charges are stored in each pixel of the CCD 21 in accordance with an image formed through the lens. The CCD 21 generates the electrical signal Se corresponding to the charges stored in each pixel in accordance with a driving signal supplied from the vertical driver 24 and sequentially supplies the electrical signal Se to the sample-hold circuit 22.

[0067] The analog electrical signal Se is the effective component of the electrical signal Se is input from the sample-hold circuit 22 to the A/D converter 23. The signal is converted into the digital data Sd by the A/D converter 23 and supplied to the color process circuit 26. The color process circuit 26 generates YUV data as luminance/color difference digital data from the digital data Sd and supplies the YUV data to the DMA controller 27. The DMA controller 27 sequentially writes the YUV data in the DRAM 28.
When YUV data of one frame is written, the DMA controller 27 transfers the YUV data of one frame from the DRAM 28 to the VRAM 34 through the VRAM controller 33 under the control of the CPU 31. The digital video encoder 35 line-sequentially reads out YUV data of one frame from the VRAM 34 through the VRAM controller 33 every predetermined period, generates the analog video signal Sa, and outputs it to the display section 10. At this time, the display section 10 operates as will be described later to display the image formed by the lens.

When the user operates the shutter key 12b, the transfer operation of the timing generator 25 and color process circuit 26 is stopped under the control of the CPU 31 in response to a corresponding command. The electrical signal Se of the last frame is converted into YUV data through the sample-hold circuit 22, A/D converter 23, and color process circuit 26 and written in the DRAM 28. This YUV data of this frame is input to the image compression/expansion circuit 32 by the DMA controller 27 and compressed. The compressed data is stored in the recording memory 30.

When the digital still camera is set in the reproduction mode by the mode setting key 12a, the CPU 31 controls the DMA controller 27 to transfer compressed data designated by operating the."+" key 12c or "," key 12d from the recording memory 30 to the image compression/expansion circuit 32. The compressed data is expanded by the image compression/expansion circuit 32 and written in the VRAM 34 under the control of the VRAM controller 33. The analog video signal Sa is generated by the digital video encoder 35 on the basis of the YUV data written in the VRAM 34 and output to the display section 10. At this time, the display section 10 operates as will be described later to display the recorded image selected by operating the."+" key 12c or "," key 12d.

In both the photographing and reproduction modes, in the display section 10, the analog video signal Sa is input to the chroma circuit 111 and separated by the chroma circuit 111 into the gamma-corrected analog RGB signals SR1, SG1, and SB1, vertical sync signal VD, and horizontal sync signal HD. The phase comparator 112 measures a timing in the horizontal direction on the basis of the horizontal sync signal HD from the chroma circuit 111 and the phase comparison signal CKH from the liquid crystal controller 101 and outputs a predetermined timing signal to the liquid crystal controller 101.

In accordance with the timing signal and vertical sync signal VD, the liquid crystal controller 101 outputs the control signal group DCNT to the drain driver 104, the control signal group GCNT to the gate driver 103, and the polarity inversion control signal CKF to the level shifter 113. The polarities of the analog video signals SR1, SG1, and SB1 output from the chroma circuit 111 are inverted by the level shifter 113 in units of lines or frames in accordance with the polarity inversion control signal CKF. The analog video signals SR2, SG2, and SB2 which have appropriately undergone polarity inversion are input to the drain driver 104 in accordance with the control signal group DCNT.

The control signal group GCNT generated by the liquid crystal controller 101 contains the start signal IN and signals φ1, φ2, CK1, and ¬CK1. These signals are supplied to the gate driver 103 at timings shown in a timing chart to be described later. When the start signal IN in the control signal group GCNT generated by the liquid crystal controller 101 is supplied to the gate driver 103, the gate driver 103 starts operation.

Fig. 6 is a timing chart showing the operation of the gate driver 103.

From time T0 to T1, the start signal IN of high level is supplied from the liquid crystal controller 101 to the drain of the transistor 201 of the first stage. Next, for a predetermined period between times T0 and T1, the signal φ1 rises to turn on the transistors 201 of the odd-numbered stages. The line capacitances C2 and C5 of the first stage are charged, and the signal goes high.

At this time, the potential at the gate of the transistor 202 of the first stage goes high to turn on the transistor 202 of the first stage. When the transistor 202 of the first stage is OFF, the signal at the line capacitance C6 is set at high level by the reference voltage Vdd supplied through the transistor 203 of the first stage. When the transistor 202 of the first stage is turned on, the reference voltage Vdd supplied through the transistor 203 of the first stage is grounded. More specifically, the line capacitance C6 of the first stage is discharged and the signal at the line capacitance C6 goes low to turn off the transistor 206 of the first stage.

Simultaneously, the potential at the gate of the transistor 205 of the first stage goes high to turn on the transistor 205 of the first stage. This state wherein the signals at the line capacitances C2 and C5 of the first stage are at high level, and the signal at the line capacitance C6 is at low level continues until the signal φ1 rises between times T2 and T3 to discharge the line capacitances C2 and C5 through the transistor 201 of the first stage.

At time T1, the signal CK1 goes high, and simultaneously, the signal ¬CK1 goes low. Since the transistor 205 of the first stage is ON, and the transistor 206 of the first stage is OFF, the output signal OUT1 of high level is output from the output terminal OT1 of the first stage and also supplied to the drain of the transistor 201 of the second stage. Assume that the signal CK1 of high level has a voltage VH. The gate voltage of the transistor 205 of the first stage is raised as the output signal OUT1 is boosted, and the drain current flowing to the transistor 205 of the first stage may be saturated. Hence, the output signal OUT1 rarely attenuates and has the voltage VH. The output signal OUT1 goes low when the signal CK1 goes low at time T2.

Even when the signal φ1 rises between times T0 and T1, the line capacitances C2 and C5 of odd-num-
bered stages from the third stage are not charged because no signals of high level are supplied to the drains of the transistors 201 of the odd-numbered stages from the third stage. Hence, in the odd-numbered stages from the third stage, the output signals OUT3, OUT5,... are kept at low level.

[0080] Next, for a predetermined period between times T1 and T2, the signal φ2 rises to turn on the transistors 201 of the even-numbered stages. The output signal OUT1 charges the line capacitances C2 and C5 of the second stage and goes high.

[0081] At this time, the potential at the gate of the transistor 202 of the second stage goes high to turn on the transistor 202 of the second stage. When the transistor 202 of the second stage is OFF, the signal at the line capacitance C6 is set at high level by the reference voltage Vdd supplied through the transistor 203 of the second stage. When the transistor 202 of the second stage is turned on, the reference voltage Vdd is supplied through the transistor 203 of the second stage is grounded. More specifically, the line capacitance C6 of the second stage is discharged and the signal at the line capacitance C6 goes low to turn off the transistor 202 of the second stage.

[0082] Simultaneously, the potential at the gate of the transistor 205 of the second stage goes high to turn on the transistor 205 of the second stage. This state where the signals at the line capacitances C2 and C5 of the second stage are at high level, and the signal at the line capacitance C6 is at low level continues until the signal φ2 rises between times T3 and T4 to discharge the line capacitances C2 and C5 of the second stage through the transistor 201 of the second stage and the transistor 206 of the first stage.

[0083] At time T2, the signal CK1 goes low, and simultaneously, the signal ~CK1 goes high. Since the transistor 205 of the second stage is ON, and the transistor 206 of the second stage is OFF, the output signal OUT2 of high level is output from the output terminal OT2 of the second stage and also supplied to the drain of the transistor 201 of the third stage. Assume that the signal ~CK1 of high level has the voltage VH. The gate voltage of the transistor 205 of the second stage, which is held by the line capacitance C5 of the second stage, is raised as the output signal OUT2 is boosted, and the drain current flowing to the transistor 205 of the second stage may be saturated. Hence, the output signal OUT2 rarely attenuates and has the voltage VH. The output signal OUT2 goes low when the signal CK1 goes low at time T3.

[0084] Even when the signal φ2 rises between times T1 and T2, the line capacitances C2 and C5 of the even-numbered stages from the fourth stage are not charged because no signals of high level are supplied to the drains of the transistors 201 of the even-numbered stages from the fourth stage. Hence, in the even-numbered stages from the fourth stage, the output signals OUT4, OUT6,... are kept at low level.

[0085] In a similar manner, any one of the signals of the output signal OUT1 from the output terminal OT1 of the first stage to the output signal OUTn from the output terminal OTn of the nth stage sequentially goes high and is output until time T(n+1). Any one of the gate lines GL1 to GLn is selected in correspondence with the signal of high level, of the signals from the output signals OUT1 to OUTn of high level. At time T0 of the next vertical period, the start signal IN is supplied from the liquid crystal controller 101, and the same processing as described above is repeated.

[0086] In one vertical period 1V, in stages RS1(i) whose output signal OUTi had already been set at high level, no signals of high level are supplied to the gates of the transistors 201 even when the signal φ1 or φ2 rises. More specifically, in one vertical period, the gate lines GL1 to GLn are sequentially selected one by one.

[0087] During a period (one horizontal period 1H) when one of the gate lines GL1 to GLn is selected by the gate driver 103, the drain driver 104 operates in the following manner in accordance with the control signal group DCNT generated by the liquid crystal controller 101.

[0088] The clock signal CLK is sequentially supplied from the liquid crystal controller 101. At this time, a sampling signal is transferred to each stage on the basis of the start signal IND output every gate line GL. The transferred sampling signals are converted into signals of an operation level by the level shifter 104b and sequentially output. The analog video signals SR2, SG2, and SB2 are parallely input to the multiplexer 104d, aligned in an order corresponding to the RGB alignment of pixels of the respective lines on the basis of the alignment signal AR in the control signal group DCNT, and output. The analog video signals SR2, SG2, and SB2 output from the multiplexer 104d are sequentially sampled in the sample-hold buffer 104c in accordance with the sampling signals from the level shifter 104b and parallely output to the drain lines DL1 to Dlm through the internal buffer.

[0089] The display signals supplied to the drain lines DL1 to Dlm are written in the pixel capacitances 102b through the TFTs 102a turned on in accordance with selection by the gate driver 103 and held for one horizontal period 1H.

[0090] By repeating the above operation, the display section 10 writes the display signals in the pixel capacitances 102b of the pixels of the liquid crystal panel 102. The aligned state changes depending on the aligned state of the liquid crystal molecules, so an image represented by “dark” and “bright” pixels is displayed on the liquid crystal panel 102.

[0091] As described above, according to the first embodiment, each stage RS1(i) of the gate driver 103 of the display section 10 does not have the EE structure at a portion immediately before the next stage. For this reason, the signal CK1 or ~CK1 of high level can be directly output as the output signals OUT1 to OUTn.
Since the gate voltage output to the gate lines GL1 to GLn can be output to the TFTs 102a without any attenuation, display errors based on a change in drain current of the TFTs 102a due to a change in gate voltage of the TFTs 102a can be prevented.

Second Embodiment

[0092] A digital still camera according to the second embodiment has substantially the same arrangement and outer appearance as those of the first embodiment. In the second embodiment, however, a signal CK2 is output in place of a signal ¬CK1 in a control signal group GCNT supplied from a liquid crystal controller 101 to a gate driver in the first embodiment, the signal CK2 changes from low level to high level a predetermined period after a signal CK1 changes from high level to low level, and the signal CK1 changes from low level to high level a predetermined period after the signal CK2 changes from high level to low level. The signal CK2 is supplied to the drains of transistors 205 of even-numbered stages RS1(i) (i = 2, 4, 6,..., n-1 or n) of a gate driver 103.

[0093] The operation of the digital still camera according to the second embodiment will be described below. The second embodiment is different from the first embodiment in that the liquid crystal controller 101 generates the signal CK2 as a signal contained in the control signal group GCNT, and the operation of the gate driver 103 changes because of the difference in signals contained in the control signal group GCNT.

[0094] FIG. 7 is a timing chart showing the operation of the gate driver 103 of the second embodiment.

[0095] This operation is almost the same as that of the first embodiment described with reference to the timing chart of FIG. 6. Between times T'1 and T'2, the period when the signal CK1 is at high level is shorter than one horizontal period 1H. An output signal OUT1 from the first stage also goes high only while the signal CK1 is at high level. This also applies to odd-numbered stages from the third stage.

[0096] In the second stage, the signal CK2 is supplied to the drain of the transistor 205. In the second stage, an output signal OUT2 goes high only while the signal CK2 is substantially at high level between times T'2 and T'3. This also applies to even-numbered stages RS1(i) from the fourth stage.

[0097] As described above, in the digital still camera of the second embodiment, the period when the signal is supplied to the drains of the transistors 205 of the odd- and even-numbered stages of the gate driver 103 is made shorter than one horizontal period 1H by using the signal CK2 in place of the signal ¬CK1. The selection period of gate lines GL1 to GLn by the gate driver 103 can be arbitrarily set in accordance with the high level period of the signal CK1 or CK2.

Third Embodiment

[0098] A digital still camera according to the third embodiment has substantially the same arrangement and outer appearance as those of the first embodiment except the arrangement of a gate driver 103. Accordingly, signals Φ3 and Φ4 are added to a control signal group GCNT supplied from a liquid crystal controller 101 to the gate driver 103.

[0099] FIG. 8 is a circuit diagram of the gate driver 103 of the digital still camera according to the third embodiment.

[0100] Each stage of the gate driver 103 has the same arrangement as in the first embodiment (FIG. 5) added with a transistor 207. The gate driver 103 also has a transistor 208 formed independently of the stages.

[0101] The transistor 208 is turned on when the signal Φ3 is at high level to supply a start signal IN supplied from the liquid crystal controller 101 to line capacitances C2 and C5 of a final stage RS2(n). When a signal ¬CK1 goes high, a signal OUTn at substantially the same level as that of the signal ¬CK1 is output from an output terminal OTn of the final stage RS2(n) to a gate line GLn. When the signal OUTn is output, the signal Φ4 is output to turn on the transistor 207 of a stage RS2(n-1), so the signal OUTn charges the line capacitances C2 and C5 of the preceding stage RS2(n-1). The signal Φ3 output from the liquid crystal controller 101 turns on the transistors 207 of even-numbered stages RS2(2k) (k is an integer of 1 or more), so a signal OUT(2k+1) from the subsequent odd-numbered stage RS2(2k+1) charges the line capacitances C2 and C5 of the even-numbered stage RS2(2k). The signal Φ4 output from the liquid crystal controller 101 turns on the transistors 207 of odd-numbered stages RS2(2k-1) (k is an integer of 1 or more), so a signal OUT(2k) from the subsequent even-numbered stage RS2(2k) charges the line capacitances C2 and C5 of the odd-numbered stage RS2(2k-1).

[0102] When the final stage RS2(n) is an even-numbered stage, the liquid crystal controller 101 is set to invert or phase-shift a signal CK1 in a forward-direction operation and the signal CK1 in a reverse-direction operation (to be described later) with respect to the start signal IN and invert or phase-shift the signal ¬CK1 in the forward-direction operation and the signal ¬CK1 in the reverse-direction operation. When the final stage RS2(n) is an odd-numbered stage, the liquid crystal controller 101 is set such that the signal CK1 in the forward-direction operation and the signal CK1 in the reverse-direction operation are in phase with respect to the start signal IN, and the signal ¬CK1 in the forward-direction operation and the signal ¬CK1 in the reverse-direction operation are in phase.

[0103] When keys 12a to 12d of a key input section 12 of the digital still camera of the third embodiment are selectively operated, the selection direction of gate lines GL1 to GLn by the gate driver 103 can be set. Instead of preparing these keys, the selection direction of the
The digital still camera of the third embodiment will be described below. In this embodiment, a driving operation when the final stage RS2 (n) is an even-numbered stage.

As shown in FIG. 10, signals $\Phi_1$ and $\Phi_2$ are always at low level. For this reason, the transistors 207 and 208 are always OFF. In this case, the operation of the gate driver 103 of the third embodiment will be described next with reference to the timing chart of FIG. 9.

As shown in FIG. 9, the signals $\Phi_3$ and $\Phi_4$ are always at low level. For this reason, the transistors 207 and 208 are always OFF. In this case, the operation of the gate driver 103 of the third embodiment will be substantially the same as in the first embodiment shown in FIG. 6.

The forward-direction scanning operation of the gate driver 103 of the third embodiment will be described first with reference to the timing chart of FIG. 9.

As shown in FIG. 9, the signals $\Phi_3$ and $\Phi_4$ are alternately supplied to a multiplexer 104d. The analog RGB signals SR2, SG2, and SB2 output from the multiplexer 104d are sequentially received by a sample-hold buffer 105, analog RGB signals SR2, SG2, and SB2 are sequentially supplied to a sample-hold circuit 22 as the effective components of respective pixels are output from a sample-hold circuit 22 in the same order as that of scanning.

In the display section 10, analog RGB signals SR2, SG2, and SB2 generated on the basis of an analog video signal $Sa$ supplied from a digital video encoder 35, and level-shifted by a level shifter 113 are sequentially supplied to a multiplexer 104d. The analog RGB signals SR2, SG2, and SB2 output from the multiplexer 104d are sequentially received by a sample-hold buffer 105; analog RGB signals are sequentially supplied to the drain lines DL1 to DLm every horizontal period 1H.

On the other hand, the gate driver 103 sequentially selects the gate lines GL1, GL2, ..., GLn in the order named from the upper side to the lower side, as shown in FIG. 11B, in accordance with the control signal group GCNT from the liquid crystal controller 101. With this operation, the liquid crystal panel 102 is driven to display an image in the same direction as that of the photographed image, as shown in FIG. 11B.

The operation of the digital still camera when the image of an object, e.g., the photographer himself/herself on the display section 10 side is to be photographed, as shown in FIG. 12A, will be described next. In this case, the photographer photographs the image while setting a lens 2a of the lens unit 2 on the same side as that of a display section 10 of the camera body 1, i.e., pivoting the lens unit 2 to make an angle of almost 0° with the camera body 1. The keys 12a, 12b, 12c, and 12d of the key input section 12 are operated in this state to set the scanning direction of the gate lines GL1 to GLn by the gate driver 103 to the forward direction. At this time, pixels P(1,1) to P(n,m) of the liquid crystal panel 102 are arranged along the original vertical and horizontal directions of the liquid crystal panel 102, as shown in FIG. 11A.

In this state, the vertical direction of the lens unit 2 matches the vertical direction of the image. For this reason, a CCD 21 is driven by a vertical driver 24 such that charges corresponding to the image formed through the lens 2a of the lens unit 2 are received by the pixels of the CCD 21 while horizontally scanning the image from the left to the right and vertically scanning it from the upper side to the lower side of FIG. 11A.

Electrical signals $Se'$ as the effective components of respective pixels are output from a sample-hold circuit 22 in the same order as that of scanning.
horizontally scanning the image from the right to the left and vertically scanning it from the lower side to the upper side of FIG. 12A. Hence, the vertical and horizontal directions of charges to be received by the pixels of the CCD 21 in accordance with the image formed through the lens 2a of the lens unit 2 are reversed. In the display section 10, when the analog video signal Sa is supplied from the liquid crystal controller 101 to the drain driver 104'. The circuit arrangement of a digital still camera of the fourth embodiment is different from that of the first or third arrangement in a drain driver 104. The drain driver 104' is shown in FIG. 13. Accordingly, signals φ1, φ2, φ3 and φ4 are added to a control signal group DCNT supplied from a liquid crystal controller 101 to the drain driver 104'.

[0123] A shift register 104a' of the fourth embodiment has m stages, as shown in FIG. 14. Each stage rs1(i) (i = 1, 2, ..., m) has substantially the same arrangement as that of the gate driver 103 in FIG. 8.

[0124] The digital still camera according to the fourth embodiment has, in a key input section 12, a key for switching the selection direction of gate lines GL1 to GLn by a gate driver 103 and a key for setting the selection direction of drain lines DL1 to DLm by the drain driver 104'.

[0125] The operation of the digital still camera of the fourth embodiment will be described below.

[0126] The digital still camera of the fourth embodiment is different from that of the third embodiment only in the operation of the shift register 104a'. A clock signal CLK and an inverted clock signal ¬CLK supplied from the liquid crystal controller 101 are sequentially received in the forward direction (from out1 to outm) or reverse direction (from outm to out1) in accordance with setting.

[0127] The forward-direction operation of the shift register 104a' of the fourth embodiment will be described first with reference to the timing chart of FIG. 15.

[0128] As shown in FIG. 15, the signals φ3 and φ4 are always at low level. For this reason, transistors 307 and 308 are always OFF. In this case, the operation of the shift register 104a' is substantially the same as the forward-direction operation of the gate driver 103 of the third embodiment when the signals φ1, φ2, CK1, and ¬CK1 and start signal IN described in association with the gate driver 103 of the third embodiment are replaced with the signals φ1, φ2, CLK1 and ¬CLK1 and start signal IND of the drain driver 104', respectively, and one vertical period 1V in FIG. 6 is replaced with one horizontal period 1H. That is, drive by the gate driver 103 in FIG. 6 in one vertical period 1V corresponds to drive by the shift register 104a' in one horizontal period 1H. Since transistors 301 to 308 in the shift register 104a' are driven at a higher frequency than in the gate driver 103, they preferably have semiconductor layers formed from polysilicon.

[0129] The reverse-direction operation of the shift register 104a' of the fourth embodiment will be described next with reference to the timing chart of FIG. 16.

[0122] The circuit arrangement of a digital still camera of the fourth embodiment is different from that of the first or third arrangement in a drain driver 104. The drain driver 104' is shown in FIG. 13. Accordingly, signals φ1, φ2, φ3 and φ4 are added to a control signal group DCNT supplied from a liquid crystal controller 101 to the drain driver 104'.

[0130] As shown in FIG. 16, the signals φ1 and φ2 are always at low level. For this reason, the transistors 307 and 308 are always OFF. In this case, the operation of the shift register 104a' is substantially the same as the reverse-direction operation of the gate driver 103 of the third embodiment when the signals φ3, φ4, CK1, and ¬CK1 and start signal IN described in the third embodiment are replaced with the signals φ3, φ4, CLK1, and ¬CLK1 and start signal IND, respectively, and one vertical period is replaced with one frame period as in the forward-direction operation.

[0131] The operation of the digital still camera of the third embodiment will be described below using a specific example. In this case, a mode setting key 12a is set
in the photographing mode, and photographing is executed in the state shown in FIG. 12A of the third embodiment. At this time, display signals similar to those in FIG. 12B of the third embodiment are supplied to a display section 10.

[0132] A case wherein the user operates keys 12a, 12b, 12c, and 12d of the key input section 12 to set the scanning direction of the gate lines GL1 to GLn by the gate driver 103 in the forward direction, and the scanning direction of the drain lines DL1 to DLm by the drain driver 104 in the forward direction will be described.

[0133] In this case, the operations of the gate driver 103 and drain driver 104 are substantially the same as those in FIG. 12B of the third embodiment, and an image shown in FIG. 17A is displayed on a liquid crystal panel 102.

[0134] When a lens 2a of a lens unit 2 is set on the opposite side of the display section 10 of a camera body 1, and the user operates the keys 12a, 12b, 12c, and 12d of the key input section 12 to set the scanning direction of the gate lines GL1 to GLn by the gate driver 103 in the reverse direction, and the scanning direction of the drain lines DL1 to DLm by the drain driver 104 in the forward direction, substantially the same image as in FIG. 12B of the third embodiment is displayed, as shown in FIG. 17A. When the lens 2a of the lens unit 2 is pivoted to the same side as that of the display section 10 of the camera body 1, an image inverted along the vertical direction of FIG. 12B is displayed.

[0135] A case wherein the lens 2a of the lens unit 2 is set on the opposite side of the display section 10 of the camera body 1, and the user operates the keys 12a, 12b, 12c, and 12d of the key input section 12 to set the scanning direction of the gate lines GL1 to GLn by the gate driver 103 in the forward direction, and the scanning direction of the drain lines DL1 to DLm by the drain driver 104 in the reverse direction will be described next.

[0136] In this case, analog RGB signals SR2, SG2, and SB2 are supplied from the liquid crystal controller 101 to the gate driver 103 are received from the right to the left, as indicated by arrows in FIG. 17A. A multiplexer 104d outputs the received analog RGB signals SR2, SG2, and SB2 in the forward direction, as in FIG. 17A. Since the shift register 104a sequentially outputs a sampling signal to the drain lines in the order from DLm to DL1, a sample-hold buffer 104c receives the analog RGB signals SR2, SG2, and SB2 in the order from DLm to DL1 and supplies the signals to the drain lines DL1 to DLm every horizontal period. On the other hand, the gate driver 103 sequentially selects the gate lines GL1, GL2, ..., GLn in the order named, as shown in FIG. 17B, in accordance with a control signal group GCNT from the liquid crystal controller 101. With this operation, the liquid crystal panel 102 is driven to display an image horizontally symmetric with respect to the photographed image, as shown in FIG. 17B. That is, the photographer can see the same image as the mirror image viewed from the object side.

[0137] A case wherein the lens 2a of the lens unit 2 is set on the same side as that of the display section 10 of the camera body 1, and the user operates the keys 12a, 12b, 12c, and 12d of the key input section 12 to set the scanning direction of the gate lines GL1 to GLn by the gate driver 103 in the reverse direction, and the scanning direction of the drain lines DL1 to DLm by the drain driver 104 in the reverse direction will be described next.

[0138] In this case, the analog RGB signals SR2, SG2, and SB2 supplied from a level shifter 113 are received while being scanned along solid arrows in FIG. 17C. The drain driver 104 supplies the received analog RGB signals SR2, SG2, and SB2 to the drain lines DLm to DL1 every horizontal period 1H. On the other hand, the gate driver 103 sequentially selects the gate lines GLn, ..., GL2, GL1 in the order named, as shown in FIG. 17C, in accordance with the control signal group GCNT from the liquid crystal controller 101. With this operation, the liquid crystal panel 102 is driven to display a photographed image as shown in FIG. 17C. That is, the same image as that viewed from the photographer side can be seen from the object side.

[0139] As described above, in the digital still camera according to the fifth embodiment, by controlling the signals φ1 to φ4 supplied from the liquid crystal controller 101 to the gate driver 103, the scanning order of the gate lines GL1 to GLn can be set in either forward or reverse direction. In addition, by controlling the signals φ1 to φ4 supplied to the drain driver 104, the direction in which the shift register 104a of the drain driver 104 receives the analog RGB signals SR2, SG2, and SB2 can be set in either forward or reverse direction. Only with this arrangement, the direction of an image to be displayed on the liquid crystal panel 102 can be arbitrarily set. Hence, according to the digital still camera of the fourth embodiment, complex control need not be performed to read out image data from a frame memory, and the arrangement of the liquid crystal controller 101 for displaying an image in an arbitrary direction can be simplified.

Fifth Embodiment

[0140] A digital still camera according to the fifth embodiment has substantially the same outer appearance and circuit arrangement as in the first embodiment except the arrangement of a gate driver 103.

[0141] FIG. 18 is a circuit diagram of the gate driver 103 of the fifth embodiment.

[0142] Each stage RS3(i) (i = 1, 2, ..., n) is a positive integer) of the gate driver 103 has six transistors 201 to 206. Signals applied to the gate of the transistor 201, the gate of the transistor 204, and the drain of the transistor 205 in an odd-numbered stage RS3(i) (i = 1, 3, ...) of the gate driver 103 are different from those in an even-numbered stage RS3(i) (i = 2, 4, ...). More specifically, in an odd-numbered stage, a signal φ1 is applied to the
gate of the transistor 201, and a signal $\neg\Phi$1 is applied to the gate of the transistor 204, and a signal $\Phi$1 is applied to the drain of the transistor 205. In an even-numbered stage, a signal $\Phi$2 is applied to the gate of the transistor 201, the signal $\Phi$1 is applied to the gate of the transistor 204, and the signal $\neg\Phi$1 is applied to the drain of the transistor 205.

[0143] The signal $\Phi$1 rises when signal $\Phi$1 is at low level. The signal $\neg\Phi$1 rises when the signal $\Phi$1 is at high level. The signals $\Phi$1 and $\neg\Phi$1 alternately rise and are applied to the gate of the transistor 201 of each odd-numbered stage and the gate of the transistor 201 of each even-numbered stage, respectively.

[0144] The arrangement and function of an odd-numbered stage RS3(i) using the first stage RS3(1) as an example will be described below.

[0145] In the first stage RS3(1) of the shift register, the signal $\Phi$1 is applied to the gate of the transistor 201, and a start signal IN is applied to the drain. A current flowing between the drain and source of the transistor 201 when the gate is ON charges line capacitances C2 and C5 formed on lines between the source of the transistor 201 and the gates of the transistors 202 and 205, respectively. The line capacitances C2 and C5 are kept at high level after the transistor 201 is turned off and until the signal $\Phi$1 is applied to turn on the transistor 201 again.

[0146] A reference voltage Vdd is applied to the gate and drain of the transistor 203, so the transistor 203 is always ON. When the line capacitance C2 is not charged, and the transistor 202 is OFF, a line capacitance C6 formed on a line to the transistor 206 is charged. When the line capacitance C2 is charged, the transistor 202 is turned on, and a through current flows between the drain and source of the transistor 202. Since the transistors 202 and 203 have an EE structure, no perfect OFF resistance is formed on the transistor 203. For this reason, the line capacitance C6 may not be completely discharged but has a voltage sufficiently lower than a threshold gate voltage Vth of the transistor 206.

[0147] The signal $\Phi$1 is supplied to the drain of the transistor 205. When the signal $\Phi$1 is at high level, the signal $\neg\Phi$1 is at low level, and the transistor 204 is OFF. For this reason, a line capacitance C1 formed on a line to the drain of the transistor 201 of the second stage is charged. Hence, an output signal OUT1 of high level is output from an output terminal OT1 of the first stage RS3(1).

[0148] Since the signal $\Phi$1 is at low level, and the transistor 201 is OFF, the line capacitance C5 is kept charged by the start signal IN. When the transistor 205 outputs the signal to the output terminal OT1, the accumulation capacitance between the gate and source of the transistor 205 increases. Along with this increase, the gate voltage of the transistor 205 rises until the current flowing between the drain and source may be saturated. As the gate voltage of the transistor 205 rises, the potential of the output signal OUT1 rises, and the transistor 205 obtains a perfect ON resistance. Hence, the level of the signal $\Phi$1 is directly output as the level of the output signal OUT1 with little attenuation. While the output signal OUT1 is being output, the signal $\Phi$2 is applied to the gate of the transistor 201 of the next stage to charge the line capacitances C2 and C5 of the next stage.

[0149] When the signal $\Phi$1 changes from high level to low level, the signal $\neg\Phi$1 goes high to turn on the gate of the transistor 204. With this operation, the line capacitance C1 between the stage and the next stage is discharged sufficiently, and the output signal OUT1 from the first stage is grounded. More specifically, in the first embodiment, the signal $\Phi$1 goes low to set the output signal OUT1 at low level. In the fifth embodiment, additionally, the signal $\neg\Phi$1 output to the gate of the transistor 204 goes high to forcibly set the output signal OUT1 at low level.

[0150] The transistors 204 and 205 do not have an EE structure. When the output signal OUT1 is at high level, the transistor 205 can obtain a perfect ON resistance, and the transistor 204 can have an almost perfect OFF resistance. For this reason, the signal $\Phi$1 of high level can be directly output as the output signal OUT1.

[0151] The arrangement of an even-numbered stage RS3(i) is substantially the same as that of an odd-numbered stage RS3(1) except that the signals $\Phi$1, $\Phi$2, $\Phi$1, $\neg\Phi$1, and $\neg\Phi$1 are replaced with the signals $\Phi$2, $\Phi$1, $\Phi$1, $\neg\Phi$1, and $\neg\Phi$1, respectively. In the stages RS3(i) (both even- and odd-numbered stages) from the second stage, the output signals OUT1 to OUT(n-1) from the preceding stages are applied to the transistors 201 instead of the start signal IN.

[0152] The line capacitances C2 and C5 are discharged through the transistor 201 of the stage and the transistor 206 of the preceding stage when the signal $\Phi$1 (in an odd-numbered stage) or $\Phi$2 (in an even-numbered stage) goes high again. The discharged line capacitances C2 and C5 of each stage RS3(i) are not charged again unless the signal $\Phi$1 or $\Phi$2 goes high in the same horizontal period in the next vertical period. Since the transistor 206 in the preceding stage is kept ON during the transistor 201 in the stage is turned on again by the signal $\Phi$1 or $\Phi$2 with the second high level, the line capacitance C1 between the stage and the preceding stage is kept low level state even when the signal $\Phi$1 or $\Phi$2 goes high, and the output signals OUT1, OUT2... output from the output terminals OT1, OT2..., respectively, go high one time in one vertical period V.

[0153] The operation of the gate driver 103 of the fifth embodiment will be described below.

[0154] The digital still camera of the fifth embodiment is different from that of the first embodiment only in the operation of the gate driver 103. As a consequence, the timing chart of input/output signals to/from the gate driver 103 is the same as that shown in FIG. 6 of the first embodiment.
At high level, and the signal at the line capacitance C6 of the first stage. This state wherein the signal of the first stage goes high to turn on the transistor 205 of the first stage.

At this time, the potential at the gate of the transistor 202 of the first stage goes high to turn on the transistor 202 of the first stage. When the transistor 202 of the first stage is OFF, the signal at the line capacitance C6 is set at high level by the reference voltage Vdd supplied through the transistor 203 of the first stage. When the transistor 202 of the first stage is turned on, the reference voltage Vdd supplied through the transistor 203 of the first stage is grounded. The line capacitance C6 of the first stage is discharged and the signal at the line capacitance C6 goes low to turn off the transistor 206 of the first stage.

In addition, the potential at the gate of the transistor 205 of the first stage goes high to turn on the transistor 205 of the first stage. This state wherein the signal at the line capacitances C2 and C5 of the first stage is at high level, and the signal at the line capacitance C6 is at low level continues until the signal φ1 rises again between times T2 and T3 to discharge the line capacitances C2 and C5 through the transistor 201 of the first stage.

At time T1, the signal CK1 goes high, and simultaneously, the signal φ1 goes low. With this operation, the transistor 204 of the first stage is turned off, and the signal CK1 of high level is supplied to the drain of the transistor 205 of the first stage. Since the transistor 205 of the first stage is ON, the transistor 204 of the first stage goes OFF, and the transistor 206 of the first stage is OFF. The output signal OUT1 of high level is output from the output terminal OT1 of the first stage and also supplied to the drain of the transistor 201 of the second stage. The output signal OUT1 is kept at high level until the signal φ1 goes high at time T2 to turn on the transistor 204 of the first stage. Assume that the signal CK1 of high level has a voltage VH. The gate voltage of the transistor 205 of the first stage is raised as the output signal OUT1 is boosted, and the drain current flowing to the transistor 205 of the first stage may be saturated. Hence, the output signal OUT1 largely attenuates and has the voltage VH.

Even when the signal φ1 rises between times T0 and T1, the line capacitances C2 and C5 of odd-numbered stages from the third stage are not charged because no signals of high level are supplied to the drains of the transistors 201 of the odd-numbered stages from the third stage. Hence, in the odd-numbered stages from the third stage, the output signals OUT3, OUT5,... are kept at low level.

Next, for a predetermined period between times T1 and T2, the signal φ2 rises to turn on the transistors 201 of the even-numbered stages. With this operation, the line capacitances C2 and C5 of the second stage are charged, and the signal goes high.

At this time, the potential at the gate of the transistor 202 of the second stage goes high to turn on the transistor 202 of the second stage. When the transistor 202 of the second stage is OFF, the signal at the line capacitance C6 is set at high level by the reference voltage Vdd supplied through the transistor 203 of the second stage. When the transistor 202 of the second stage is turned on, the reference voltage Vdd supplied through the transistor 203 of the second stage is grounded. The line capacitance C6 of the second stage is discharged and the signal at the line capacitance C6 goes low to turn off the transistor 206 of the second stage.

Simultaneously, the potential at the gate of the transistor 205 of the second stage goes high to turn on the transistor 205 of the second stage. This state wherein the signal at the line capacitances C2 and C5 of the second stage is at high level, and the signal at the line capacitance C6 is at low level continues until the signal φ2 rises between times T3 and T4 to discharge the line capacitances C2 and C5 of the second stage through the transistor 201 of the second stage and the transistor 206 of the second stage.

At time T2, the signal φ1 goes low, and simultaneously, the signal φ1 goes high. With this operation, the transistor 204 of the second stage is turned off, and the signal φ1 of high level is supplied to the drain of the transistor 205 of the second stage. The transistor 205 of the second stage is OFF, and the transistor 206 of the second stage is OFF. The output signal OUT2 of high level is output from the output terminal OT2 of the second stage and also supplied to the drain of the transistor 201 of the second stage. The output signal OUT2 is kept at high level until the signal CK1 goes high at time T3. Assume that the signal CK1 of high level has the voltage VH. The gate voltage of the transistor 205 of the second stage is raised as the output signal OUT2 is boosted, and the drain current flowing to the transistor 205 of the second stage may be saturated. Hence, the output signal OUT2 rarely attenuates and has the voltage VH.

Even when the signal φ2 rises between times T1 and T2, the line capacitances C2 and C5 are not charged because no signals of high level are supplied to the drains of the transistors 201 of the even-numbered stages from the fourth stage. Hence, in the even-numbered stages from the fourth stage, the output signals OUT4, OUT6,... are kept at low level.

In a similar manner, one of the output signal OUT1 from the output terminal OT1 of the first stage to the output signal OUTn from the output terminal OTn of the nth stage sequentially goes high and is output until time T(n+1). The gate lines GL1 to GLn are selected in correspondence with the output signals OUT1 to OUTn of high level. At time T0 of the next vertical period, the start signal IN is supplied from the liquid crystal control-
The operation of the gate driver 103 will be described with reference to the timing chart of FIG. 6. Between times T'1 and T'2, the period when the signal CK1 is at high level is shorter than one horizontal period 1H. An output signal OUT1 from the first stage also goes high only while the signal CK1 is at high level. This also applies to odd-numbered stages from the third stage.

In the second stage, the signal CK2 is supplied to the drain of the transistor 205, and the signal —CK2 is supplied to the gate of the transistor 204. The period when the signal CK1 is at high level is shorter than one horizontal period 1H. In the second stage, an output signal OUT2 goes high while the signal CK2 is at high level between times T'2 and T'3. This also applies to even-numbered stages RS4(i) from the fourth stage.

As described above, in the digital still camera of the sixth embodiment, the period when the signals are supplied to the gates of the transistors 204 and the drains of the transistors 205 of the odd- and even-numbered stages of the gate driver 103 is made shorter than one horizontal period 1H by using the signals CK1 and CK2 (and their inverted signals). When the period when the signal CK1 or CK2 is set at high level is changed, the selection period of gate lines GL1 to GLn by the gate driver 103 can be arbitrarily selected.

Seventh Embodiment

A digital still camera according to the seventh embodiment has substantially the same outer appearance and circuit arrangement as in the third embodiment except the arrangement of a gate driver 103.

FIG. 21 is a circuit diagram of the gate driver 103 of the digital still camera of the seventh embodiment.

Each stage of the gate driver 103 has the same arrangement as in the fifth embodiment (FIG. 18) added with a transistor 207. The gate driver 103 also has a transistor 208 formed independently of the stages.

The transistor 208 is turned on when a signal φ3 is at high level to supply a start signal IN supplied from a liquid crystal controller 101 to line capacitances C2 and C5 of a final stage RS5(n). When a signal —CK1 goes high, a signal OUTn at substantially the same level is supplied to the gate of the transistor 204 in place of the signal CK2, and the signal CK2 is supplied to the drain of the transistor 205 in place of the signal —CK1.

The operation of the digital still camera according to the sixth embodiment will be described below.

The digital still camera of this embodiment is different from that of the first embodiment only in the operation of the gate driver 103 shown in FIG. 19. The operation of the gate driver 103 of the sixth embodiment will be described with reference to the timing chart of FIG. 20.

This operation is almost the same as that of the first embodiment described with reference to the timing chart of FIG. 6. Between times T'1 and T'2, the period when the signal CK1 is at high level is shorter than one horizontal period 1H. An output signal OUT1 from the first stage also goes high only while the signal CK1 is at high level. This also applies to odd-numbered stages from the third stage.

In the second stage, the signal CK2 is supplied to the drain of the transistor 205, and the signal —CK2 is supplied to the gate of the transistor 204. The period when the signal CK1 is at high level is shorter than one horizontal period 1H. In the second stage, an output signal OUT2 goes high while the signal CK2 is at high level between times T'2 and T'3. This also applies to even-numbered stages RS4(i) from the fourth stage.

As described above, in the digital still camera of the sixth embodiment, the period when the signals are supplied to the gates of the transistors 204 and the drains of the transistors 205 of the odd- and even-numbered stages of the gate driver 103 is made shorter than one horizontal period 1H by using the signals CK1 and CK2 (and their inverted signals). When the period when the signal CK1 or CK2 is set at high level is changed, the selection period of gate lines GL1 to GLn by the gate driver 103 can be arbitrarily selected.

Sixth Embodiment

A digital still camera according to the sixth embodiment has substantially the same outer appearance and circuit arrangement as in the second embodiment except the arrangement of a gate driver 103. Accordingly, signals CK2 and —CK2 are added to a control signal group GCNT supplied from a liquid crystal controller 101 to the gate driver 103.

FIG. 19 is a circuit diagram of the gate driver 103 of the digital still camera according to the sixth embodiment. Each stage RS4(i) (i = 1, 2, ..., n; n is a positive integer) of the gate driver 103 has six transistors 201 to 206.

In this embodiment, the gate driver 103 is different from that of the fifth embodiment in an even-numbered stage RS4(i) (i = 2, 4, ..., n-1 or n). The signal —CK2 is supplied to the gate of the transistor 204 in place of the signal CK1, and the signal CK2 is supplied to the drain of the transistor 205 in place of the signal —CK1.

The operation of the digital still camera according to the sixth embodiment will be described below.

The digital still camera of this embodiment is different from that of the first embodiment only in the operation of the gate driver 103 shown in FIG. 19. The operation of the gate driver 103 of the sixth embodiment will be described with reference to the timing chart of
odd-numbered stages RS5(2k-1) (k is an integer of 1 or more), so a signal OUT(2k) from the subsequent even-numbered stage RS5(2k) charges the line capacitances C2 and C5 of the odd-numbered stage RS5(2k-1).

[0181] When the final stage RS5(n) is an even-numbered stage, the liquid crystal controller 101 is set to invert or phase-shift the signal CK1 in a forward-direction operation and the signal CK1 in a reverse-direction operation (to be described later) with respect to the start signal IN, and invert or phase-shift the signal ¬CK1 in the forward-direction operation and the signal ¬CK1 in the reverse-direction operation. When the final stage RS5(n) is an odd-numbered stage, the liquid crystal controller 101 is set such that the signal CK1 in the forward-direction operation and the signal CK1 in the reverse-direction operation are in phase with respect to the start signal IN, and invert or phase-shift the signal ¬CK1 in the forward-direction operation and the signal ¬CK1 in the reverse-direction operation are in phase.

[0182] The operation of the digital still camera of the seventh embodiment will be described below. The operation of the gate driver 103 of the seventh embodiment is the same as that described in the third embodiment when "as in the first embodiment" is replaced with "as in the fifth embodiment". Except this, the description is the same as in the third embodiment.

[0183] As described above, in the digital still camera of the seventh embodiment, the scanning order of gate lines GL1 to GLn can be set to be in either forward or reverse direction by controlling the signals φ1 to φ4 supplied from the liquid crystal controller 101 to the gate driver 103. Only with this arrangement, a mirror image inverted in the vertical and horizontal directions can be displayed on a liquid crystal panel 102. According to the digital still camera of the seventh embodiment, even when a display section 10 is directed to the opposite side of a lens 2a, the same object image as that viewed from the photographer side can be displayed on the display section 10. For example, when the display section 10 is directed to the same side as that of the lens 2a to display the photographer himself/herself, a mirror image can be displayed without inverting the image in the vertical direction. At this time, complex control need not be performed to read out image data from a frame memory, and the arrangement of the liquid crystal controller 101 for displaying an image in an arbitrary direction can be simplified.

Eighth Embodiment

[0184] A digital still camera according to the eighth embodiment has substantially the same outer appearance and circuit arrangement as in the fourth embodiment except the arrangement of a gate driver 103 and the arrangement of a shift register 104a' in a drain driver 104'.

[0185] In the eighth embodiment, the circuit arrangement of the gate driver 103 is the same as in the seventh embodiment (FIG. 21). The shift register 104a' has m stages, as shown in FIG. 22. Each stage rs2(i) (i = 1, 2,..., m) has substantially the same arrangement as that of the gate driver 103 in FIG. 21.

[0186] The operation of the digital still camera of the eighth embodiment will be described below. In this embodiment, when signals φ1, φ2, CK1, ¬CK1, and start signal IN are replaced with signals φ1, φ2, ckl, ¬ck1 and start signal IND, respectively, one vertical period is replaced with one horizontal period, and one horizontal period is replaced with one vertical period, the operation is substantially the same as that of the gate driver 103 of the seventh embodiment in both the forward and reverse directions.

[0187] As described above, in the digital still camera according to the eighth embodiment, by controlling the signals φ1 to φ4 supplied to the drain driver 104', the direction in which the shift register 104a' of the drain driver 104' receives the analog RGB signals SR2, SG2, and SB2 can be set in either forward or reverse direction. Only with this arrangement, the direction of an image to be displayed on the liquid crystal panel 102 can be arbitrarily set. Hence, according to the digital still camera of the fourth embodiment, complex control need not be performed to read out image data from a frame memory, and the arrangement of the liquid crystal controller 101 for displaying an image in an arbitrary direction can be simplified.

Modifications of the Embodiments

[0188] The present invention is not limited to the above first to eighth embodiments, and various changes and modifications can be made. Modifications of the first to eighth embodiments will be described below.

[0189] In the first to eighth embodiments, in each stage of the shift register 104a or 104a' of the gate driver 103 or drain driver 104 or 104', a load is generated by applying a voltage from the voltage source to the gate and drain of the transistor 203 or 303. Instead, a resistor may be used.

[0190] In the second or sixth embodiment, only the gate driver 103 has an arrangement different from that of the first or third embodiment, and the signals CK2 and ¬CK2 are supplied from the liquid crystal controller 101. The shift register 104a of the drain driver 104 of the first, second, fifth, and sixth embodiments may have the arrangement in FIG. 14. In this case, the shift register 104a outputs the output signals out1 to outm in one horizontal period 1H. Even in the gate driver 103 or shift register of the drain driver 104 which operates in both the forward and reverse directions, as described in the third, fourth, seventh, or eighth embodiment, signals may be supplied at different timings between odd- and even-numbered stages, as in the second and fifth embodiments. In the present invention, one of the above-
scribed combinations of the gate driver 103 and the shift register 104a of the drain driver 104 can be arbitrarily selected.

In the first to eighth embodiments, as elements constructing the gate driver 103 or shift register 104a or 104a', n-channel MOSFETs are used. However, p-channel MOSFETs may be used by inverting the control signals. Alternatively, field effect transistors other than MOSFETs may be used.

In the first to eighth embodiments, the gate driver 103 (including the reverse direction in the third and fourth embodiments) sequentially selects the lines without performing interfaced scanning of the gate lines GL1 to GLn. When one frame is formed from two fields of even-numbered gate line scanning and odd-numbered gate line scanning, and interfaced scanning is to be performed in one field, the circuit shown in FIG. 5, 8, 18, or 19 is formed in correspondence with each of the two fields, and the start signal is supplied to the circuit for each field to perform interfaced scanning.

In the first to eighth embodiments, the display section 10, another flat panel display device may be applied in place of the transistor 203 or 303 of each stage. Alternatively, as shown in FIG. 23, one resistance element 403 may be connected in series to all the stages, in place of the transistor 203 or 303 is arranged in each stage. However, as elements constructing the gate driver 103 or shift register 104a or 104a' of the drain driver 104 or 104', n-channel MOSFETs are used. However, p-channel MOSFETs may be used by inverting the control signals. Alternatively, field effect transistors other than MOSFETs may be used.

In the first to eighth embodiments, the display device of another apparatus (e.g., a portable finder) can be arbitrarily selected. In this case as well, when the gate driver described in the third or seventh embodiment is used, a mirror image can be displayed. When the gate driver and drain driver 104 described in the fourth or eighth embodiment are used, an image can be displayed by arbitrarily setting the vertical and horizontal directions of the image. The present invention can also be applied to, e.g., a portable terminal.

In all embodiments, the present invention can also be applied to a video camera using a liquid crystal display device as a viewfinder. In this case as well, when the gate driver described in the third or seventh embodiment is used, a mirror image inverted in the vertical direction on the image sensing signal output from the output terminal OT can be easily obtained and applied to, e.g., pattern matching for comparing a photographed image with an image stored in a memory in advance.

Claims

1. A shift register comprising a plurality of stages, the stages (RS1(i)) including:

- a first switching circuit (201) which has a first control terminal for receiving a first or second control signal and outputs a driving signal in accordance with the first or second control signal;

- a second switching circuit (202) which has a second control terminal for receiving the driving signal and discharges a power supply voltage input (Vdd) through a load in accordance with input of the driving signal to the second control terminal; and

- a third switching circuit (205) which has a third control terminal for receiving the driving signal and outputs a third or fourth control signal in accordance with input of the driving signal to the third control terminal.

2. A register according to claim 1, further comprising a fourth switching circuit (206) for, in accordance with the power supply voltage input through the load
of a predetermined stage (RS1(1), discharging the driving signal input to a next stage of the predetermined stage through said first switching circuits (201) of the next stage (RS1(2)).

3. A register according to claim 1, wherein the third or fourth control signal output from said third switching circuit (205) of a predetermined stage (RS1(1)) is output to said first switching circuits (201) of a next stage (RS1(2)) of the predetermined stage as the driving signal.

4. A register according to claim 1, wherein each said first switching circuits (201) comprises a thin film transistor having a drain for receiving the driving signal and a source for outputting the third or fourth control signal and a source for outputting the third or fourth control signal.

5. A register according to claim 1, wherein in an odd-numbered stage (RS1(2k + 1)), the control terminal of the said first switching circuit (201) is input with the first control signal, and said third switching circuit (205) is input with the third control signal, and in an even-numbered stage (RS1(2k)), the control terminal of said switching circuit (201) is input with the second control signal, and said third switching circuit (205) is input the fourth control signal.

6. A register according to claim 1, wherein a level of the third and fourth control signals is inverted at a predetermined period each other, and a level of one of the first and second control signals is inverted in only part of every half period of a level inversion period of the third or fourth control signal.

7. A register (RS2) according to claim 1, further comprising in each stage of said shift register, a fifth switching circuit (204) which has a control terminal for receiving a fifth control signal and discharges the third or fourth control signal output from said third switching circuit (205) in accordance with input of the fifth control signal.

8. A register according to claim 1, wherein the load has a load switching circuit (203) whose control terminal and drain are applied with the power supply voltage (Vdd).

9. A register according to claim 1, further comprising in an odd-numbered stage (RS2(2k+1)) if the stages of said shift register, a first reverse shift switching circuit (207) which has a control terminal for receiving a sixth control signal and outputs the third of fourth control signal output from said third switching circuit (205) of a next stage (RS2(2k+2) to the control terminal of said second switching circuit (202) of the odd-numbered stage (RS2(2k+1)) and the control terminal of said third switching circuit (205) of the odd numbered stage (RS2(2k+1)) in accordance with input of the sixth control signal, and in an even-numbered stage (RS2(2k)) of the stages of said shift register, a reverse second shift switching circuit (207) which has a control terminal for receiving a seventh control signal and outputs the third of fourth control signal output from said third switching circuit (205) of a next stage (RS2(2k+1)) to the control terminal of said second switching circuit (202) of the even-numbered stage (RS2(2k)) and the control terminal of said third switching circuit (205) of the even-numbered stage in accordance with input of the seventh control signal.

10. A register according to claim 9, wherein the third of fourth control signal output from the first reverse shift switching circuit (207) or said second reverse shift switching circuit (207) on the basis of the sixth or seventh control signal is input to the control terminal of said second switching circuit (202) of the stage and the control terminal of said third switching circuit (205) of the stage to continuously drive said second switching circuit (202) of the stage and said third switching circuit (205) of the stage after said first switching circuit (201) is turned off and until the said first switching circuit (201) is turned on again.

11. A register according to claim 1, wherein the fourth control signal corresponds to a signal obtained by inverting a level of the third control signal.

12. A register according to claim 1, further comprising a selection control circuit (208) for selectively supplying an externally supplied start signal to one of a first stage (RS2(1)) and a final stage of the stages (RS2(n)), a first driving circuit for outputting a Kth driving signal from said third switching circuit of a driving signal from said third switching circuit (205) of a (K-1)th stage to said first switching circuit (201) of the Kth stage and outputting a (K+1)th driving signal from said third switching circuit (205) of the Kth stage to the (K+1)th stage, a second driving circuit for outputting a (K+2)th driving signal from said third switching circuit of the (K+1)th driving signal from said third switching circuit (205) of the Kth stage to the (K-1)th stage, and a shift direction control circuit for selectively driving said first and second driving circuits.

13. A register according to any claims 1, to 12, wherein said first (201) to third switching circuits (205) are
formed from channel field effect transistors of the same type.

14. A display device comprising
   a shift register according to any devices 1 to 13,
   a selection driving circuit (103, 104) driven in accordance with an externally supplied start signal (IN, IND), and
   a display element (102) having a plurality of pixels arranged for display in accordance with the third or fourth control signal from said selection driving circuit (103, 104).

15. A device according to claim 14, further comprising
   A signal driving circuit (104) for supplying signal corresponding to an externally supplied image signal (SR2, SG2, SB2) to a pixel selected by said selection driving circuit (103), and
   a control circuit (101) for controlling said selection driving circuit (103) and said signal driving circuit (104).

16. A device according to claim 14 or 15, wherein said selection driving circuit (208) comprises first selection controller for selectively supplying the start signal to one of the first stage (RS2(1)) and the final stage (RS2(n)) of the stages, and second selection control means for selecting whether a selection signal received by each stage is to be shifted to a preceding stage (RS2(i)) or a next stage (RS2(i+1)).

17. A device according to any of claims 14 to 16, characterised in that said display element comprises a liquid crystal display element (102b).

18. An image sensing apparatus comprising
   an image sensing element (500) for generating an image signal corresponding to incident light,
   a control circuit (510) having a shift register driven in accordance with an externally supplied start signal, said shift register being in accordance with any of claims 1 to 13, and
   a display element (102) having a plurality of pixels and selected on the basis of the third or fourth control signal from said shift register so as to perform display in accordance with an image signal from said image sensing element (500).

19. An apparatus according to claim 18, wherein said control circuit comprises a first selection controller for selectively supplying the externally supplied start signal to one of the first stage and a final stage of the stages of said shift register, and a second selection controller for selecting whether a selection signal received by each stage is to be shifted to a preceding stage or a next stage.

20. An apparatus according to claim 19, which further comprises vertical direction setting means for setting a vertical direction of an image to be displayed on said display element,
   said first selection controller selectively supplying an externally supplied selection signal to one of the first stage and the final stage of the stages of said shift register in accordance with the vertical direction of the image, which is set by said vertical direction setting means, and
   said second selection controller selecting whether the selection signal received by each stage is to be shifted to the preceding stage or the next stage in accordance with the vertical direction of the image, which is set by said vertical direction setting means.

Patentansprüche

1. Schieberegister, das eine Vielzahl von Stufen umfasst, wobei die Stufen (RS1(i)) enthalten:

   einen ersten Schaltkreis (201), der einen ersten Steueranschluss zum Empfangen eines ersten oder zweiten Steuersignals aufweist und entsprechend dem ersten oder zweiten Steuersignal ein Ansteuersignal ausgibt;

   einen zweiten Schaltkreis (202), der einen zweiten Steueranschluss zum Empfangen des Ansteuersignals aufweist und entsprechend dem Eingang des Ansteuersignals in den zweiten Steueranschluss einen Stromversorgungsspannungs-Eingang (Vdd) über eine Last abgibt; und

   einen dritten Schaltkreis (205), der einen dritten Steueranschluss zum Empfangen des Ansteuersignals aufweist und entsprechend dem Eingang des Ansteuersignals in den dritten Steueranschluss ein drittes oder viertes Steuersignal ausgibt.

2. Register nach Anspruch 1, das des Weiteren einen vierten Schaltkreis (206) umfasst, der entsprechend dem Stromversorgungsspannungs-Eingang über die Last einer vorgegebenen Stufe (RS1(1)) den Ansteuersignalleingang an eine nächste Stufe der vorgegebenen Stufe über den ersten Schaltkreis (201) der nächsten Stufe (RS1(2)) abgibt.

3. Register nach Anspruch 1, wobei das dritte oder vierte Steuersignal, das von dem dritten Schaltkreis (205) einer vorgegebenen Stufe (RS1(1)) ausgegeben wird, an den ersten Schaltkreis (201) einer nächsten Stufe (RS1(2)) der vorgegebenen Stufe als das Ansteuersignal ausgegeben wird.
4. Register nach Anspruch 1, wobei jeder der ersten Schaltkreise (201) einen Dünnschichttransistor umfasst, der einen Drain zum Empfangen des Ansteuersignals und eine Source zum Ausgeben des Ansteuersignals hat, und jeder der dritten Schaltkreise (205) einen weiteren Dünnschichttransistor umfasst, der einen Drain zum Empfangen des dritten oder des vierten Steuersignals und eine Source zum Ausgeben des dritten oder vierten Steuersignals hat.

5. Register nach Anspruch 1, wobei:

   in einer ungeradzahligen Stufe (RS1(2k + 1)) das erste Steuersignal in den Steueranschluss des ersten Schaltkreises (201) eingegeben wird und das dritte Steuersignal in den dritten Schaltkreis (205) eingegeben wird, und

   in einer geradzahligen Stufe (RS1(2k)) das zweite Steuersignal in den Steueranschluss des Schaltkreises (201) eingegeben wird und das vierte Steuersignal in den dritten Schaltkreis (205) eingegeben wird

6. Register nach Anspruch 1, wobei:

   ein Pegel des dritten und des vierten Signals in einer vorgegebenen Periode zueinander umgekehrt wird, und

   ein Pegel des ersten und des zweiten Steuersignals in lediglich einem Teil jeder Halbperiode einer Pegelumkehrperiode des dritten oder vierten Steuersignals umgekehrt wird.

7. Register (RS2) nach Anspruch 1, das des Weiteren in jeder Stufe des Schieberegisters einen fünften Schaltkreis (204) umfasst, der einen Steueranschluss zum Empfangen eines fünften Steuersignals aufweist und das dritte oder vierte Steuersignal, das von dem dritten Schaltkreis (205) ausgegeben wird, entsprechend dem Eingang des fünften Steuersignals abgibt.

8. Register nach Anspruch 1, wobei die Last einen Lastschaltkreis (203) aufweist, an dessen Steueranschluss und Dran die Stromversorgungsspannung (Vdd) angelegt wird

9. Register nach Anspruch 1, das des Weiteren umfasst:

   in einer ungeradzahligen Stufe (RS2(2k + 1)) der Stufen des Schieberegisters einen ersten Rückschiebe-Schaltkreis (207), der einen Steueranschluss zum Empfangen eines sechsten Steuersignals aufweist und das dritte oder vierte Steuersignal, das von dem dritten Schaltkreis (205) einer nächsten Stufe (RS2(2k + 2)) ausgegeben wird, an den Steueranschluss des zweiten Schaltkreises (202) der ungeradzahligen Stufe (RS2(2k + 1)) und den Steueranschluss des dritten Schaltkreises (205) der ungeradzahligen Stufe entsprechend dem Eingang des sechsten Steuersignals ausgibt, und

   in einer geradzahligen Stufe (RS2(2k)) der Stufen des Schieberegisters einen zweiten Rückschiebe-Schaltkreis (207), der einen Steueranschluss zum Empfangen eines siebten Steuersignals aufweist und das dritte oder vierte Steuersignal, das von dem dritten Schaltkreis (205) einer nächsten Stufe (RS2(2k + 1)) ausgegeben wird, an den Steueranschluss des zweiten Schaltkreises (202) der geradzahligen Stufe (RS2(2k)) und den Steueranschluss des dritten Schaltkreises (205) der geradzahligen Stufe entsprechend dem Eingang des siebten Steuersignals ausgibt.

10. Register nach Anspruch 1, wobei das dritte oder vierte Steuersignal, das von dem ersten Rückschiebe-Schaltkreis (207) oder dem zweiten Rückschiebe-Schaltkreis (207) auf Basis des sechsten oder siebten Steuersignals ausgegeben wird, in den Steueranschluss des zweiten Schaltkreises der Stufe und den Steueranschluss des dritten Schaltkreises (205) der Stufe ausgegeben wird, um den zweiten Schaltkreis (202) der Stufe und den dritten Schaltkreis (205) der Stufe kontinuierlich anzusteuer, nachdem der erste Schaltkreis (201) abgeschaltet wurde und bis der erste Schaltkreis (201) wieder angeschaltet wird

11. Register nach Anspruch 1, wobei das vierte Steuersignal einem Signal entspricht, das gewonnen wird, indem ein Pegel des dritten Steuersignals umgekehrt wird

12. Register nach Anspruch 1, das des Weiteren umfasst:

   eine Auswahl-Steuerschaltung (208), die selektiv ein von außen zugeführtes Startsignal einer ersten Stufe (RS2(1)) oder einer abschließenden Stufe der Stufen (RS2(n)) zuführt,

   eine erste Ansteuerschaltung, die ein K-tes Ansteuersignal von dem dritten Schaltkreis eines Ansteuersignals von dem dritten Schaltkreis (205) einer (K-1)-ten Stufe an den ersten Schaltkreis (201) der K-ten Stufe ausgibt und ein (K + 1)-tes Ansteuersignal von dem dritten Schaltkreis (205) der K-ten Stufe an die (K +
1)-te Stufe ausgibt,
eine zweite Ansteuerschaltung, die ein \((K + 2)\)-tes Ansteuersignal von dem dritten Schaltkreis des \((K + 1)\)-ten Ansteuersignals von dem dritten Schaltkreis \((205)\) der K-ten Stufe an die \((K - 1)\)-te Stufe ausgibt, und

eine Schieberichtungs-Steuerschaltung, die selektiv die erste und die zweite Ansteuerschaltung ansteuert.

13. Register nach einem der Ansprüche 1 bis 12, wobei der erste \((201)\) bis dritte \((205)\) Schaltkreis aus Kanal-Feldeffekttransistoren des gleichen Typs bestehen.

14. Anzeigevorratung, die umfasst

- ein Schieberegister nach einem der Ansprüche 1 bis 13,
- eine Auswahl-Ansteuerschaltung \((103, 104)\), die entsprechend einem von außen zugeführten Startsignal \((IN, IND)\) angesteuert wird, und
- ein Anzeigeelement \((102)\) mit einer Vielzahl von Pixeln, die zur Anzeige entsprechend dem dritten oder vierten Steuersignal von der Auswahl-Ansteuerschaltung \((103, 104)\) eingerichtet sind

15. Vorrichtung nach Anspruch 14, die des Weiteren umfasst:

- eine Signal-Ansteuerschaltung \((104)\), die ein Signal, das einem von außen zugeführten Bildsignal \((SR2, SG2, SB2)\) entspricht, einem durch die Auswahl-Ansteuerschaltung \((103)\) ausgewählten Pixel zuführt, und
- eine Steuerschaltung \((101)\), die die Auswahl-Ansteuerschaltung \((103)\) und die Signal-Ansteuerschaltung \((104)\) steuert.

16. Vorrichtung nach Anspruch 14 oder 15, wobei die Auswahl-Ansteuerschaltung \((208)\) eine erste Auswahlsteuerung, die das Startsignal selektiv der ersten Stufe \((RS2(1))\) oder der abschließenden Stufe \((RS2(n))\) der Stufen zuführt, sowie eine zweite Auswahl-Steuerung umfasst, die auswählt, ob ein durch jede Stufe empfangenes Auswahlsignal zu einer vorangehenden Stufe oder einer folgenden Stufe zu verschieben ist.

17. Vorrichtung nach einem der Ansprüche 14 bis 16, dadurch gekennzeichnet, dass das Anzeigeelement ein Flüssigkristall-Anzeigeelement \((102b)\) umfasst.

18. Bilderfassungsvorratung, die umfasst:

ein Bilderfassungselement \((500)\), das entsprechend auftreffendem Licht ein Bildsignal erzeugt,
eine Steuerschaltung \((510)\), die ein Schieberegister hat, das entsprechend einem von außen zugeführten Startsignal angesteuert wird, wobei das Schieberegister einem der Ansprüche 1 bis 13 entspricht, und
ein Anzeigeelement \((102)\), das eine Vielzahl von Pixeln hat und auf Basis des dritten oder vierten Steuersignals von dem Schieberegister ausgewählt wird, um Anzeige entsprechend einem Bildsignal von dem Bilderfassungselement \((500)\) durchzuführen.

19. Vorrichtung nach Anspruch 18, wobei die Steuerung ein Schieberegister nach einem der Ansprüche 1 bis 13 umfasst, die erste Auswahl-Ansteuerung \((103, 104)\), die entsprechend einem von außen zugeführten Startsignal \((IN, IND)\) angesteuert wird, und

ein Anzeigeelement \((102)\) mit einer Vielzahl von Pixeln, die zur Anzeige entscheidend dem dritten oder vierten Steuersignal von der Auswahl-Ansteuerung \((103, 104)\) eingerichtet sind

20. Vorrichtung nach Anspruch 19, die des Weiteren eine horizontale Stellung einstellend, die erste Auswahl-Ansteuerung \((103, 104)\), die entsprechend einem von außen zugeführten Startsignal \((IN, IND)\) angesteuert wird, und

ein Anzeigeelement \((102)\) mit einer Vielzahl von Pixeln, die zur Anzeige entscheidend dem dritten oder vierten Steuersignal von der Auswahl-Ansteuerung \((103, 104)\) eingerichtet sind

Revendications

1. Registre à décalage comprenant une pluralité d'êta-

- un premier circuit de commutation \((201)\) qui
- un second circuit de commutation \((202)\), qui

These are the translations of the text from German to English. The text is a patent specification describing inventors in the field of electronics and computer science. The description includes technical details about registers, circuitry, and signal processing. The text is complex, technical, and includes specific terms and concepts related to electronics and computer architecture.
pour recevoir le signal d'activation et décharge une entrée de tension d'alimentation en énergie (Vdd) à l'intérieur d'une charge conformément l'arrivée signal d'activation à la seconde borne de commande; et
un troisième circuit de commutation (205), qui possède une troisième borne de commande pour recevoir le signal d'activation et délire un troisième ou un quatrième signal de commande conformément à une entrée du signal d'activation à la troisième borne de commande.

2. Registre selon la revendication 1, comprenant en outre un quatrième circuit de commutation (206) pour, conformément à l'entrée de tension d'alimentation en énergie par l'intermédiaire d'un étage prédéterminé (RS1(1)), décharger le signal d'activation envoyé à un étage suivant qui suit l'étage prédéterminé par l'intermédiaire dudit premier circuit de commutation (201) de l'étage suivant (RS1(2)).

3. Registre selon la revendication 1, dans lequel le troisième ou le quatrième signal de commande délivré par ledit troisième circuit de commutation (205) d'un étage prédéterminé (RS1(1)) est délivré audit premier circuit de commutation (201) d'un étage suivant (RS1(2)) qui suit l'étage prédéterminé, en tant que signal d'activation.

4. Registre selon la revendication 1, dans lequel chacun desdits premiers circuits de commutation (201) comprend un transistor à film mince comportant un drain pour recevoir le signal d'activation et une source pour délivrer le signal d'activation, et chacun desdits troisièmes circuits de commutation (205) comprend un autre transistor à film mince possédant un drain servant à recevoir le troisième ou le quatrième signal de commande, et une source pour délivrer le troisième ou le quatrième signal de commande.

5. Registre selon la revendication 1, dans lequel dans un étage portant un numéro impair (RS1(2k+1)), la borne de commande dudit premier circuit de commutation (201) reçoit un premier signal de commande, et ledit troisième circuit de commutation (205) reçoit un second signal de commande, et dans un étage portant un numéro pair (RS1(2k)), la borne de commande dudit circuit de commutation (201) reçoit le second signal de commande, et ledit troisième circuit de commutation (205) reçoit le quatrième signal de commande.

6. Registre selon la revendication 1, dans lequel les niveaux des troisième et quatrième signaux de commande sont inversés l'un l'autre pendant une période de commande prédéterminée, et un niveau de l'un des premier et second signaux de comman-
de commande dudit troisième circuit de commutation (205) de l'étage pour activer continuellement le dit second circuit de commutation (202) de l'étage et ledit troisième circuit de commutation (205) de l'étage après que ledit premier circuit de commutation (201) a été bloqué et jusqu'à ce que ledit premier circuit de commutation (201) soit à nouveau passant.

11. Registre selon la revendication 1, dans lequel le quatrième signal de commande correspond à un signal obtenu en inversant un niveau haut du troisième signal de commande.

12. Registre selon la revendication 1, comprenant en outre un circuit de commande de sélection (208) pour envoyer sélectivement un signal de démarrage délivré extérieurement à l'un d'un premier étage (RS2(1)) et d'un étage final parmi les étages (RS2(n)), un premier circuit d'activation pour délivrer un K-ème signal d'activation à partir dudit troisième circuit de commutation d'un signal d'activation depuis ledit troisième circuit de commutation (205) d'un (K-1)-ème étage jusqu'au premier circuit de commutation (201) du K-ème étage et délivrer un (K+1)-ème signal d'activation à partir dudit troisième circuit de commutation (205) du K-ème étage ou (K+1)-ème étage, un second circuit d'activation pour délivrer un (K+2)-ème signal d'activation depuis ledit troisième circuit de commutation (205) du K-ème étage au (K-1)-ème étage, et un circuit de commande de direction de décalage pour activer sélectivement lesdits premier et second circuits d'activation.

13. Registre selon l'une quelconque des revendications 1 à 12, dans lequel lesdits circuits allant dudit premier circuit (201) audit troisième circuit (205) sont formés de transistors à effet de champ à canal du même type.

14. Dispositif d'affichage comprenant un registre à décalage selon l'une quelconque des revendications 1 à 13, un circuit de commande de sélection (103,104) activé conformément à un signal de démarrage (IN, IND) délivré de l'extérieur, et un élément d'affichage (102) comportant une pluralité de pixels disposés pour l'affichage conformément aux premier à quatrième signaux de commande provenant dudit circuit de commande de sélection (103,104).

15. Dispositif selon la revendication 14, comprenant en outre un circuit d'activation de signal (104) pour délivrer un signal correspondant à un signal d'image (SR2,SG2,B2) délivré de l'extérieur à un pixel sélectionné par ledit circuit de commande de sélection (103), et un circuit de commande (101) pour commander ledit circuit d'activation de sélection (103) et ledit circuit d'activation de signal (104).

16. Dispositif selon la revendication 14 ou 15, dans lequel ledit circuit de commande de sélection (208) comprend un premier contrôleur de sélection pour délivrer sélectivement le signal de démarrage à l'un du premier étage (RS2(1)) et de l'étage final (RS2(n)) parmi les étages, et des seconds moyens de commande de sélection pour sélectionner si un signal de sélection reçu par chaque étage doit être décalé vers un étage précédent (RS2(i)) ou vers un étage suivant (RS2(i+1)).

17. Dispositif selon l'une quelconque des revendications 14 à 16, caractérisé en ce que ledit élément d'affichage comprend un élément d'affichage à cristal liquide (102b).

18. Dispositif de détection d'images, comprenant un élément de détection d'image (500) pour générer un signal d'image correspondant à une lumière incidente, un circuit de commande (510) comprenant un registre à décalage activé conformément à un signal de démarrage délivré de l'extérieur, ledit registre à décalage correspondant à l'une quelconque des revendications 1 à 13, et un élément d'affichage (102) possédant une pluralité de pixels et sélectionné sur la base du troisième ou du quatrième signal de commande provenant dudit registre à décalage de manière à exécuter un affichage conformément à un signal d'image délivré par ledit élément de détection d'image (500).

19. Dispositif selon la revendication 18, dans lequel ledit circuit de commande comprend un premier contrôleur de sélection pour envoyer sélectivement le signal de démarrage délivré de l'extérieur à l'un du premier étage et d'un étage final parmi les étages dudit registre à décalage, et un second contrôleur de sélection pour sélectionner si un signal de sélection reçu par chaque étage peut être décalé vers un étage précédent ou un étage suivant.

20. Dispositif selon la revendication 19, qui comporte en outre des moyens de réglage de direction verticale pour régler une direction verticale d'une image devant être affichée sur ledit élément d'affichage, ledit premier contrôleur de sélection envoie sélectivement un signal de sélection délivré de l'extérieur, à l'un du premier étage et de l'étage final parmi les
étages dudit registre à décalage conformément à la direction verticale de l'image, qui est réglée par les dits moyens de réglage de direction verticale, et ledit second contrôleur de sélection sélectionnant si le signal de sélection reçu par chaque étage doit être décalé vers l'étage précédent ou vers l'étage suivant conformément à la direction verticale de l'image, qui est réglée par les dits moyens de réglage de direction verticale.