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Non-contact information storage medium and data transmission method for the medium
Kontaktloses Informations-Speichermedium und Verfahren zur Datenübertragung dazu
Support d’enregistrement sans contact pour d’information et procédé de transmission de données correspondant

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This invention relates to a non-contact information storage medium according to the preamble of claim 1. More particularly, it is applicable to a medium of this type, such as a non-battery type radio card or a radio tag, and a data transmission method for the medium, used to perform communication with a data processing unit such as a card reader/writer (hereinafter simply called a "reader/writer").

In the field of information processing systems, an information processing system has recently been developed, which includes a non-contact information storage medium (such as a non-battery type radio card or a radio tag) used as, for example, an entrance/leaving management system, and an information processing unit (such as a reader/writer) for performing non-contact radio communication with the non-contact information storage medium.

The non-contact information storage medium, i.e. the non-battery type radio card or the radio tag, receives a radio wave generated through the transmission antenna of the information processing unit, i.e. the reader/writer, and simultaneously subjects a signal indicative of data stored therein to slight amplitude modulation, thereby transmitting the modulated signal to the reader/writer in the form of a transmission wave. The reader/writer receives the transmission wave from the non-battery type radio card or the radio tag, using a signal reception antenna.

More specifically, the non-contact information storage medium generally obtains power for driving its internal circuit by rectifying and smoothing a radio wave (i.e. an electromagnetic wave) from the reader/writer, using an antenna incorporated in the medium, and simultaneously transmits data stored therein, using the same antenna. To this end, the medium employs a data transmission method, such as a method for increasing a load current obtained through the antenna, or a method for changing its antenna-resonating electrostatic capacitance.

However, in the case of using, as the data transmission method, the method for increasing the load current obtained through the antenna, a great amount of load current will be lost. On the other hand, in the case of using the method for changing the antenna-resonating electrostatic capacitance, the resonance frequency of the antenna will inevitably vary. As a result, the amount of power which can be used within the non-contact information storage medium may well decrease, or the distance over which data can be transmitted may decrease. Thus, neither method is suitable for efficient data transmission between the non-contact information storage medium and the reader/writer.

A medium according to the preamble of claim 1 is known from EP 0 525 642 A2.

It is the object of the invention to provide a non-contact information storage medium capable of efficiently using power obtained via an antenna incorporated therein, keeping the resonance frequency of the antenna constant, preventing loss of power used within the medium, thereby securing a sufficient distance over which data can be transmitted, and a data transmission method used in the non-contact information storage medium.

This object is achieved by a non-contact information storage medium according to claim 1.

When the output current of the rectifier circuit, i.e., a rectifier circuit, is interrupted, it is possible that its output voltage will exceed the breakdown voltage of each circuit element. To avoid this, the modulation circuit preferably includes a voltage limiting circuit for limiting the output voltage of the rectifier circuit to a value less than a predetermined value.

Further developments of the invention are given in the dependent claims.

Further features and advantages of embodiments of the invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram, useful in explaining the subject matter of the invention:

FIG. 2 is a block diagram, showing an essential part of a first embodiment of the invention;

FIGS. 3A - 3C are views, showing waveforms generated from the essential part of the first embodiment while it operates;

FIG. 4 is a circuit diagram, showing an essential part of a second embodiment of the invention; and

FIG. 5 is a circuit diagram, showing an essential part of a third embodiment of the invention.

The embodiments of the invention will be described with reference to the accompanying drawings.

FIG. 1 is a block diagram, showing a non-contact IC card system to which the invention is applied. This system is used to store or read information in or from a memory incorporated in a non-contact IC card 106 in accordance with an instruction from a reader/writer 101.

In this system, the non-contact IC card 106 does not have a battery therein but receives power from a power transmission wave generated by the reader/writer 101. Thus, the card 106 is operated by the reader/writer operate in a non-contact manner. The present invention is directed to an improvement in data transmission means incorporated in the system for transmitting data from the non-contact IC card to the reader/writer.

FIG. 1 is a schematic view, showing an information processing system in which radio communication is performed between the reader/writer 101 and the information processing unit and the non-contact information storage medium 106 such as a non-battery type radio card. The present invention is directed, in particular, to an improvement in the non-contact information storage medium.
storage medium 106 incorporated in the system.

First, the schematic structure of the reader/writer 101 will be described with reference to FIG. 1. The reader/writer 101 has a transmission circuit 102 and a reception circuit 104, which are controlled by a host computer 100.

The transmission circuit 102 and the reception circuit 104 are connected to a transmission antenna coil 103 and a reception antenna coil 105, respectively. This enables transmission of power and data to the non-contact information storage medium 106, and reception of data from the medium.

On the other hand, the non-contact information storage medium 106 receives data and power through a transmission/reception antenna coil 107. The received power is converted into a stable DC current by means of a rectifier circuit 109, a capacitor 111 and a power smoothing circuit 112, and supplied to a control circuit 113, a memory 114, etc. incorporated in the non-contact information storage medium 106.

A wave received by the transmission/reception antenna coil 107 and including data is input via a capacitor 108. Then, the control circuit 113 subjects the received wave to a predetermined demodulation processing, and stores, in the memory 114, data extracted from the wave as a result of demodulation.

The control circuit 113 also reads data stored in the memory 114, subjects the data to predetermined processing, and supplies a modulation circuit 110 with the processing result as a transmission wave.

The present invention aims to provide a non-contact information storage medium capable of efficient data transmission and a data transmission method for the medium. To this aim, on the non-contact information storage medium 106 side, the output current of the rectifier circuit 109 is periodically reduced or interrupted, which serves as power supply means for supplying the internal circuit of the medium with a wave received by the transmission/reception antenna coil 107 and functioning as power for driving the circuit. This prevents the increase of a loss in the power obtained through the transmission/reception antenna coil 107, or a change in the resonant frequency of the antenna coil 107. As a result, the reduction of the power which can be used in the non-contact information storage medium 106, or the reduction of the distance through which data can be transmitted is prevented.

The embodiments of the invention with the above-described basic structure will be described in detail.

FIG. 2 shows an essential part of the non-contact information storage medium 106 of FIG. 1, and more specifically, a basic structure for transmitting data from the medium 106 side. FIGS. 3A - 3C show the waveforms of signals generated from elements in FIG. 2.

The output (b) (see FIG. 3B) of a rectifier circuit 209 is connected to and disconnected from a smoothing capacitor 211 side circuit by means of a switching element 210, which is controlled by transmission data from the control circuit 113. As a result, a current (c) (see FIG. 3C) occurring at an antenna coil 207 is controlled by a transmission wave (a) (see FIG. 3A) from the control circuit 113.

The transmission wave corresponds to transmission data modulated with a carrier wave which is used for radio transmission and has a predetermined frequency, and corresponds to data read from the memory 114. The frequency of the transmission wave will be described, taking, as an example, a frequency half the frequency of a radio wave from which power for driving the internal circuit is obtained (see FIG 3A). The carrier wave is formed by dividing the radio wave into two portions by means of the control circuit 113.

The switching element 210 in FIG. 2, which corresponds to the modulation circuit 107 in FIG. 1, is switched between a state in which the output current (i.e. the load current) of the rectifier circuit 209 is supplied to the smoothing capacitor side, and a state in which the supply of the output current is stopped.

FIGS. 3A - 3C show signal waveforms occurring when the switching operation is performed. As is shown in FIG. 3C, the current (c) of the antenna coil 207 contains the transmission wave (a). In other words, when the transmission wave (a) is at high level, the antenna coil current (c) has a large amplitude. The reader/writer 101 detects changes in the antenna coil current (c), thereby receiving data from the IC card.

On the basis of data from the control circuit 113, the switching element 210 as the modulation circuit 110 subjects the carrier wave to phase modulation, amplitude modulation (for example, the signal amplitude is set to a predetermined value or zero), frequency modulation, etc., thereby transmitting data.

Since the output of the rectifier circuit 209 is interrupted by the transmission wave (a) while the switching element 210 is in the non-conductive state, it appears that the efficiency of power extraction is extremely low in the non-conductive state. However, the antenna coil 207 and the capacitor 208 constitute a resonance circuit which resonates with the radio wave from which the power for the internal circuit is obtained. Therefore, a greater portion of the current is accumulated as a circulating current in the resonance circuit while the output of the rectifier circuit 209 is interrupted.

When the switching element 210 is returned to the conductive state by means of the transmission wave (a), a greater portion of the accumulated current is stored in the smoothing capacitor 211.

In the case of the conventional non-contact information storage medium, the rectifier output (b) is formed when the output of the rectifier circuit 209 flows to the earth via a resistor with a relatively low resistance, depending upon the contents of the transmission data. As a result, the antenna current is varied, thereby transmitting data. This being so, a loss in current is high at
the time of data transmission.

[0033] On the other hand, in the present invention, the loss in the output of the rectifier circuit 209 mainly includes a loss occurring in the resonance circuit of the antenna coil 207 and the capacitor 208, and little loss due to a resistor as above required in principle at the time of modulation.

[0034] Accordingly, the data transmission method for the non-contact information storage medium of the invention is characterized in that a reduction in power is extremely small when the transmission wave (a) is generated.

[0035] When the data transmission method for the non-contact information storage medium of the invention is actually used, if the distance between the IC card as the storage medium 106 and the reader/writer is short, there is a case where the power generated from the antenna coil 207 is extremely large, and an excessive voltage is applied to the rectifier circuit 209 when, in particular, the output of the circuit 209 is interrupted. This makes it difficult to provide the rectifier circuit in a semiconductor integrated circuit with a low breakdown voltage.

[0036] FIG. 4 shows an IC card according to a second embodiment, which has a structure for preventing application of an excessive voltage as above to a rectifier circuit 309. The output of the rectifier circuit 309 is compared with a reference voltage (described later) by a comparator 310f, and is made to flow to the earth via the resistors 310h and 310i when it nearly exceeds the breakdown voltage of each internal element of the circuit 309.

[0037] An antenna coil 307 and a capacitor 308 are connected parallel and constitute a parallel resonance circuit, which is connected to the rectifier circuit 309. The rectifier circuit 309 performs full-wave rectification of an AC voltage generated from the resonance circuit. The output terminal of the rectifier circuit 309 is connected to a node N1, which is connected to resistors 310d and 310b and also to the source of a p-channel MOS transistor (hereinafter simply called a "p-channel transistor") 310a. The resistor 310d is connected to a resistor 310e in series, thereby forming a voltage divider circuit. A junction therebetween provides a comparative voltage VB.

[0038] The source and gate of the p-channel transistor 310a are connected to each other via a resistor 310b. The drain of the transistor 310a is connected to a node N2. The node N2 is connected to a smoothing capacitor 311, a resistor 310h, the drain of an n-channel MOS transistor (hereinafter simply called a "n-channel transistor") 312a, and a resistor 312, for supplying them with a power supply output.

[0039] The gate of the p-channel transistor 310a is connected to a node N3, which is connected to the drains of n-channel transistors 310g and 310c. The sources of the n-channel transistors 310g and 310c are both grounded. The gate of the n-channel transistor 310c is supplied with a transmission wave from the control circuit 113.

[0040] Resistors 312d and 312e are connected in series, thereby forming a voltage divider circuit. A junction therebetween is connected to a non-inversion output terminal of a comparator 312b. The inversion input terminal of the comparator 312b is connected to the plus side of a reference voltage generating element 312c. The output of the comparator 312b is connected to the gate of the n-channel transistor 312a, and the source of the n-channel transistor 312a is grounded. The transistors 312a - 312e constitute a voltage stabilizing circuit 312. The output voltage VE of the voltage stabilizing circuit 312, i.e. the charge voltage of the smoothing capacitor 311, is kept constant.

[0041] The resistor 310h and a resistor 310l are connected in series, thereby forming a voltage divider circuit. A junction therebetween provides a reference voltage VC. The reference voltage VC is applied to the inversion input terminal of a comparator 310f, while the comparative voltage VB generated from the divider circuit consisting of the resistors 310d and 310e is applied to the non-inversion input terminal of the comparator 310f. The output of the comparator 310f is connected to the gate of the n-channel transistor 310g.

[0042] In the above-described structure, the p-channel transistor 310a, the resistor 310b and the n-channel transistor 310c constitute a switching circuit, and the resistors 310d and 310e, the n-channel transistor 310g, the comparator 310f and the resistors 310h and 310i constitute a voltage limiting circuit. The switching circuit (310a - 310c) and the voltage limiting circuit (310d - 310i) constitute a modulation circuit 310.

[0043] The operation of the circuit shown in FIG. 4 will now be described in detail.

[0044] The voltage generated at the antenna coil 207 is rectified by the rectifier circuit 309. The resistor 310b is an element for applying a bias voltage to the p-channel transistor 310a, and the n-channel transistor 310c is an element for introducing a signal for switching on and off the p-channel transistor 310a in a cycle corresponding to that of the transmission wave under the control of the control circuit 113. Thus, the p-channel transistor 310a is controlled by the transmission wave from the control circuit 113.

[0045] The rectified wave of the rectifier circuit 309 is accumulated in the smoothing capacitor 311 via the p-channel transistor 310a when the transistor 310a is in the conductive state. Further, while the transistor 310a is in the conductive state, the output voltage of the rectifier circuit 309 substantially depends upon the charge voltage of the smoothing capacitor 311. The charge voltage of the smoothing capacitor 311 is controlled at a constant value by the voltage stabilizing circuit 312.

[0046] Specifically, the resistors 312d and 312e and the reference voltage element 312c of the voltage stabilizing circuit 312 apply a comparative voltage VF and a reference voltage VG to the comparator 312b, respec-
tively. When the comparative voltage \( VF \) is lower than the reference voltage \( VG \), the output of the comparator 312b is at low level, the n-channel transistor 312a is in the non-conductive state, and the voltage \( VE \) at the node N2 is at high level. When, on the other hand, the comparative voltage \( VF \) is higher than the reference voltage \( VG \), the output of the comparator 312b is at high level, the n-channel transistor 312a is in the conductive state, and the voltage \( VE \) at the node N2 is at low level. Thus, the voltage stabilizing circuit 312 keeps the voltage \( VE \) at the node N2 constant.

[0047] While the p-channel transistor 310a is in the non-conductive state, no load is applied to the rectifier circuit 309 and hence the output voltage \( VA \) of the circuit 309 increases. At this time, the comparator 310f compares the voltage \( VB \) obtained by dividing the output voltage of the circuit 309 by the resistors 310d and 310e, with the voltage \( VC \) obtained by dividing the charge voltage of the smoothing capacitor 311 by the resistors 310h and 310i. When the voltage \( VB \) is higher than the voltage \( VC \), the output voltage \( VD \) of the comparator 310f is at high level. Accordingly, the n-channel transistor 310g is in the on-state, which means that the p-channel transistor 310a is in the conductive state and the output voltage \( VA \) of the rectifier circuit 309 is at low level.

[0048] On the other hand, when the voltage \( VB \) is higher than the voltage \( VC \), the output voltage \( VD \) of the comparator 310f is at low level. Accordingly, the n-channel transistor 310g is in the conductive state and the output voltage \( VA \) of the rectifier circuit 309 is at high level. Thus, the transistor 310g repeatedly turns on and off, thereby controlling the output voltage \( VA \) of the rectifier circuit 309 within a predetermined range.

[0049] The p-channel transistor 310a as the switching element is set in the non-conductive state in a cycle corresponding to that of the transmission wave. The maximum value of the output voltage \( VA \) of the rectifier circuit 309 can be set at an optimal value by adjusting the resistance ratio of the resistor 310d to the resistor 310e of one divider circuit and that of the resistor 310h to the resistor 310i of the other divider circuit.

[0050] FIG. 5 shows the circuit structure of a third embodiment of the invention. In this circuit, the power supply voltage smoothed by a smoothing capacitor 411 is accumulated in another capacitor 410i. The voltage accumulated in the capacitor 410i is added to the smoothed power supply voltage when the output current of the rectifier circuit 409 is interrupted, thereby generating a voltage for driving the switching element 410a. This circuit is constructed such that the voltage for driving the switching element 410a will not exceed a value twice the smoothed power supply voltage, thereby preventing the output voltage of the rectifier circuit 409 from exceeding a predetermined value.

[0051] An antenna coil 407 and a capacitor 408 are connected parallel to each other and constitute a parallel resonance circuit. This parallel resonance circuit is connected to the rectifier circuit 409 for performing full-wave rectification of the AC voltage generated in the resonance circuit. The output terminal of the rectifier circuit 409 is connected to a node N10, which is connected to resistors 410e, 410b and the source of a p-channel transistor 410a as a switching element. The other end of the resistor 410e is connected to a node N11, which is connected to the gate of a p-channel transistor 410d and the drain of an n-channel transistor 410f. The gate of the n-channel transistor 410f is supplied with a transmission wave via an inverter 410m, and the source thereof is grounded.

[0052] The other end of the resistor 410b is connected to a node N12, which is connected to the gate of an n-channel transistor 420c and the drain of an n-channel transistor 410d. The gate of the n-channel transistor 410d is supplied with the transmission wave via the inverter 410m and an inverter 410c, and the source thereof is grounded.

[0053] The drain of the p-channel transistor 410a serving as a switching element is connected to a node N15, which is connected to the sources of p-channel transistors 410g and 410j, the smoothing capacitor 411, the drain of an n-channel transistor 412a, and a resistor 412b, and provides the power supply voltage. Resistors 412d and 412e are connected in series, thereby forming a voltage divider circuit. A junction therebetween is connected to a non-inversion input terminal of a comparator 412b. The inversion input terminal of the comparator 412b is connected to the plus side of a reference voltage generating element 412c. The output of the comparator 412b is connected to the gate of the n-channel transistor 412a, and the source of the n-channel transistor 412a is grounded. The transistors 412a - 412e constitute a voltage stabilizing circuit 412. The output voltage \( VI \) of the voltage stabilizing circuit 412, i.e., the charge voltage of the smoothing capacitor 411, is kept constant.

[0054] The gate of the p-channel transistor 410j is connected to a node N16, which is connected to the gate of the n-channel transistor 410k, the output terminal of the inverter 410m, the input terminal of the inverter 410c, and the gate of the n-channel transistor 410f. The drain of the p-channel transistor 410j is connected to a node N17, which is connected to the drain of the n-channel transistor 410k and one of the terminals of the capacitor 410i. The source of the n-channel transistor 410k is grounded.

[0055] The other terminal of the capacitor 410i is connected to a node N13, which is connected to the drain of the p-channel transistor 410g and the source of the p-channel transistor 410h. The drain of the p-channel transistor 410h is connected to a node N14, which is connected to the drain of the n-channel transistor 410c and the gate of the p-channel transistor 410a. The source of the n-channel transistor 410c is grounded.

[0056] In the structure of FIG. 5, the p-channel transistor 410a, the resistor 410b, the n-channel transistors
410c and 410d constitute a switching circuit, while the resistor 410e, the n-channel transistor 410f, the p-channel transistors 410g and 410h, the capacitor 410i, the p-channel transistor 410j, the n-channel transistor 410k and the inverters 410c and 410m constitute a voltage limiting circuit. The switching circuit (410a - 410d) and the voltage limiting circuit (410e - 410m) constitute a modulation circuit 410.

[0057] The operation of the circuit shown in FIG. 5 will now be described.

[0058] First, the voltage generated at the antenna coil 407 is rectified by the rectifier circuit 409. The voltage rectified by the rectifier circuit 409 is accumulated in the smoothing capacitor 411 via the p-channel transistor 410a when the transistor 410a is in the conductive state. Further, while p-channel transistor 410a is in the conductive state, the output voltage of the rectifier circuit 409 substantially depends upon the charge voltage of the smoothing capacitor 411. The charge of the smoothing capacitor 411 is controlled at a constant value by the voltage stabilizing circuit 412.

[0059] Specifically, the resistors 412d and 412e and the reference voltage element 412c of the voltage stabilizing circuit 412 apply a comparative voltage VJ and a reference voltage VK to the comparator 412b, respectively. When the comparative voltage VJ is lower than the reference voltage VK, the output of the comparator 412b is at high level, the n-channel transistor 410a is in the off-state, and the voltage VI at the node N15 is at low level. Thus, when the transmission wave from the control circuit 113 is at low level, the p-channel transistor 410h in the on-state, the n-channel transistor 410g in the off-state.

[0060] On the other hand, when the transmission wave is at high level, the p-channel transistor 410a is in the non-conductive state by the transmission wave from the control circuit 113, an increase in the output voltage VH of the rectifier circuit 409 can be optimally controlled by setting the gate voltage of the p-channel transistor 410a at a value substantially equal to twice the charge voltage of the smoothing capacitor 411. In other words, when the p-channel transistor 410a is in the non-conductive state, the output voltage VH of the rectifier circuit 409 is kept at a voltage obtained by adding the threshold voltage of the p-channel transistor 410a to the voltage (2 × VI).

[0061] Thus, when the transmission wave is at high level, the p-channel transistor 410a is in the non-conductive state. Since there is no load on the rectifier circuit 409 in the non-conductive state, its output voltage VH is kept at high level. At this time, a voltage obtained by adding the charge voltage of the capacitor 410i to the charge voltage VI of the smoothing capacitor 411 is applied to the gate of the p-channel transistor 410a via the p-channel transistor 410h. In other words, a voltage substantially equal to twice the voltage VI is applied to the gate of the p-channel transistor 410a.

[0062] As described above, during the time when the p-channel transistor 410a is kept in the non-conductive state by the transmission wave from the control circuit 113, an increase in the output voltage VH of the rectifier circuit 409 can be optimally controlled by setting the gate voltage of the p-channel transistor 410a at a value substantially equal to twice the charge voltage of the smoothing capacitor 411. In other words, when the p-channel transistor 410a is in the non-conductive state, the output voltage VH of the rectifier circuit 409 is kept at a voltage obtained by adding the threshold voltage of the p-channel transistor 410a to the voltage (2 × VI).

[0063] In summary, the present invention provides a non-contact information storage medium capable of data transmission with only a small loss in the power obtained from an electromagnetic wave applied thereto from the outside, and a data transmission method employed therein.

[0064] Moreover, the present invention provides a cheap non-contact information storage medium with a circuit which is designed to limit the voltage input through its antenna and hence is constituted of elements with low breakdown voltages, and also a data transmission method employed therein.

Claims

1. A non-contact information storage medium for receiving power from a radio wave applied to the medium from the outside, and transmitting data in the form of a transmission wave to the outside, comprising

- at least one antenna (207, 307, 407) for obtaining the power from the radio wave applied thereto from the outside of the medium;
- a rectifier circuit (209, 309, 409) for converting the power obtained by the antenna (207, 307, 407) into an output current as power for a circuit incorporated in the medium,
- a smoothing capacitor (211, 311, 411) for accumulating the output current of the rectifier circuit (209, 309, 409) and smoothing an output voltage thereof, and
a voltage stabilizing circuit (212, 312, 412) connected to the smoothing capacitor (211, 311, 411), for keeping at a constant value a charge voltage of the smoothing capacitor (211, 311, 411),
characterized by
a switching circuit (210, 310a-c, 410a-d), connected to an output of the rectifier circuit (209, 309, 409) and the smoothing capacitor (211, 311, 411) in series, for switching on and off a current path from the rectifier circuit to the smoothing capacitor in accordance with the transmission wave.

2. The medium according to claim 1, further comprising a voltage limiting circuit (310d-310i; 410e-401m), for limiting an output voltage of the rectifier circuit (209) to a value less than a predetermined value when the current path from the rectifier circuit is switched off by the switching circuit (210, 310a-310c, 410a-410d).

3. The medium according to claim 2, characterized in that the switching circuit includes
a p-channel transistor (310a) having a source connected to an output of the rectifier circuit, a drain connected to the smoothing capacitor, and a gate connected to the source via a resistor, and
an n-channel transistor (310c) having a drain connected to the gate of the p-channel transistor (310a), a source grounded, and a gate for receiving the transmission wave.

4. The medium according to one of claims 1 to 3, wherein the voltage stabilizing circuit includes
an n-channel transistor (312a) having a drain connected to the smoothing capacitor (311), a grounded source, and a gate,
a voltage divider circuit (312d, 312e) for dividing a charge voltage of the smoothing capacitor to provide a divided voltage,
a reference voltage generating circuit (312c) for generating a reference voltage, and
a comparator (312b) having an input for receiving the divided voltage from the voltage divider circuit, another input for receiving the reference voltage from the reference voltage generating circuit, and an output connected to the gate of the n-channel transistor (312a).

5. The medium according to one of claims 2 to 4, characterized in that the voltage limiting circuit includes
an n-channel transistor (310g) having a drain connected to the gate of the p-channel transistor 310a, and a source grounded, and a gate,
a first voltage divider circuit (310h, 310i) for dividing a charge voltage of the smoothing capacitor to provide a first divided voltage,
a second voltage divider circuit (310d, 310e) for dividing the output voltage of the rectifier circuit to provide a second divided voltage, and
a comparator (310f) having an input for receiving the first divided voltage, another input for receiving the second divided voltage, and an output connected to the gate of the n-channel transistor (310g).

6. The medium according to claim 2, characterized in that the voltage limiting circuit includes
a control voltage generating circuit (410i) for generating a control voltage (2·VI) corresponding to the predetermined value, and a voltage control circuit (410h) for controlling the output voltage of the rectifier circuit using the control voltage.

7. The medium according to claim 6, wherein the switching circuit includes a p-channel MOS transistor 410a having a source connected to an output of the rectifier circuit, a drain connected to the smoothing capacitor 411 and a gate, and the voltage control circuit 410h controls the output voltage of the rectifier circuit by supplying the control voltage to the gate of the p-channel MOS transistor.

8. The medium according to claim 6 or 7, wherein the control voltage generating circuit (410i) includes a booster capacitor (410i) which is charged up to a charge voltage of the smoothing capacitor during the time when the rectifier circuit is connected to the smoothing capacitor (411) via the switching circuit (410a-d), and generates, when the rectifier circuit (409) is disconnected from the smoothing capacitor (411), a voltage substantially twice the charge voltage of the smoothing capacitor by adding to the charge voltage of the smoothing capacitor (411) a charge voltage applied to the booster capacitor (410i) during the time when the rectifier circuit (409) is connected to the smoothing capacitor (411).

9. The medium according to claim 1, further comprising current control means, for controlling, in accordance with a control voltage, a charging current flowing from the rectifier circuit to the smoothing capacitor, another capacitor for accumulating an electric charge of the smoothing capacitor, and means for adding a charge voltage of the another capacitor to the charge voltage of the smoothing capacitor when the output current of the rectifier circuit is interrupted, thereby providing the current control means with an addition result as the control voltage.
Patentansprüche

1. Kontaktloses Informationsspeichermedium zum Empfangen von Leistung über eine Funkwelle, die an das Medium von außerhalb angelegt wird, und zum Übertragen von Daten in der Form einer Übertragungswelle an die Außenwelt, mit

mindestens einer Antenne (207, 307, 407) zum Erhalten der Leistung von der Funkwelle, die an diese von außerhalb des Mediums angelegt wird,
einer Gleichrichterschaltung (209, 309, 409) zum Wandeln der über die Antenne (207, 307, 407) erhaltenen Leistung in einen Ausgangsstrom als Leistung für eine Schaltung, die in dem Medium eingebaut ist,
einem Glättungskondensator (211, 311, 411) zum Sammeln des Ausgangstroms der Gleichrichterschaltung (209, 309, 409) und zum Glätten einer Ausgangsspannung derselben, und
einer Spannungsstabilisierungsschaltung (212, 312, 412), die mit dem Glättungskondensator (211, 311, 411) verbunden ist, zum Halten einer Ladespannung des Glättungskondensators (211, 311, 411) auf einem konstanten Wert, gekennzeichnet durch
eine Umschaltachaltung (210, 310a-c, 410a-d), die mit einem Ausgang der Gleichrichterschaltung (209, 309, 409) und dem Glättungskondensator (211, 311, 411) in Reihe geschaltet ist, zum Anschalten und Abschalten eines Stromweges von der Gleichrichterschaltung zu dem Glättungskondensator entsprechend der Übertragungswelle.

2. Medium nach Anspruch 1, das weiter eine Spannungsbegrenzungsschaltung (310d-310i, 410e-410m) zum Begrenzen einer Ausgangsspannung der Gleichrichterschaltung (209) auf einen Wert, der kleiner als ein vorbestimmer Wert ist, wenn der Stromweg von der Gleichrichterschaltung durch die Umschaltachaltung (210, 310a-310c, 410a-410d) ausgeschaltet ist, aufweist.

3. Medium nach Anspruch 2, dadurch gekennzeichnet, daß die Umschaltachaltung

 einen p-Kanal-Transistor (310a), der eine Source, die mit einem Ausgang der Gleichrichterschaltung verbunden ist, ein Drain, das mit dem Glättungskondensator verbunden ist, und ein Gate, das mit der Source über einen Widerstand verbunden ist, aufweist, und
 einen n-Kanal-Transistor (310c), der ein Drain, das mit dem Gate des p-Kanal-Transistors (310a) verbunden ist, eine auf Masse gelegte Source, und ein Gate zum Empfangen der Übertragungswelle aufweist, aufweist.

4. Medium nach einem der Ansprüche 1 bis 3, bei dem die Spannungsstabilisierungsschaltung

 einen n-Kanal-Transistor (312a), der ein Drain, das mit dem Glättungskondensator (311) verbunden ist, eine auf Masse gelegte Source und ein Gate aufweist,
eine Spannungsteilerschaltung (312d, 312e) zum Teilen einer Ladespannung des Glättungskondensators zum Liefern einer geteilten Spannung,
eine Referenzspannungserzeugungsschaltung (312c) zum Erzeugen einer Referenzspannung, und
 einen Komparator (312b), der einen Eingang zum Empfangen der geteilten Spannung von der Spannungsteilerschaltung, einen anderen Eingang zum Empfangen der Referenzspannung von der Referenzspannungserzeugungsschaltung, und einen Ausgang, der mit dem Gate des n-Kanal-Transistors (312a) verbunden ist, aufweist.

5. Medium nach einem der Ansprüche 2 bis 4, dadurch gekennzeichnet, daß die Spannungsbegrenzungsschaltung

 einen n-Kanal-Transistor (310g), der ein Drain, das mit dem Gate des p-Kanal-Transistors (310a) verbunden ist, und eine Source, die auf Masse gelegt ist, und ein Gate aufweist,
eine erste Spannungsteilerschaltung (310h, 310i) zum Teilen der Ladespannung des Glättungskondensators zum Liefern einer ersten geteilten Spannung,
eine zweite Spannungsteilerschaltung (310d, 310e) zum Teilen der Ausgangsspannung der Gleichrichterschaltung zum Liefern einer zweiten geteilten Spannung, und
 einen Komparator (310f), der einen Eingang zum Empfangen der ersten geteilten Spannung, einen anderen Eingang zum Empfangen der zweiten geteilten Spannung, und einen Ausgang, der mit dem Gate des n-Kanal-Transistors (310g) verbunden ist, aufweist.

6. Medium nach Anspruch 2, dadurch gekennzeichnet, daß die Spannungsbegrenzungsschaltung
eine Steuerspannungserzeugungsschaltung (410i) zum Erzeugen einer Steuerspannung (2·VI), die dem vorbestimmbten Wert entspricht, und eine Spannungssteuerschaltung (410h) zum Steuern der Ausgangsspannung der Gleichrichterschaltung unter Verwendung der Steuerspannung, aufweist.

7. Medium nach Anspruch 6, bei dem

die Umschaltschaltung einen p-Kanal-MOS-Transistor (410a), der eine Source, die mit einem Ausgang der Gleichrichterschaltung verbunden ist, ein Drain, das mit dem Glättungskondensator (411) verbunden ist, und ein Gate aufweist, aufweist, und
die Spannungssteuerschaltung (410h) die Ausgangsspannung der Gleichrichterschaltung durch Liefern der Steuerspannung an das Gate des p-Kanal-MOS-Transistors steuert.

8. Medium nach Anspruch 6 oder 7, bei dem die Steuerspannungserzeugungsschaltung (410i) einen Verstärkungskondensator (410i) aufweist, der auf eine Ladespannung des Glättungskondensators während der Zeit, wenn die Gleichrichterschaltung mit dem Glättungskondensator (411) verbunden ist, auffädt, und der, wenn die Gleichrichterschaltung (409) von dem Glättungskondensator (411) getrennt ist, eine Spannung, die im wesentlichen das Doppelte der Ladespannung des Glättungskondensators (411) erzeugt.


Revendications

1. Support d'enregistrement d'information sans contact pour recevoir de l'énergie d'une onde radio appliquée au support de l'extérieur, et émettre des données sous la forme d'une onde d'émission à l'extérieur, comprenant

au moins une antenne (207, 307, 407) pour obtenir l'énergie de l'onde radio qui lui est appliquée de l'extérieur du support ;

un circuit redresseur (209, 309, 409) pour convertir l'énergie obtenue par l'antenne (207, 307, 407) en un courant de sortie en tant qu'alimentation pour un circuit incorporé au support,

un condensateur de filtre (211, 311, 411) pour accumuler le courant de sortie du circuit redresseur (209, 309, 409) et filtrer une tension de sortie de celui-ci, et

un circuit de stabilisation de tension (212, 312, 412) connecté au condensateur de filtre (211, 311, 411), pour maintenir à une valeur constante une tension de charge du condensateur de filtre (211, 311, 411), caractérisé par

circuit de commutation (210, 310a-c, 410a-d), connecté à une sortie du circuit redresseur (209, 309, 409) et au condensateur de filtre (211, 311, 411) en série, pour fermer et ouvrir un trajet de courant depuis le circuit redresseur provenant du circuit redresseur au condensateur de filtre conformément à l'onde d'émission.

2. Support selon la revendication 1, comprenant en outre un circuit de limitation de tension (310d-310, 410e-410m) pour limiter une tension de sortie du circuit redresseur (209) à une valeur inférieure à une valeur prédéterminée lorsque le trajet de courant provenant du circuit redresseur est interrompu par le circuit de commutation (210, 310a-310c, 410a-410d).

3. Support selon la revendication 2, caractérisé en ce que le circuit de commutation comprend

un transistor à canal-p (310a) ayant une source connectée à une sortie du circuit redresseur, un drain connecté au condensateur de filtre, et une grille connectée à la source par l'intermédiaire d'une résistance, et

un transistor à canal-n (310c) ayant un drain connecté à la grille du transistor à canal-p (310a), une source à la masse, et une grille pour recevoir l'onde d'émission.

4. Support selon l'une des revendications 1 à 3, dans lequel le circuit de stabilisation de tension comprend

un transistor à canal-n (312a) ayant un drain connecté au condensateur de filtre (311), une source à la masse, et une grille,
un circuit diviseur de tension (312d, 312e) pour diviser une tension de charge du condensateur de filtrage afin de délivrer une tension divisée, un circuit (312c) de génération de tension de référence pour générer une tension de référence, et un comparateur (312b) ayant une entrée pour recevoir la tension de référence provenant du circuit de génération de tension de référence, et une sortie connectée à la grille du transistor à canal-n (312a).

5. Support selon l'une des revendications 2 à 4, caractérisé en ce que le circuit de limitation de tension comprend

un transistor à canal-n (310g) ayant un drain connecté à la grille du transistor à canal-p (310a), et une source à la masse, et une grille, un premier circuit diviseur de tension (310h, 310i) pour diviser la tension de charge du condensateur de filtrage pour délivrer une première tension divisée,

un second circuit diviseur de tension (310d, 310e) pour diviser la tension de sortie du circuit redresseur pour délivrer une seconde tension divisée, et

un comparateur (310f) ayant une entrée pour recevoir la première tension divisée, une autre entrée pour recevoir la seconde tension divisée, et une sortie connectée à la grille du transistor à canal-n (310g).

6. Support selon la revendication 2, caractérisé en ce que le circuit de limitation de tension comprend

un circuit de génération de tension de commande (410i) pour générer une tension de commande (2.VI) correspondant à la valeur prédéterminée, et un circuit de commande de tension (410h) pour commander la tension de sortie du circuit redresseur en utilisant la tension de commande.

7. Support selon la revendication 6, dans lequel le circuit de commutation comprend un transistor MOS à canal-p (410a) ayant une source connectée à une sortie du circuit redresseur, un drain connecté au condensateur de filtrage (411) et une grille, et le circuit de commande de tension (410h) commande la tension de sortie du circuit redresseur en appliquant la tension de commande à la grille du transistor MOS à canal-p.

8. Support selon la revendication 6 ou 7, dans lequel le circuit de génération de tension de commande (410i) comprend un condensateur élévateur (410i) qui est chargé à une tension du condensateur de filtrage durant le temps pendant lequel le circuit redresseur est connecté au condensateur de filtrage (411) par l'intermédiaire du circuit de commutation (410a-d), et génère, lorsque le circuit redresseur (409) est déconnecté du condensateur de filtrage (411), une tension sensiblement double de la tension de charge du condensateur de filtrage par additionnant à la tension de charge du condensateur de filtrage (411) une tension de charge appliquée au condensateur élévateur (410i) durant le temps pendant lequel le circuit redresseur (409) est connecté au condensateur de filtrage (411).

9. Support selon la revendication 1, comprenant en outre des moyens de commande de courant pour commander, conformément à une tension de commande, un courant de charge circulant depuis le circuit redresseur vers le condensateur de filtrage, un autre condensateur pour accumuler une charge électrique du condensateur de filtrage, et des moyens pour additionner une tension de charge de l'autre condensateur à la tension de charge du condensateur de filtrage lorsque le courant de sortie du circuit redresseur est interrompu, en constituant ainsi les moyens de commande de courant avec le résultat de l'addition en tant que tension de commande.
FIG. 2