**EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent: 10.10.2001 Bulletin 2001/41

(21) Application number: 96109048.7

(22) Date of filing: 05.06.1996

(54) Video signal processing device, information processing system, and video signal processing method

Vorrichtung zur Verarbeitung eines Videosignals, System zum Verarbeiten von Informationen und Verfahren zum Verarbeiten eines Videosignals

Dispositif de traitement d’un signal vidéo, système de traitement d’information, et procédé de traitement de signal vidéo

(84) Designated Contracting States: DE FR GB

(30) Priority: 16.06.1995 JP 17420195


(73) Proprietor: SEIKO EPSON CORPORATION Shinjuku-ku Tokyo (JP)

(72) Inventor: Hirashima, Satoshi Suwa-shi, Nagano-ken (JP)

(74) Representative: Hoffmann, Eckart, Dipl.-Ing. Patentanwalt, Bahnhofstrasse 103 82166 Gräfelfing (DE)

(56) References cited:

Description

Background of the Invention

Field of the Invention

[0001] The present invention relates to a video-signal processing device, an information processing system comprising this video signal processing device, and a method of processing a video signal.

Background of the Invention

[0002] A conventional information processing system uses an image supply apparatus such as a personal computer, multimedia terminal, and game machine to supply a video signal and output the signal to a display device such as a monitor or a liquid crystal panel. In such a system, the configuration is such that the image supply apparatus and the display device are linked together by an analog interface, and an analog video signal from the image supply apparatus is supplied to the display device. Therefore, if it is desired to subject the supplied video signal to digital signal processing, the video signal should first be converted by an A/D converter into a digital signal. Then, the converted signal be output to the display device through a D/A converter after the signal has been subjected to the digital signal processing.

[0003] Currently, the development and implementation of a projection type of display system is in progress as one type of multimedia presentation system. To ensure that an information processing system such as this projection type of display system can be used in as many situations as possible, it is preferable to develop a system which can be connected to and compatible with all types of personal computer. However, it is unfortunately true that the clock frequencies of video signals differ between different personal computers. Thus, it is difficult to adjust the phase of a sampling clock signal used by the A/D converter, if the clock frequencies of different types of personal computer are greatly different. If it is not possible to adjust the phase of the sampling clock signal as appropriate, problems such as a dramatic deterioration in the display characteristics will occur.

[0004] One method that has been considered for implementing such a phase adjustment is to have the user manually operate a control called SYNC adjustment. Nevertheless, this operation places a large burden on the user in that it is complicated and difficult to understand. That is why it is desired to provide a system that enables simple and automatic adjustment of the phase of the sampling clock signal.

[0005] A video signal processing device in accordance with the preamble of claim 1 and a method in accordance with the preamble of claim 7 are known from EP-A- 202 015. This document discloses method of and device for generating an electrical signal representative of subcarrier to horizontal sync phase of a composite video signal that includes a horizontal sync pulse and a colour burst, wherein the video signal is sampled under control of a clock signal having a frequency equal to an integral multiple of the burst frequency. The two samples taken immediately before and after the sync point of the horizontal sync pulse are determined and the samples are interpolated to determine the value of a first angle representative of the phase within the clock cycle at which the sync point occurred. The value of the second angle is determined which is representative of the phase within the subcarrier cycle at which a third sample is taken and the required electrical signal is generated using the values of the first and second angles and the relationship between the clock frequency and burst frequency.

Summary of the Invention

[0006] The present invention has been devised in order to solve the above concern with the prior art. Its objective is to provide a video signal processing device, an information processing system, and a method of processing a video signal that enables simple adjustment of the phase of a sampling clock signal.

[0007] This object is achieved with a video signal processing device as claimed in claim 1, an information processing system as claimed in claims 5 and 6, and a method as claimed in claim 7, respectively. Preferred embodiments of the invention are subject-matter of the dependent claims.

[0008] In accordance with the invention edge pulses are generated by subjecting a video signal and a delayed video signal to subtraction processing, and the edge pulses or information obtained from the edge pulses is used as edge information in the adjustment of the phase of the sampling clock signal. The width of the edge pulses is obtained from the video signal and the delayed video signal, and can be determined by the delayed time of the delayed video signal. Thus the width of the edge pulses can be kept constant, regardless of the state of the video signal, making it possible to guarantee stable operation of the circuitry to which these edge pulses are input. This aspect of the invention makes it possible to obtain appropriate edge information, even when ringing occurs or the video signal is nois, so that a suitable sampling clock signal can be obtained and thus a high-quality display image can be obtained.

[0009] One embodiment of the present invention has a circuit for comparing the amplitude voltage of the edge pulse with a given threshold voltage, and an adjustment circuit for adjusting the value of the threshold voltage.

[0010] This makes it possible for an adjustment circuit to adjust the value of a threshold voltage that is compared by a comparison circuit with the amplitude voltage of the edge pulse. Thus, the threshold voltage can be increased if the amplitude voltage of the edge pulse is
large, or decreased if the amplitude voltage is small. This makes it possible to prevent problems such as misoperation of the comparison circuit due to noise.

[0011] In this case, the adjustment circuit preferably adjusts the threshold voltage in accordance with the magnitude of the amplitude voltage of the video signal. This is because the amplitude voltage of edges pulses is often large when the amplitude voltage of the video signal is large.

[0012] Another embodiment of the present invention has phase adjustment means for adjusting the phase of the sampling clock signal based on a digital signal that is output from the A/D converter.

[0013] This makes it possible for the phase adjustment means to check the digital signal that is obtained by the A/D converter by using the given sampling clock signal, and adjust the phase of the sampling clock signal on the basis of the result of this check. The digital signal obtained by the sampling clock signal that has been subjected to this phase adjustment can be checked again and the phase of the sampling clock signal can be adjusted on the basis of the result of this check, so that a sampling clock signal of an appropriate phase can be obtained by repeating this process. This aspect of the invention makes it possible to implement complicated and highly accurate phase adjustment, using any processor that operates with any given software.

[0014] In this embodiment of the invention, the phase adjustment means may perform the phase adjustment by comparing a digital signal that is output from the A/D converter when the sampling clock signal has a first phase and a digital signal that is output from the A/D converter when the sampling clock signal has a second phase. Adjusting the phase by comparing the results with first and second phases in this manner enables a simple method of determining the maximum and minimum values of a characteristic of the video signal, such as its brightness.

[0015] Still another embodiment of the invention, comprises a circuit for extracting a reference clock signal from the video signal; a circuit for generating clock signals with different phases, based on the extracted reference clock signal; a selector for selecting one of the clock signals and supplying the selected clock signal as the sampling clock signal to the A/D converter; and means for indicating to the selector which of the clock signals is to be selected. This makes it possible to implement adjustment of the phase of the sampling clock signal by simply selecting one of a plurality of clock signals, which simplifies the circuit configuration and speeds up the processing.

Detailed Description of the Preferred Embodiments

First Embodiment

[0017] A first embodiment of the present invention is shown in Fig. 1. This embodiment generates an edge pulse by performing a subtraction based on a video signal and a signal that is delayed by the video signal, then adjusts the phase of a sampling clock signal of an A/D converter on the basis of the edge pulse. Note that the description of the following embodiments mainly deals with examples in which the present invention is applied to a projection type of display system, though the present invention is not necessarily limited thereto.
ratus such as a personal computer, via a PC video input terminal 4. The A/D converter 10 converts the video signal 22 into a digital signal 24, and outputs the thus obtained digital signal 24 to a digital signal processor 12. The digital signal processor 12 subjects the digital signal 24 to various types of digital signal processing for on-screen display (the display of additional material such as writing on the screen) and digital y correction. A signal that has been subjected to the digital signal processing is converted into an analog signal by a D/A converter 14, and is output to a projector mechanism (display device) 16. The projector mechanism 16 projects a picture from the personal computer onto a screen, and comprises a signal driver, a scan driver, a liquid crystal panel, and an optical system.

In this embodiment, A/D conversion is necessary to enable the analog video signal 22 that is input from the personal computer to be subjected to various types of digital signal processing. However, it should be noted that this A/D conversion would still be necessary, even if the signal is not subjected to processing to enable on-screen display. In other words, it is preferable that the recently developed projection type of display system is capable of displaying TV images, making it necessary to provide a digital chroma circuit 18 for converting a TV video signal into an RGB signal. This TV video signal may be of any of various formats, such as NTSC and PAL/SECAM, and is received via a TV video input terminal 6. The output of the digital chroma circuit 18 is usually a digital signal. Therefore, to make it possible for a projection type of display system to display both images from a personal computer and a TV set, it is necessary to convert the TV image into a digital signal in the same manner as the video signal 22 from the personal computer. That is why the A/D conversion performed by the A/D converter 10 is necessary, even if no digital signal processing is required for purposes such as on-screen display.

Note that the signal after D/A conversion is input to the projector mechanism 16 in Fig. 1, but the output of the digital signal processor 12 may be input directly to the projector mechanism 16 if the projector mechanism 16 has a digital interface. The digital signal processor 12 selects either the output of the A/D converter 10 or the output of the digital chroma circuit 18. A sampling clock signal supply circuit 30 supplies a sampling clock signal 26 to the A/D converter 10, when it is necessary to sample the video signal 22. The sampling clock signal supply circuit 30 comprises a reference clock signal extraction circuit 32, a multi-stage clock signal delay circuit 34, a selector 36, and an edge detection circuit 40. A processor 20 provides control over the entire apparatus, and comprises components such as a CPU and memory. The processor 20 also indicates to the sampling clock signal supply circuit 30 (the selector 36 therein) that the phase of the sampling clock signal is to be adjusted, on the basis of edge information 28 that is input thereto from the edge detection circuit 40.

The configuration and operation of the present embodiment will now be described in detail. An example of the video signal 22 that is input from a personal computer is shown in Fig. 2A. The pulses shown at J and K in this figure are used for enabling horizontal synchronization and are equivalent to a horizontal synchronization signal. A part L of the waveform in Fig. 2A is shown enlarged in Fig. 2B. If the period of the video signal is assumed to be T, a frequency $F = 1/T$ will differ according to the type of personal computer that is supplying the video signal. This frequency is approximately $25\, \text{MHz}$ in a personal computer manufactured by IBM Corporation, for example, but it is $21\, \text{MHz}$ in a personal computer manufactured by NEC Corporation. There are also subtle differences in frequency between different models produced by IBM Corporation, as well as differences in the quality of the video signal, i.e., differ frequency characteristic. This has various effects on the video signal. For instance, the waveform of the video signal should ideally be as shown in Fig. 2B. Nevertheless, in practice it depends on the capabilities of the video board and other components used by the personal computer and often ringing noise is superimposed on the signal, as shown in Fig. 2C.

The above described A/D converter 10 is able to input various types of video signals, with different characteristics such as frequency that depend on the type of personal computer. However, to make the system more universal, it is preferable that the A/D converter 10 is compatible with all types of personal computer. Thus, it is necessary to design the A/D converter 10 for the conversion of all types of video signal as appropriate.

An example of the configuration of the reference clock signal extraction circuit 32 is shown in Fig. 3. The reference clock signal extraction circuit 32 extracts a clock signal to act as a reference from the video signal. A typical configuration of this circuit may comprise a phase comparator 60, a low-pass filter (LPF) 62, a voltage-controlled oscillator (VCO) 64, and a 1/N frequency divider 66. Inputs to the phase comparator 60 are an horizontal synchronization signal $Hs$ that is equivalent to pulses J and K in Fig. 2A and a signal 1 that is an output CLK0 from the VCO 64, divided by N by the 1/N frequency divider 66. With the VGA standard, there are 640 dots across the screen in the scan direction, which means that the value of N set in the 1/N frequency divider 66 would be approximately 800. Thus, if the frequency of the horizontal synchronization signal $Hs$ is assumed to be $Fs$, a reference clock signal CLK0 having a frequency of $800 \times Fs$ is output from the VCO 64. This reference clock signal CLK0 also acts as a dot clock signal for display devices such as liquid crystal displays.

An example of the configuration of the multi-stage clock signal delay circuit 34 is shown in Fig. 4. This multi-stage clock signal delay circuit 34 comprises serially connected buffers 70-1 to 70-n. The reference clock signal CLK0 extracted by the reference clock sig-
nal extraction circuit 32 is input to the first buffer 70-1, and outputs CLK1 to CLKn from these buffers are input to the selector 36.

[0026] The relationship between these outputs CLK1 to CLKn and the video signal 22 is shown in Fig. 5. As can be seen from this figure, the phase of CLK1 is shifted by 3 to 4 ns which is equivalent to the delay set by that buffer from that of CLKO. The relationship between CLK1 and CLK2, and between CLK3 and CLK4, etc, is the same. The selector 36 selects one clock signals from this group of clock signals CLKO to CLKn having different phases, in accordance with an indication from the processor 20, and outputs that signal as the sampling clock signal 26 to the A/D converter 10. An edge of this sampling clock signal such as the rising edge should be matched with the maximum and minimum points of the brightness of the video signal 22. If the edge and these points are not matched, the picture quality will be greatly deteriorated in such a manner that the display device will shown grey, for example, even when the video signal specifies black. Therefore, the selector 36 selects a clock signal such as CLK2, and this CLK2 is used as the sampling clock signal 26 for output to the A/D converter 10. As shown in Fig. 5, the rising edges of CLK2 match a maximum point G and minimum point H of the brightness of the video signal 22. Therefore, a good-quality picture can be obtained by using this CLK2 to sample the video signal 22.

[0027] An example of the configuration of the A/D converter 10 is shown in Fig. 6. The A/D converter 10 compares the input analog video signal 22 with various quantized levels, to convert the signal 22 into an 8-bit digital signal D0 to D7. A voltage range between an upper reference voltage VH and a lower reference voltage VL is divided by resistors 74-1 to 74-254, and the thus divided voltages are input to sampling comparators 72-1 to 72-255. These sampling comparators 72-1 to 72-255 sample the video signal 22 on the basis of the sampling clock signal 26 that is input there to the selector 36, and also compare the thus sampled video signal with the above described divided voltages. The results are output to an encoder 76 which determines a digital value corresponding to the level of the video signal 22, on the basis of these comparison results, and latches that value in a latch 78. The latched digital signal is output to the digital signal processor 12.

[0028] It should be noted that, although a parallel-comparator type of A/D converter is shown in Fig. 6, the configuration of the A/D converter is not limited thereto. This configuration may be of any form, such as a 2-step (N-step) parallel-comparator type of A/D converter, provided that an analog video signal is at least sampled with a sampling clock signal to implement an A/D conversion.

[0029] In this first embodiment, the processor 20 gives the selector an indication as to which sampling clock signal to select. In this case, this indication from the processor 20 is based on edge information that is input from the edge detection circuit 40, i.e., information indicating the position of the edge in the video signal.

[0030] The edge detection circuit 40 comprises a delay circuit 42, an inverting buffer 44, and a comparator 46, as shown in Fig. 1. An example of the configuration of the delay circuit 42 is shown in Fig. 7. The video signal 22 is buffered by a circuit consisting of a transistor 80 and a resistor R1, then is delayed by a circuit consisting of capacitors C1 and C2 and an inductance L1. In the example shown in Fig. 7, the video signal is delayed by approximately 10 ns. Note that R2 and R3 in this figure denote resistors for impedance matching.

[0031] The video signal 22 having a waveform such as that shown in Fig. 8A is input to the delay circuit 42 and the inverting buffer 44. The video signal that has been delayed by the delay circuit 42 is added to the video signal that has been inverted by the inverting buffer 44 to generate edge pulses such as those shown in Fig. 8B. The width of these edge pulses is set to be approximately 10 ns which is equivalent to the delay of the delay circuit 42. The edge pulses are input to one of the terminals of the comparator 46, such as the positive terminal, and is compared with a threshold voltage VT input to the other terminal such as the negative terminal. This causes a signal such as that shown in Fig. 8C to be output from the comparator 46, and the signal is input to the processor 20 as edge information.

[0032] It should be noted that, although the rising edges of the video signal 22 are used as edge information in Fig. 8C, the falling edges are equally valid, as is a combination of both rising and falling edges. In such a case, a comparator is used that compares a threshold voltage VT and edge pulses crossing the VT, as shown in Fig. 8B. The output of the comparator and that of the above described comparator which uses VT may be input to means such as an OR circuit.

[0033] The above described first embodiment is characterized in the generation of edge pulses by subtracting a delayed video signal from the video signal itself. This method of using a delay circuit has advantages, as described below.

[0034] Firstly, the width of the edge pulses shown in Fig. 8A is determined by the delay of the delay circuit 42, and thus the width can be set to be constant such as approximately 10 ns. Since this prevents problems such as variations in the width of the edge pulses according to the waveform of the video signal, this ensures stable operation of subsequent circuits such as the comparator 46.

[0035] Secondly, if ringing should occur in the video signal, such as is shown for example in Fig. 9A, it is possible to reduce the amplitude voltage of pulses generated at positions where ringing is generated, as shown in Fig. 9B. Therefore, appropriate edge information such as that shown in Fig. 9C can be output to the processor 20, even if problems such as ringing occur.

[0036] Thirdly, in conditions where the frequency characteristic of the video signal is poor or the signal is noisy, the present embodiment may generate edge
pulses of a constant amplitude voltage and constant width, and thus obtain stable and appropriate edge information, regardless of the quality of the video signal.

Thus, the above described first embodiment enables the processor 20 to receive appropriate and stable edge information, regardless of the quality of the video signal, so that the processor 20 can select a sampling clock signal on the basis of this favorable edge information, in other words, adjust the phase of the sampling clock signal. The thus obtained appropriate and stable sampling clock signal 26 can be supplied to the A/D converter 10, enabling a huge improvement in display quality.

It should be noted that, although the phase adjustment of the sampling clock signal in accordance with the first embodiment uses components such as the reference clock signal extraction circuit 32, the multi-stage clock signal delay circuit 34, and the selector 36, the present invention is not limited thereto and various other equivalent circuit configurations can be used instead. For example, the reference clock signal CLK0 may be supplied from external equipment, not extracted from the video signal 22. Note also that the circuit for obtaining edge pulses from the video signal 22 and a delayed video signal is not limited to the configuration shown in Fig. 1. Similarly, the configuration may be one in which components such as the comparator 46 are omitted and edge pulses are used as the edge information without modification.

Second Embodiment

A second embodiment of the present invention is provided with a circuit that adjusts the threshold voltage VT used for comparing edge pulses. An example of the configuration of the present embodiment is shown in Fig. 10.

An adjustment circuit 82 comprises an integrating circuit 84, an LPF 86, and a reference threshold voltage generation circuit 88. The threshold voltage VT, which is an output from the circuit 82, is input to the negative terminal of the comparator 46. The comparator 46 compares the threshold voltage VT and the edge pulses as shown in Fig. 8B, and outputs the edge information shown in Fig. 8C. It is clear from Fig. 8B that, if VT is too small, the comparator 46 will react to pulses caused by factors such as low-level noise in the amplitude voltage. On the other hand, if VT is too large, the problem will occur that the comparator 46 will not react to the edge pulses. These problems can be solved by the provision of the adjustment circuit 82 for adjusting the threshold voltage VT.

With the circuitry shown in Fig. 10, the value of the threshold voltage VT is adjusted according to the amplitude voltage of the video signal 22. Assume for example that a waveform signal shown in Fig. 11A is input as the video signal 22. This video signal 22 is integrated by the integrating circuit 84, so that a waveform signal similar to that shown in Fig. 11B is output from the integrating circuit 84. When this signal is input to the LPF 86, a DC voltage of, for example, 0.3 V is output from the LPF 86, as shown in Fig. 11C. This 0.3-V DC voltage is added to a 0.3-V DC voltage that is output from the reference threshold voltage generation circuit 88, so that, as a result, a threshold voltage VT of 0.6 V is output from the adjustment circuit 82. If, however, a waveform video signal such as that shown in Fig. 11D whose overall amplitude voltage is lower than the waveform video signal of Fig. 11A is input, a waveform signal such as that shown in Fig. 11E is output from the integrating circuit 84, and a DC voltage of 0.1 V is output from the LPF, as shown in Fig. 11F. Thus a threshold voltage VT of 0.4 V is output.

As described above, the present embodiment ensures that the threshold voltage VT increases if the amplitude voltage of the video signal 22 is large overall. The threshold voltage VT decreases if the amplitude voltage is small. In general, the amplitude voltage of edge pulses is often dependent on the magnitude of the amplitude voltage of the video signal. Thus it is possible to implement an edge detection circuit which is not susceptible to noise and which can accurately detect edges in the video signal, by adjusting the threshold voltage VT in accordance with the magnitude of the amplitude voltage of the video signal.

It should be noted that the method of adjusting the threshold voltage VT in accordance with the present invention is not limited to the second embodiment as described above. Any method can be used therefor, provided that it at least allows for the mutual relationship between the magnitude of the amplitude voltage of the edge pulses and the magnitude of the threshold voltage VT. The configuration of the edge detection circuit and other circuitry can also be implemented in many different ways.

Third Embodiment

A third embodiment of the present invention adjusts the phase of the sampling clock signal on the basis of a digital signal that is output from the A/D converter. An example of the configuration of this embodiment is shown in Fig. 12.

In this figure, components such as line memories 90 and 92 and the processor 20 act as phase adjustment means. Each of these line memories 90 and 92 holds a given amount of data, such as data for one scan line, that is output from the A/D converter 10. The configuration may, of course, be such that data for a plurality of scan lines is held therein. In the same manner as in the first embodiment, the sampling clock signal supply circuit 30 may comprise a reference clock signal extraction circuit 32, a multi-stage clock signal delay circuit 34, a selector 36, and an edge detection circuit 40.

An example of the operation of this third embodiment will now be described. At initialization, the
The configuration of the sampling clock signal 1 supply circuit 30 is not limited to that shown in Fig. 12.

**Fourth Embodiment**

[0051] A fourth embodiment of the present invention facilitates the phase adjustment by supplying a phase-adjustment video signal to the video signal processing device. An example of the configuration of the present embodiment is shown in Fig. 13.
of the phase-adjustment video signal is preferably slightly wider than a window defined by voltage levels VH and VL, as shown in Fig. 14B. In other words, the maximum brightness of the phase-adjustment video signal, for example, the white level, is preferably slightly greater by, for example, one quantized level than VH whereas the minimum brightness thereof is slightly smaller by, for example, one quantized level than VL. These levels VH and VL act as upper and lower reference voltages for the A/D converter 10, as shown in Fig. 6, and define an A/D conversion window for the A/D converter 10. The A/D converter 10 divides the voltage difference defined by this window into a number of levels, such as 256 levels (for 8-bit display).

The voltage difference between the black and white levels is regulated by the analog video signal interface to be 0.714 V, for example. Therefore it is common to fix the width of this window to 0.71 V. However, personal computers that can supply video signal are made by different manufacturers and name different capabilities, causing various problems such as a voltage difference between the black and white levels being greater than 0.714 V, or less than 0.714 V, which adversely affects the resolution of the A/D conversion. In order to prevent such problems, the video signal generation means 102 in the personal computer 100 outputs a video signal with an amplitude voltage that is slightly wider than the window width, as a phase-adjustment video signal. The processor 20 may also indicate to the personal computer 100 that a video signal with this larger amplitude voltage is to be output.

The voltage may also be such that the values of VH and VL set by the A/D converter 10 can be changed by the use of components such as resistors, to match the type of personal computer being used.

Since this fourth embodiment makes it possible to adjust the phase of the sampling clock signal without wasting any time using a phase-adjustment video signal that has been optimized for phase adjustment, it enables huge improvements in display quality and ease of use.

It should be noted that the present invention is not to be taken as being limited to the above described first to fourth embodiments; the present invention can be modified in various ways within the scope of the claims stated herein.

For example, although the present invention is particularly suitable for a projection type of display system, it can also be applied to other types of information processing system such as a multimedia system.

The configurations of circuits such as the sampling clock signal supply circuit and edge detection circuit should also not be taken as limited to those described in the above described first to fourth embodiment; other equivalent circuits can be used instead.

Claims

1. A video signal processing device, comprising:

   an A/D converter (10) for sampling an analog video signal (22) by a given sampling clock signal (26), and for converting said sampled signal into a digital signal; and
   a sampling clock signal supply circuit (30) for supplying said sampling clock signal (26) to said A/D converter (10);

   characterized in that said sampling clock signal supply circuit (30) comprises

   - sampling clock signal generating means (32),
   - phase adjustment means (20, 34, 36) for adjusting the phase of said sampling clock signal (26) generated by said sampling clock signal generating means (32), and
   - an edge detection circuit for obtaining edge information for use in adjusting the phase of said sampling clock signal (26),

   wherein said edge detection circuit (40) comprises a circuit for generating an edge pulse (28) by subtracting said video signal and a delayed version of said video signal from one another, said edge pulse representing said edge information.

2. The device as defined in claim 1, wherein said edge detection circuit (40) comprises a circuit for comparing the amplitude voltage of said edge pulse with a given threshold voltage and an adjustment circuit (82) for adjusting the value of said threshold voltage.

3. The device as defined in claim 1, wherein said phase adjustment means (20, 34, 36, 90, 92) comprises means (90, 92) for adjusting the phase of said sampling clock signal based on the digital signal that is output from said A/D converter (10).

4. The device as defined in any one of claims 1 to 3, further comprising:

   - a circuit (32) for extracting a reference clock signal from said video signal;
   - a circuit (34) for generating clock signals with different phases based on said extracted reference clock signal;
   - a selector (36) for selecting one of said clock signals and supplying the selected clock signal as said sampling clock signal to said A/D converter (10); and
   - means (20) for indicating to said selector (36) which of said clock signals is to be selected.
5. An information processing system comprising an image supply apparatus (100) for supplying a video signal and the video signal processing device (110) as defined in any one of claims 1 to 4, wherein said video signal processing device (110) comprises means for subjecting a digital signal that is output from said A/D converter (10) to given digital signal processing.

6. An information processing system comprising an image supply apparatus (100) for supplying a video signal and the video signal processing device (110) as defined in any one of claims 1 to 4, wherein said video signal processing device (110) comprises means for converting a given television video signal into a digital signal and means for selecting one of said digital signal and a digital signal that is output from said A/D converter (10) as an image signal.

7. A method of processing a video signal, comprising:
   (a) sampling an analog video signal (22) by means of a sampling clock signal (26); and
   (b) converting the samples obtained in step (a) into a digital signal;

   characterized in that step (a) further comprises
   (a1) generating an edge pulse (28) by subtracting said video signal and a delayed version of said video signal from one another, said edge pulse representing edge information, and
   (a2) adjusting the phase of said sampling clock signal in accordance with said edge information.

Patentansprüche

1. Videosignalverarbeitungsvorrichtung mit
   einem A/D-Umsetzer (10) zum Abtasten eines analogen Videosignals (22) mit einem gegebenen Abtasttaktsignal (26) und zum Umwandeln des abgetasteten Signals in ein digitales Signal; und
   einer Abtasttaktsignalschaltung (30), welche dem A/D-Umsetzer (10) das Abtasttaktsignal (26) liefert,

dadurch gekennzeichnet, daß die Abtasttaktsignalschaltung (30) folgendes aufweist:
   - eine Abtasttaktigenieurzeugereinrichtung (32),
   - eine Phaseneinstelleinrichtung (20, 34, 36) zum Einstellen der Phase des von der Abtasttaktigenieurzeugereinrichtung (32) erzeugten Abtasttaktsignals (26) und
   - eine Flankenfassungsschaltung zum Erhalten von Flankeninformation zur Benutzung beim Einstellen der Phase des Abtasttaktsignals (26),

wobei die Flankenfassungsschaltung (40) eine Schaltung aufweist, um durch Subtrahieren eines Videosignals und einer verzögerten Form des Videosignals voneinander einen Flankenimpuls (28) zu erzeugen, wobei der Flankenimpuls die Flankeninformation darstellt;

2. Vorrichtung nach Anspruch 1, bei der die Flankenfassungsschaltung (40) eine Schaltung zum Vergleichen der Amplitudenspannung des Flankenimpulses mit einer gegebenen Schwellschaltung und eine Einstellschaltung (82) zum Einstellen des Wertes der Schwellschaltung aufweist.

3. Vorrichtung nach Anspruch 1, bei der die Phaseneinstelleinrichtung (20, 34, 36, 90, 92) Mittel (90, 92) zum Einstellen der Phase des Abtasttaktsignals anhand des vom A/D-Umsetzer (10) abgegebenen digitalen Signals aufweist.

4. Vorrichtung nach einem der Ansprüche 1 bis 3, ferner mit:
   - einer Schaltung (32) zum Extrahieren eines Bezugstaktsignals aus dem Videosignal;
   - einer Schaltung (34) zum Erzeugen von Takt- signalen mit unterschiedlichen Phasen anhand des extrahierten Bezugstaktsignals;
   - einem Selektor (36) zur Auswahl eines der Taktsignale und zum Liefern des ausgewählten Taktsignals an den A/D-Umsetzer (10) als Abtastsignal; und
   - einer Einrichtung (20), die dem Selektor (36) anzeigt, welches der Taktsignale auszuwählen ist.

5. Informationsverarbeitungssystem mit einem Bildliefergerät (100) zum Liefern eines Videosignals und der Videosignalverarbeitungsvorrichtung (110) gemäß einem der Ansprüche 1 bis 4, bei dem die Videosignalverarbeitungsvorrichtung (110) eine Einrichtung aufweist, die ein vom A/D-Umsetzer (10) abgegebenes digitales Signal einer gegebenen digitalen Signalverarbeitung unterzieht.

6. Informationsverarbeitungssystem mit einem Bildliefergerät (100) zum Liefern eines Videosignals und der Videosignalverarbeitungsvorrichtung (110) gemäß einem der Ansprüche 1 bis 4, bei dem die Videosignalverarbeitungsvorrichtung (110) Einrichtungen zum Umwandeln eines gegebenen Fernsehvideosignals in ein digitales Signal und Einrich-
tungen aufweist, um als Bildsignal entweder das digitale Signal oder ein digitales Signal auszuwählen, das vom A/D-Umsetzer (10) ausgegeben wird.

7. Verfahren zum Verarbeiten eines Videosignals mit:
   (a) Abtasten eines analogen Videosignals (22) mittels eines Abtastaktsignals (26) und
   (b) Umwandeln der im Schritt (a) erhaltenen Abtastwerte in ein digitales Signal,

dadurch gekennzeichnet, daß der Schritt (a) ferner folgendes umfaßt:
   (a1) Erzeugen eines Flankenimpulses (28) durch Subtrahieren des Videosignals und einer verzögerten Form des Videosignals voneinander, wobei der Flankenimpuls Flankeninformation darstellt und
   (a2) Einstellen der Phase des Abtastaktsignals in Übereinstimmung mit der Flankeninformation.

Revidications

1. Dispositif de traitement de signal vidéo, comprenant:
   un convertisseur A/N (10) destiné à échantillonner un signal vidéo analogique (22) au moyen d’un signal d’horloge d’échantillonnage donné (26), et à convertir le signal échantillonné en un signal numérique ; et
   un circuit (30) de fourniture de signal d’horloge d’échantillonnage destiné à fournir le signal (26) d’horloge d’échantillonnage au convertisseur A/N (10) ;
   caractérisé en ce que le circuit de fourniture de signal d’horloge d’échantillonnage (30) comprend:
   - des moyens de production de signal d’horloge d’échantillonnage (32) ;
   - des moyens d’ajustement de phase (20, 34, 36, 90, 92) destinés à ajuster la phase du signal d’horloge d’échantillonnage (26) produit par les moyens de production de signal d’horloge d’échantillonnage (32) ; et
   - un circuit de détection de fronts destiné à obtenir des informations de fronts pour une utilisation dans l’ajustement de la phase du signal d’horloge d’échantillonnage (26) ; dans lequel le circuit de détection de fronts (40) comprend un circuit destiné à produire une impulsion de front (28) en soustrayant l’un à l’autre le signal vidéo et une version retardée de ce signal vidéo, l’impulsion de front représentant ces informations de fronts.

2. Dispositif suivant la revendication 1, dans lequel le circuit (40) de détection de fronts (40) comprend un circuit destiné à comparer la tension d’amplitude de l’impulsion de front à une tension de seuil donnée et un circuit d’ajustement (82) pour ajuster la valeur de cette tension de seuil.

3. Dispositif suivant la revendication 1, dans lequel les moyens d’ajustement de la phase (20, 34, 36, 90, 92) comprennent des moyens (90, 92) destinés à ajuster la phase du signal d’horloge d’échantillonnage sur la base du signal numérique qui est fourni en sortie par le convertisseur A/N (10).

4. Dispositif suivant l’une quelconque des revendications 1 à 3, comprenant en outre :
   un circuit (32) destiné à extraire un signal d’horloge de référence du signal vidéo ; un circuit (34) destiné à produire des signaux d’horloge ayant des phases différentes sur la base du signal d’horloge de référence extrait ; un sélecteur (36) destiné à sélectionner l’un, de ces signaux d’horloge et à fournir le signal d’horloge sélectionné en tant que signal d’horloge d’échantillonnage au convertisseur A/N (10) ; et des moyens (20) destinés à indiquer au sélecteur (36) lequel des signaux d’horloge doit être sélectionné.

5. Système de traitement d’informations comprenant un appareil (100) de fourniture d’image destiné à fournir un signal vidéo et le dispositif (110) de traitement de signal vidéo suivant l’une quelconque des revendications 1 à 4, dans lequel le dispositif (110) de traitement de signal vidéo comprend des moyens destinés à soumettre un signal numérique qui est fourni en sortie par le convertisseur A/N (10) à un traitement de signal numérique donné.

6. Système de traitement d’informations comprenant un appareil (100) de fourniture d’image destiné à fournir un signal vidéo et le dispositif (110) de traitement de signal vidéo suivant l’une quelconque des revendications 1 à 4, dans lequel le dispositif (110) de traitement de signal vidéo comprend des moyens destinés à convertir un signal vidéo de télévision donné en un signal numérique et des moyens destinés à sélectionner l’un du signal numérique et d’un signal numérique qui est fourni en sortie par le convertisseur A/N (10) en tant qu’un signal d’image.
7. Procédé de traitement d'un signal vidéo, comprenant :

(a) l'échantillonnage d'un signal vidéo analogique (22) au moyen d'un signal d'horloge d'échantillonnage (26) ; et
(b) la conversion des échantillons obtenus à l'étape (a) en un signal numérique ;

caractérisé en ce que l'étape (a) comprend en outre :

(a1) la production d'une impulsion de front (28) en soustrayant l'un à l'autre le signal vidéo et une version retardée de ce signal vidéo, l'impulsion de front représentant des informations de fronts, et
(a2) l'ajustement de la phase du signal d'horloge d'échantillonnage en fonction de ces informations de fronts.
FIG. 4

26 SAMPLING CLOCK SIGNAL

FROM PROCESSOR

SELECTOR

CLK0

CLK1

CLK2

CLK3

CLK4

CLKn

CLKn-1

70-(n-1)

70-n

70-3

70-2

70-1

36

34