Information storage controller

Informationsspeicherungssteuerungsgerät

Contrôleur de stockage d'information

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US-A- 4 303 988

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an information storage controller for high speed information transmission in a magnetic storage device or the like.

Description of the Prior Art

[0002] Recent development of digital compression technology of visual and audio signals makes it possible to process visual and audio signals by a computer and store the signals in a magnetic storage device to be accessed by a computer.

[0003] As to visual and audio signals, it is a problem that an image or a sound is stopped when processing of a prescribed amount of information is not completed in a prescribed time. In order to prevent this problem, a high speed magnetic storage device is demanded for high speed information processing.

[0004] Further, it is also demanded to increase a memory capacity and to store a large capacity of information. A technique called redundant array of inexpensive disk (herein referred to as RAID) is used practically in order to meet this demand.

[0005] A RAID is an information storage controller which controls a plurality of magnetic disks so that redundant information as well as information to be stored are stored in the magnetic disks in a distributed way. When one of the magnetic disks is failed, it can recover the information in the failed magnetic disk according to the redundant information. Then, a normal operation can be performed again.

[0006] RAID-5 (or RAID level 5), as one of the techniques of RAID, stores redundant information in a plurality of magnetic disks cyclicly. Let us assume that the information storage controller (RAID-5) has five magnetic disks HD1 - HD5. Information to be written is divided to four information blocks D1 - D4. First, the information blocks D1 - D4 are written to four magnetic disks HD1 - HD4, respectively, and redundant information block P1 is generated for the information blocks D1 - D4 to be written to the fifth magnetic disk HD5. Subsequently, when information blocks D5 - D8 is written, the information is written to HD2 - HD5, while redundant information block P2 for the information blocks D5 - D8 is written to the first magnetic disk HD1. In this way, redundant information blocks P1, P2, … are stored cyclicly to a different magnetic disk from the magnetic disk which stores the previous redundant information.

[0007] However, in the information storage controller, when information is written to a plurality of magnetic disks, redundant information has to be generated. Then, write operation may become slower than in a case using a single magnetic disk. Further, when one of the magnetic disks has a fault, processing speed becomes very slow in order to restore the information in the fault magnetic disk. Further, when the faulty magnetic disk is replaced with a new normal one, the information in the fault magnetic disk has to be restored in the normal one automatically. However, the operation speed becomes rather slow during this operation. This is ascribed to a task to generate redundant information and to write it to a prescribed memory after the central processing unit reads data a plurality of times (sequential read). This work is performed for all the data, so that a long processing time is needed.

[0008] Further, in the prior art information storage controller, a work on each magnetic disk and an input/output operation with the external are performed in time sharing. That is, only one work is performed at a time.

[0009] The US-patent 5,128,810 is concerned with a multiple disk drive array storage device. This storage device emulates the operation of a single disk drive in such a way that the handshaking and protocol between the array storage device in the host computer appears to the host computer to be that of a single disk drive. Digital data words received by the array storage device controller divides the words into subparts and writes each subpart to a different disk drive within the storage device.

SUMMARY OF THE INVENTION

[0010] An object of the invention is to provide an information storage controller having a higher speed of information transmission with magnetic storage devices.

[0011] This object is solved according to the present invention, which is defined in detail in the appended independent claim 1, by an information storage controller for controlling write and read of information to and from magnetic disks, the controller comprising: an external communications means for communicating information with an external equipment; a plurality of magnetic disk communication means for communicating information with a plurality of magnetic disks; first and second groups each consisting of a plurality of memory devices, wherein a number of memory devices in each of said groups being equal to the number of magnetic disk communication means; and a switch control means for changing connection of buses provided between said external communication means, said plurality of magnetic disk communication means and the memory devices in said first and second groups, wherein in a first status communication is enabled between the memory devices in said second group and said external communication means, said plurality of magnetic disk communication means and the memory devices in said first and second groups, wherein in a second status communication is enabled between the memory devices in said first group and said external communication means individually for each pair of a memory device and a magnetic disk communication means while communication is enabled between said first group and said external communication means individually for each of the memory devices in said first group, and in a second status communication is enabled...
between memory devices in said second group and said external communication means individually for each of the memory device in said second group while communication is enabled between memory devices in said second group and said external communication means individually for each of a memory device and a magnetic disk communication means.

[0012] In the above-mentioned information storage controller, the first and second memory groups perform a work with the external communication means or with the magnetic disk communication means alternately by the switch means, and each memory group performs work in parallel. Then, information transmission speed is improved.

[0013] An advantage of the invention is that write speed and read speed to and from the magnetic disks can be increased by using the first memory group, the second memory group and the switch means for changing work state.

[0014] Further, another advantage of the invention is that, by providing an exclusive redundant information generation circuit, generation of redundant information or verification and recovery of data can be performed at a high speed, and parallel work by the switch means becomes more efficient in the information storage controller.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and other objects and features of the present invention will become clear from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings, and in which:

Fig. 1 is a block diagram on a structure of an information storage controller of an embodiment of the invention;
Fig. 2 is a block diagram of a redundancy information generation unit;
Fig. 3 is a timing chart of the generation of redundant information;
Fig. 4 shows an example of a parity generator used in the redundant information generation unit;
Fig. 5A is a block diagram of a switch in the switch means, and Fig. 5B is a block diagram of an example of the switch;
Fig. 6 is a timing chart of data write to a magnetic disk in the embodiment; and
Fig. 7 is a timing chart of data output to an external communication means in the embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] Referring now to the drawings, wherein like reference characters designate like or corresponding parts throughout the several views, Fig. 1 shows an information storage controller of an embodiment of the invention. Two memory groups, a first memory group 10 and a second memory group 11 are provided in correspondence to the six magnetic disks. The first memory group 10 and the second memory group 11 comprise six memories 21, 22, 23, 24, 25, 26 and 31, 32, 33, 34, 35, 36, respectively. A central processing unit (hereinafter referred to as CPU) 1 is connected through a CPU bus 13 to six switches 41, 42, 43, 44, 45, 46 in the switch means 12 and sends a control signal therefor. Each switch 41 - 46 is connected to a memory in the first memory group 10 and to a counterpart memory in the second memory group 11. That is, the switch 41 - 46 selects one of the pair of the memories according to the control signal received from the CPU 1, so as to send information stored in one of the memories through an external communication means 2, made of a component such as NCR 53C720, to an external equipment, or to one of the magnetic disk HD1 - HD6 through a redundant information generation unit 3 and one of magnetic disk communication means 4, 5, 6, 7, 8, 9 (hereinafter referred to as HD communication means) made of a component such as NCR 53C720. The information storage controller controls six magnetic disks HD1, HD2, HD3, HD4, HD5 and HD6 connected thereto. In this example, the hard disk drive connected to the HD communication line 4 is referred to as HD1, the hard disk drive connected to the HD communication line 5 is referred to as HD2, the hard disk drive connected to the HD communication line 6 is referred to as HD3, the hard disk drive connected to the HD communication line 7 is referred to as HD4, the hard disk drive connected to the HD communication line 8 is referred to as HD5, and the hard disk drive connected to the HD communication line 9 is referred to as HD6.

[0017] The CPU 1 is connected through a bus 14 to a contact point 15 for opening or closing a connection of the CPU bus 13 with the bus 14 and to six contact points 16 to be opened or closed on communication between the CPU 1, the redundant information generation unit 3 and each HD communication means 4 - 9. The contact point 15 is closed by the CPU 1 to connect the CPU 1 to the external communication means 2, so that a command from the CPU 1 is transmitted to the external communication means 2. When the transmission completes, the external communication means 2 informs the completion to the CPU 1, and the CPU 1 opens the point 15 to allow communication between the external communication means 2 with the switch means 12, while the bus 14 is changed to an open state (or a high impedance state). When the CPU 1 sends a command to the contact point 15, the bus is in the open state, so that no collision of information happens. Similarly, the contact point 16 is closed only when a command is sent from the CPU 1 to each HD communication means 4 - 9 and to the redundant information generation circuit 3, and it is opened when the transmission is completed. In this case, no collision of information happens.

[0018] Fig. 2 shows the redundancy information gen-
Connection of six buses thereof at the contact points 16 to be connected to the six buses M1A - M6A extending from the CPU 1 and to six buses M1B - M6B extending to the switches 41 - 46 and to the HD communication means 4 - 9. Open circles in Fig. 2 show the contact points 16.

When information is received from the external communication means 2 to be stored in a hard disk, the CPU 1 divides the information received from the external communication means 2 to a prescribed amount of data to be stored in the memories in the memory groups 10, 11 at the same area therein. Next, the CPU 1 instructs the redundant information generation unit 3 to generate redundant information by designating a start address in the memory area, a memory region (word number) and a memory for the redundant information to be stored.

In the redundant information generation unit 3, a command detector 33 monitors signals at the bus M1A to detect a command sent from the CPU 1 to the redundant information generation unit 3. A command includes three kinds of information: an address data for an address generator 35 as a memory start address, a channel data for a channel register 33 for designating a memory (bus) for generating redundant information, and a word number for a word counter 32. The command detector 31 detects the command and sets data in the register and the like 32, 33 and 35. When a data is set in the word counter 32, this is informed to a control pulse generator 34. Then, the control pulse generator 34 performs the following work as shown in Fig. 3 on a timing of the generation of redundant information. That is, (a) a r/w signal generated by the control pulse generator 34 is connected to a write line (w) in the bus designated by the channel register 33 among the buses M1A to M6A and to read lines (r) for the other buses. (b) An address signal generated by the address register 33 is connected to the same address for the buses M1A to M6A. (c) Then, an output of a parity generator 36 which generates a parity data on six read data is connected to the bus designated by the channel register 33.

Fig. 4 shows an example of the parity generator 36 used in the redundant information generation unit 3. Data of eight bits from each of the six memories received at six gates 51 - 56 are sent to eight XOR gates 61 - 68 to generate an 8-bit parity data for redundant information to be stored. The gate in correspondence to the memory designated by the channel register 33 does not send signals to the XORs.

Fig. 5A shows an example of the switch 41 - 46 in the switch means 12 comprising a pair of switch units 121 and 122. Buses from the memory 21 - 26 in the first memory group 10 are connected to one input of the switch units 121 and 122, while the counterparts from the memory 31 - 36 in the second memory group 11 are connected to the other inputs thereof. On the other hand, a control signal and an inverted signal thereof are supplied to the switch units 121 and 122. Fig. 5B shows an example of the switch units 121, 122 each comprising CMOS integrated circuits 123 - 128 connected to an address bus, a control bus and a data bus, but the switch units 121, 122 may be made of a gate array.

Data stored at the address are supplied to the parity generator 36 from the memories not designated by the channel register 33, and redundant information is generated according to the data by the parity generator 36. The redundant information is written to the memory designated by the channel register 33. A pulse from the control pulse generator 34 is sent to the address register 35 to increase the address by one, and the address is sent to the word counter 32 to decrease the count by one. As explained above, when the control pulse generator 34 generates a r/w signal, redundant information at a successive address is generated and written to the relevant memory.

In the redundant information generation unit 3, a command detector 33 monitors signals at the bus M1A to detect a command sent from the CPU 1 to the redundant information generation unit 3. A command includes three kinds of information: an address data for an address generator 35 as a memory start address, a channel data for a channel register 33 for designating a memory (bus) for generating redundant information, and a word number for a word counter 32. The command detector 31 detects the command and sets data in the register and the like 32, 33 and 35. When a data is set in the word counter 32, this is informed to a control pulse generator 34. Then, the control pulse generator 34 performs the following work as shown in Fig. 3 on a timing of the generation of redundant information. That is, (a) a r/w signal generated by the control pulse generator 34 is connected to a write line (w) in the bus designated by the channel register 33 among the buses M1A to M6A and to read lines (r) for the other buses. (b) An address signal generated by the address register 33 is connected to the same address for the buses M1A to M6A. (c) Then, an output of a parity generator 36 which generates a parity data on six read data is connected to the bus designated by the channel register 33.

This processing is repeated until the word counter 32 becomes zero. Then, the control pulse generator 34 stops generation of redundant information, and the completion is informed to the CPU 1 with an interrupt signal. Then, the CPU 1 connects the buses M1A to M6A to buses M1B to M6B at the contact points 16.

As explained above, the controller is connected through the HD communication means 4 - 9 to the six hard disk drives HD1 - HD6, and it is needed to specify whether HD connection exists or not and which lines are designated as main lines and spare line. The main line means a line connected to a hard disk drive actually, while the spare line means a line connected to a hard disk drive which is used not actually, but used when a fault arises in one of the hard disks connected to the main lines. That is, when a fault is generated in one of the hard disk drives connected to the main lines, the information in the faulty hard disk drive is generated in the hard disk connected to the spare line according to redundancy information stored therein and the faulty hard disk is not used.

In this embodiment, the main line hard disk drives are connected to the HD communication means 4, 5, 6, 7 and 8, while the spare line hard disk is connected to the HD communication means 9.

The external communication means 2 communicates with the HD communication means 4, 5, 6, 7, 8 and 9 with direct memory access (called as DMA) independently of the CPU 1. Further, the external communication means 2 and the HD communication means 4, 5, 6, 7, 8 and 9 use small computer system interface (SCSI) standard, and a write or read instruction by the CPU 1 specifies a logic block address and a transmission block number. A logic block usually consists of 512 bytes.

Each switch 41 - 46 in the switch means 12 is operated according to a control signal generated by the CPU 1. When memories in the first memory group 10 are connected to the bus 14, memories in the second
memory group 11 are connected to the redundant information generation unit 3 (referred to as state A), while when memories in the first memory group 10 are connected to the redundant information generation unit 3, memories in the second memory group 11 are connected to the bus 14 (referred to as state B).

[0029] Further, the contact points 15 and 16 are opened or closed when a request or an instruction is communicated by the CPU 1 through the buses M1A - M6A, the external communication means 2, HD communication means 4 - 9 and the like, if necessary.

[0030] When information in the memories is output through the external communication means 2, the CPU 1 instructs hard disk drives through the HD communication means 4 - 9 to read information in the same designated area from the same designated address. The informations read from each hard disk drive are stored in a relevant memory. When a hard disk drive is found to have a fault, the CPU 1 designates a memory in correspondence to the fault hard disk drive and instructs generation of redundant information corresponding with those stored in the fault hard disk drive. The generation of the redundant information is similar to that on storing information explained above. If no hard disk drive has a fault, it is not needed to restore the information according to the redundant information.

[0031] An operation of the information storage controller of the embodiment is explained below. In a case explained below, the information storage controller is connected to five hard disks HD1 - HD5. First, an operation is explained when information from the external equipment is written to one or more magnetic disks. Fig. 6 shows a timing chart of this operation. The external communication means 2 first analyzes an instruction from the external equipment to detect a write request. In response to the request, the CPU 1 changes the switch means 12 (switches 41 - 46) to the state A. Next, the CPU 1 instructs transmission of information D1 of one block (512 bytes) to the memory 21 in the first memory group 10. The external communication means 2 transmits the read information D1 successively, and after the transmission of one block completes, the external communication means 2 informs the CPU 1 of the completion by an interrupt signal. Similarly, the informations D2, D3 and D4 are transmitted through the external communication means 2 to the memories 22, 23 and 24, successively.

[0032] After the transmission, the CPU 1 changes the switch means 12 to the state B. Thus, a work between each HD communication means 4 - 9 and the first memory group 10 is possible, and a work between the external communication means 2 and the second memory group 11 is also possible.

[0033] Similarly to in the state A, informations D5, D6, D7 and D8 are transmitted to the memories 32, 33, 34 and 35 in the second memory group 11. In parallel to this operation, the CPU 1 instructs the redundant information generation circuit 3 to generate redundant information P1 by reading the informations D1, D2, D3 and D4 stored in the memories 21, 22, 23 and 24 and writing it to the memory 25. The redundant information generation circuit 3 reads data in the memories 21, 22, 23 and 24 simultaneously for each byte, generates the redundant information P1 by the parity generator 36 and writes it to the memory 25 by the channel register 33. The redundant information generation unit 3 performs this operation on one block, and sends an interrupt signal to the CPU 1 to inform the completion of the operation. Then, the CPU 1 instructs to write the informations D1, D2, D3 and D4 and the redundant information P1 to the hard disk drives. In this stage, the redundant information generation unit 3 only passes each information there through.

[0034] The HD communication means 4, 5, 6, 7 and 8 write the information in the memories to hard disk drives HD1, HD2, HD3, HD4 and HD5, respectively, and each HD communication means 4 - 8 informs completion of write to the CPU 1 with an interrupt signal. Then, the CPU 1 changes the switch means 12 to the state A.

[0035] The above-mentioned operation is continued by cycling the hard disk drive to which the redundant information is written until a work on all the information is written completely.

[0036] Next, it is explained that information in the hard disks is read to be output to the external communication means 2. Fig. 7 is a timing chart in this operation. First, the external communication means 2 analyzes an instruction from the external equipment to detect a read instruction. The CPU 1 changes the switch means 12 to the state B in correspondence to the instruction, to allow a work between each HD communication means 4 - 8 and the memories in the first memory group 10. Next, the CPU 1 instructs the HD communication means 4 to read data of one block from the hard disk drive HD1 to the memory 21. Similarly, it instructs read of data from the HD communication means 5, 6, 7 and 8 to the memories 22, 23, 24 and 25. This read operation to each memory of the first memory group 10 is performed in parallel. In this case, the redundant information generation circuit 3 only passes each information there through. Each HD communication means 4 - 8 informs completion of the read operation to the CPU 1 with an interrupt signal. When the read operation is not completed within a predetermined time, it is decided that the hard disk drive has a fault. A fault hard disk is also found when a hard disk drive is found to have a fault in status confirmation thereon. A fault hard disk drive is not used for read operation.

[0037] If there is a fault hard disk drive, the CPU 1 enables write to the memory in correspondence to the faulty hard disk drive and instructs the redundant information generation circuit 3 to recover the data. If there is no fault hard disk drive, this recovery is not needed. However, verification of information is performed. That is, when information is read from the magnetic disks, information is read simultaneously from a designated
address of the memories not in correspondence to the faulty hard disk drive. Redundant information is generated from the read information, and the redundant information is verified on the information at the address of the memories not in correspondence to the faulty hard disk drive.

[0038] After completion of read or recovery of data when a faulty hard disk drive is found, the CPU 1 changes the switch means 12 to the state A. Similarly to in the state B, the CPU 1 instructs each HD communication means 4 - 8 to read a block of data from a specified address in the memories in the second memory group 11. Each HD communication means 4 - 8 informs completion of read with an interrupt signal to the CPU 1. In parallel to this operation, the CPU 1 instructs the external communication means 2 to output the information D1 of one block in the memory 21 to the external equipment. The completion of output of one block is informed by the external communication means 2 to the CPU 1 with an interrupt signal. The CPU 1 instructs the external communication means 2 to output the information D2 of one block in the memory 22. Similarly, the CPU 1 also instructs the external communication means 2 to output the information D3 and D4 of one block in the memories 23 and 24, respectively. After the completion of the output of the information, the switch means 12 is changed to the state B. The above-mentioned operation is performed until processing on all the information to be read is completed.

[0039] As explained above, in this embodiment, a combination of the external communication means 2 and each HD communication means with the first and second memory groups alternately is changed by the switch means 12 for parallel work. Thus, speeds of write to and read from the hard disk drives can be increased. In this embodiment, because a bus is provided for each hard disk drive, work can be performed in parallel completely. Therefore, processing speed becomes faster than a case with a single bus used in time sharing.

[0040] The external communication means 2 uses SCSI standards, but another type of communication technique may also be used.

[0041] In this embodiment, the number of the magnetic disks is six (five main lines and one spare line). However, it is not limited to this example.

[0042] The redundant information generation unit 3 is provided between each memory and each magnetic disk communication means in this embodiment. However, the redundant information generation unit 3 may be connected to each memory in the memory group 10, 11 used for a work with the magnetic disk communication means 4 - 9, while each memory in the memory group 10, 11 used for a work with the magnetic disk communication means 4 - 9 is connected to each magnetic disk communication means, not through the redundant information generation unit 3. Further, though the redundant information unit 3 is provided in the controller in this embodiment, if the controller is operated in a state such as RAID-0 which needs no redundant information, the redundant information generation unit 3 need not be provided so that the magnetic disk communication means are connected directly to each memory.

[0043] Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art.

Claims

1. An information storage controller for controlling write and read of information to and from magnetic disks, the controller comprising:

- an external communications means (2) for communicating information with an external equipment;
- a plurality of magnetic disk communication means (4-9) for communicating information with a plurality of magnetic disks; characterized by

first (10) and second (11) memory groups, each consisting of a plurality of memory devices, wherein the number of memory devices in each of said first and second memory groups (10, 11) being equal to the number of magnetic disk communication means (4-9), where each said magnetic disk communication means (4-9) is pair wise associated with one of said plurality of memory devices within each one of said two memory groups (10,11);

- buses (13,14) provided between said external communication means (2), said plurality of magnetic disk communication means (4-9) and the plurality of memory devices in said first and second memory groups (10,11); and;

- a switch control means for changing the connection of said buses (13, 14) provided between said external communication means (2), said plurality of magnetic disk communication means (4-9) and the plurality of memory devices in said first and second memory groups (10, 11), wherein, in a first state, communication is enabled between the memory devices in said second memory group (11) and said magnetic disk communication means (4-9) individually for each pair of a memory device and a magnetic disk communication means (4-9) while communication is enabled between said first memory group (10) and said external communication means (2) individually for each of the memory devices in said first memory group (10), and, in a second state, communication is enabled between memory devices in said second memory group (11) and said external com-
munication means (2) individually for each of the memory devices in said second memory group (11) while communication is enabled between memory devices in said second memory group (11) and said external communication means (2) individually for each of the memory devices and a magnetic disk communication means (4-9).

2. The information storage controller according to Claim 1, further comprising a redundant information generation circuit, the redundant information generation circuit comprising a means, when information is written to the magnetic disks, for reading information simultaneously from a designated address of one or more designated memories among said memory group connected to said magnetic disk communication means by said switch means to generate redundant information from the information read simultaneously and for writing the redundant information to an address of a memory different from the designated one or more memories.

3. The information storage controller according to Claim 2, the redundant information generation circuit further comprising a means, when information is read from the magnetic disks, for reading information simultaneously from a designated address of one or more designated memories among said memory group used for work with said magnetic disk communication means, generating redundant information from the information read simultaneously and verifying the redundant information to information at an address of a memory different from the designated one or more memories.

4. The information storage controller according to Claim 1, wherein said switch control means comprises a switch means which connects memories in said first memory group to said external communication means and memories in said second memory group to said magnetic disk communication means and vice versa.

Patentansprüche

1. Informationsspeicher-Steuervorrichtung zum Steuern des Schreibens von Informationen auf und zum Lesen von Informationen von Magnetdisks, wobei die Steuervorrichtung enthält:

   ein externes Kommunikationsmittel (2) zum Datenaustausch mit einem externen Gerät; und

   eine Vielzahl von Magnetdisk-Kommunikationsmitteln (4-9), zum Datenaustausch mit einer Reihe an Magnetdisks; gekennzeichnet durch eine erste (10) sowie eine zweite (11) Speichergruppe, wobei jede Speichergruppe aus einer Reihe an Speichereinrichtungen besteht, wobei die Zahl der Speichereinrichtungen in sowohl der ersten als auch in der zweiten Speichergruppe (10, 11) gleich der Zahl an Magnetdisk-Kommunikationsmitteln (4-9) ist, wobei jedes Magnetdisk-Kommunikationsmittel (4-9) mit einer der Speichereinrichtungen innerhalb jeder der beiden Speichergruppen (10, 11) paarweise zusammenwirkt; Busse (13, 14), die zwischen den externen Kommunikationsmitteln (2), der Reihe an Magnetdisk-Kommunikationsmitteln (4-9) und der Reihe an Speichereinrichtungen in der ersten sowie der zweiten Speichergruppe (10, 11) vorgesehen sind; und ein Schaltersteuermittel zum Ändern der Verbindung der Busse (13, 14), die zwischen den externen Kommunikationsmitteln (2), der Reihe an Magnetdisk-Kommunikationsmitteln (4-9) und der Reihe an Speichereinrichtungen in der ersten und der zweiten Speichergruppe (10, 11) vorgesehen sind, wobei in einem ersten Zustand die Übertragungsverbindung zwischen den Speichereinrichtungen in der zweiten Speichergruppe (11) und den Magnetdisk-Kommunikationsmitteln (4-9) für jedes Paar aus einer Speichereinrichtung und einem Magnetdisk-Kommunikationsmittel (4-9) individuell ermöglicht ist, während die Übertragungsverbindung zwischen der ersten Speichergruppe (10) und den externen Kommunikationsmitteln (2) für jede der Speichereinrichtungen in der ersten Speichergruppe (10) individuell ermöglicht ist, und wobei in einem zweiten Zustand die Übertragungsverbindung zwischen den Speichereinrichtungen in der zweiten Speichergruppe (11) und den externen Kommunikationsmitteln (2) für jede der Speichereinrichtungen in der zweiten Speichergruppe (11) individuell ermöglicht ist.

2. Informationsspeicher-Steuervorrichtung nach Anspruch 1, weiterhin enthaltend eine redundante Informationserzeugungsschaltung, die ein Mittel enthält, um Informationen aus einer vorgegebenen Adresse aus einem oder mehreren vorgegebenen Speichern aus der Speichergruppe, die mit dem Magnetdisk-Kommunikationsmittel über das Schaltmittel verbunden ist, simultan zu lesen, wenn Informationen auf die Magnetdisk geschrieben wer-
1. Contrôleur de stockage d’informations pour commander l’écriture et la lecture d’informations vers et depuis des disques magnétiques, le contrôleur comprenant :

un moyen de communication externe (2) pour communication des informations avec un équipement externe ; et

une pluralité de moyens de communication de disques magnétiques (4 à 9) pour communication des informations avec une pluralité de disques magnétiques ; caractérisé par

des premier (10) et second (11) groupes mémoires, chacun étant constitué d’une pluralité de dispositifs mémoires, dans lequel le nombre des dispositifs mémoires dans chacun desdits premier et second groupes mémoires (10, 11) est égal au nombre des moyens de communication du disque magnétique (4 à 9), où chaque dit moyen de communication de disques magnétiques (4 à 9) est apparié à un de ladite pluralité des dispositifs mémoires à l’intérieur de chacun desdits deux groupes mémoires (10, 11)

2. Contrôleur de stockage d’informations selon la revendication 1, comprenant, en outre, un circuit de génération d’informations redondantes, le circuit de génération d’informations redondantes comprenant un moyen, lorsque les informations sont écrites sur les disques magnétiques, pour lire simultanément les informations depuis une adresse désignée d’une ou plusieurs mémoires désignées parmi lesdits. groupes mémoires connectés audit moyen de communication de disques magnétiques dans ledit moyen de commutation pour générer les informations redondantes à partir des informations lues simultanément et pour écrire des informations d’adresse redondante à une adresse de mémoire différente d’une mémoire désignée et de plusieurs mémoires désignées.

3. Contrôleur de stockage d’informations selon la revendication 2, le circuit de génération d’informations redondantes comprenant un moyen, lorsque les informations sont lues à partir des disques mag-
gnétiques, pour lire les informations simultanément à partir d'une adresse désignée d'une ou plusieurs mémoires désignées parmi lesdits groupes mémoires utilisés pour l'opération avec ledit moyen de communication du disque magnétique, pour générer les informations redondantes à partir des informations simultanément lues et pour vérifier les informations redondantes comme information à une adresse mémoire différente de l'une ou plusieurs mémoires désignées.

4. Contrôleur de stockage d'informations selon la revendication 1, dans lequel ledit moyens de commande de commutation comprend un moyen de commutateur qui connecte les mémoires dans ledit premier groupe mémoire audit moyen de communication externe et les mémoires dans ledit second groupe mémoire audit moyen de communication du disque magnétique et vice-versa.
Fig. 1
Fig. 6

First memory group

Second memory group

State A

State B

Time

D1 D2 D3 D4

D5 D6 D7 D8

D9 D10 D11 D12

write

write

P1

P2