## EUROPEAN PATENT SPECIFICATION

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### (54) Failure tolerant memory device, in particular of the flash EEPROM type

Fehlertolerantes Speichergerät, insbesondere des Typs "flash EEPROM"

Dispositif de mémoire défaillant aux pannes, en particulier de type "flash EEPROM"

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### (73) Proprietor: **STMicroelectronics S.r.l.**

20041 Agrate Brianza (Milano) (IT)

### (72) Inventors:

- **Campardo, Giovanni**
  I-24100 Bergamo (IT)
- **Camerlenghi, Emilio**
  I-24100 Bergamo (IT)

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### (74) Representative: **Botti, Mario**

Botti & Ferrari S.r.l.
Via Locatelli, 5
20124 Milano (IT)

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Description

[0001] The present invention relates to a memory device and in particular a flash EPROM in accordance with the preamble of claim 8 and a method for discriminating a gain-based insulated-gate single memorisation-transistor memory cell and to a method of deleting a memory cell of the same type. The memory device in accordance with the present invention can find advantageous application also in integrated circuits such as microprocessors and microcontrollers.

[0002] In the area of non-volatile semiconductor memories, presently comprising the UVEPROM, EEPROM and flash EPROM, the memory device consists of a matrix of equal cells which comprise for the memorisation of the data a single MOS transistor having at least one insulated gate. The value 0 or 1 of the data memorised depends on the amount of charges present on the insulated gate which in turn determines the threshold voltage of the MOS transistor.

[0003] As known, with the matrix must be connected row and/or column address decoding means and a control logic for reading, writing and deletion of the matrix cells.

[0004] There are often provided in the matrix one or more redundant rows and/or one or more redundant columns. These are used during manufacturing testing to obviate manufacturing defects by replacing the rows or columns containing faults with redundant rows or columns.

[0005] A memory system having a two dimensional array of EEPROM or Flash EEPROM cells is known from the international patent application No. WO 94/07211 filed on September 1, 1993 in the name of Sundisk Corporation.

[0006] In particular such a document describes a matrix of memory cells having a plurality of rows and columns, decoding means for row and/or column address decoding, and a control logic for writing, reading and deletion of the cells, said control logic providing for the identification of cell faults in order to replace defective cells by good ones.

[0007] International patent application No. WO 94/07211 reflects the features of the preamble of claims 1 and 8.

[0008] Moreover, the UK Patent Application No. 2 254 173 filed on January 30, 1992 in the name of Intel Corporation describe a method and apparatus for providing row redundancy in EEPROM devices, using a content addressable memory for storing the information indicating defective cells.

[0009] FIG. 1 shows a flash EPROM cell matrix with 2 rows and 3 columns.

[0010] Various well known mechanisms are used for the programming and deletion operation which can take place either globally, i.e. they affect the entire matrix, or selectively. The reading operation consists of applying to the selected cell a polarisation voltage (for writing) and detecting the corresponding current (for writing) and in comparing it with appropriate reference currents.

[0011] In particular in flash EPROM memories, reading and programming are selective while deletion is done electrically and globally.

[0012] Almost always, the programming and deletion operations take place by means of a series of identical successive phases. For programming, injection of ‘hot electrons’ and, for deletion, extraction of charges by the Fowler-Nordheim effect. After each individual programming or deletion phase there is a phase of verification of the charge present on the insulated gate of each cell. In this manner the charge status and consequently the threshold voltage of the individual cells can be controlled with great precision.

[0013] FIG. 2 shows in a simplified manner the gate voltage versus channel current characteristics of cells having different charge status. In particular, A0 indicates the characteristic of a cell at instant t0 having a threshold voltage VT(t0) and gain G1 while A1 indicates the characteristic of the same cell at instant t1, following t0, after a deletion phase and thus having the same gain G1 but threshold voltage VT(t1) lower than VT(t0).

[0014] The verification phase consists of a particular reading operation performed with particular reference currents more restrictive than those used for the normal reading operation.

[0015] In flash EPROM devices it is extremely important that all the cells ‘experience the same history’, i.e. they must be programmed and deleted the same number of times. For this reason, before the actual deletion there is a programming operation of all the cells denominated ‘preconditioning’.

[0016] After the ‘preconditioning’ operation, all the cells have a threshold voltage higher than a pre-set value VT0. The characteristic indicated by A2 in FIG. 2 having a reference gain G represents the limit of the programming condition while after the subsequent deletion operation all the cells have a threshold voltage lower than a pre-set value VT1. The characteristic indicated by A3 in FIG. 2 having the same reference gain G represents the limit of the deletion condition. The values VT0 and VT1 depend on the manufacturing process and design choices. A possible choice could be 5V for VT0 and 2V for VT1 respectively.

[0017] Ideally all the memory cells are deleted with the same speed and hence, after the deletion operation the threshold voltage values of the various cells are found in a small area slightly below the value VT1.

[0018] During laboratory experiments and manufacturing tests some phenomena were found which degrade the performance and life of flash EPROM devices.

[0019] There are cells which are deleted more rapidly than others. This phenomenon leads to the fact that when the deletion operation is completed their threshold voltage can be lowered much below VT1, as with the characteristic A5 and some times to a level, in general less than 0V as in the case of the characteristic A6, such
as to become an irreversible lowering 'emptied cell' or 'depleted bit'. This can generate errors during writing operations because said cells conduct current even when they are not selected.

[0020] There are cells which are deleted more slowly than others because their transconductance, and hence their gain and reading current, is lower than average. The characteristic indicated by A4 in FIG. 2 belongs to a cell of this type having gain G2. This phenomenon is found in manufacturing testing and during the life of the device and leads to the fact that when the deletion operation is terminated the cells having normal transconductance, i.e. nearly all, have reached extremely low threshold voltages often less than 0V. This leads to the shortcomings mentioned above and can also lead to degradation of a large part of the cell matrix. In addition it is also possible that the deletion operation will not end in the maximum time limits provided.

[0021] Heretofore it was sought to identify these situations and rectify them during manufacturing testing. The purpose of the present invention is to provide a method capable of identifying these situations during normal operation of the device and rectify them, in the light of the found and unexpected fact that they can arise even during the life of the device, and provide a memory device which would be tolerant of 'fault' situations like these and in particular gain lowering.

[0022] This purpose is achieved by a method for discrimination of a memory cell having the characteristics set forth in claim 1, and by a memory device having the characteristics set forth in claim 8. Additional advantageous aspects of the present invention are set forth in the dependent claims.

[0023] Since fault phenomena such as those discussed occur during normal operation the present invention proposes that in the memory device the decoding means comprise at least one non-volatile memory for address mapping and that the control logic comprise means for identifying cell faults in the rows and/or columns of the matrix and writing means designed for writing on said non-volatile memory during normal operation addresses corresponding to the redundant rows and/or columns to rectify said faults.

[0024] In addition it is possible to not degrade the cell matrix even in the presence of lowered gain cells by foreseeing that these will be identified and that during the deletion operation the deletion status will occur only for the non-lowered gain cells.

[0025] The present invention is clarified by the following description together with the annexed drawings wherein:

FIG. 1 shows a memory cell matrix,

FIG. 2 shows in a simplified manner in a Cartesian voltage-current diagram the characteristics of some memory cells having different threshold voltages,

FIG. 3 shows in a simplified manner in a Cartesian voltage-current diagram the characteristics of some memory cells having different gains,

FIG. 4 shows a flow chart of a discrimination method in accordance with the present invention,

FIG. 5 shows a flow diagram of a deletion method in accordance with the present invention, and

FIG. 6 shows a block diagram of a memory device in accordance with the present invention.

[0026] FIG. 3 shows a series of characteristics of cells all having different gains and a common point P1 identified by the co-ordinates V1, I1, i.e. by applying the reading voltage V1 to all these cells there is obtained therefrom the same reading current I1 and the characteristics are indicated in decreasing order of gain and threshold voltage by B0 (with gain G0 and threshold voltage VT(B0)), B1 (with gain G1 and threshold voltage VT(B1)), B2 (with gain G2 and threshold voltage VT(B2)) respectively. The voltages VT0 and VT1 keep the same meaning explained above.

[0027] The method in accordance with the present invention for discriminating on the basis of the gain a memory cell of the type with single insulated-gate memory transistor comprises the following phases:

a. carry the insulated gate of the cell in a charge state such that by applying a first reading voltage V1 to the cell by means of successive programming and/or deletion and verification phases there is detected a first reading current about equal to a first value I1 (as shown in FIG. 3),

b. apply a second reading voltage V2,

c. detect a second reading current I(V2) opposite the second reading voltage V2,

d. compare the value of the second reading current I(V2) with a second value I2 which together with the second reading voltage V2 identifies a point P2, and

e. associate the cell alternatively with a first or a second class of cells based on the outcome of said comparison.

[0028] Specifically for the purposes of the present invention it proved advantageous to have the second reading voltage V2, e.g. 6.25V, higher than the first reading voltage V1, e.g. 4.5V, the second value I2 higher than the first value I1, and the cell associated with a first class of high-gain cells if from said comparison it proved that said second reading current I(V2) was higher than said second value I2 and otherwise with a second low-gain cell class.
The discrimination method can be rapidly understood by considering the description made together with the flow chart shown in FIG. 4, having the following block-actions correspondence:

100 method start
110 cell conditioning - phase a. of the method
101 apply V1
102 detect I(V1)
103 test on I(V1) in relation to I1
104 deletion phase
105 programming phase
120 apply V2 - phase b. of the method
130 detect I(V2) - phase c. of the method
140 test on I(V2) in relation to I2 - phase d. of the method
150 high-gain association - end of method phase e.
160 low-gain association - end of method phase e.

The one shown in FIG. 3 could be the situation which appears in three cells of an EPROM flash memory device after phase a. of the method in accordance with the present invention. By applying to the three cells the second reading voltage V2 there will be detected the currents I(BO), I(B1), I(B2) respectively of which the first two are higher than the second value I2 while the last, i.e. I(B2), is not. For the purposes of the present method therefore the first two cells will be considered high-gain and the last low-gain. Graphically it can be seen that the characteristics slope reflects this situation.

It is specified lastly that the real form of the cell characteristics is not the rectilinear type but their qualitative behaviour, for the purposes of the graph and method, is the same.

It remains to be discussed how to perform practically in a physical memory device phase d. of the method, i.e. the current comparison. This can be done, e.g. by using a reference memory cell having the BRIF characteristic having a reference gain GRIF and brought to a threshold voltage VT(BRIF) such that by applying thereto the second reading voltage V2 the reading current I2 is detected, and sending to a sense amplifier the currents of the reference cell and of the cell to be discriminated. Current comparisons by means of sense amplifiers and reference cells are used normally in reading operations and in programming and deletion verification phases using appropriate reference cells. Thus to discriminate the cells on the basis of gain basically no further circuitry in the memory device is necessary.

Since the low cell gain problem becomes, as explained above, particularly dangerous for the memory device when one prepares to delete it, the ideal moment for performance of a discrimination phase is concomitantly with the deletion operation.

As explained above, a conventional deletion operation of the cells of a memory device of the insulated-gate single-transistor memorisation type, in particular the EPROM flash type, consists of at least one series of successive individual deletion and verification phases of the cell deletion status.

The deletion method in accordance with the present invention comprises also at least one individual cell discrimination phase on the basis of the gain suitable for identifying the high-gain cells and provides that, after said discrimination phase, the individual verification phases affect only the high-gain cells.

In this manner it is avoided that many cells be ‘depleted’.

The discrimination phase can be provided by any method.

It is particularly advantageous to use the discrimination method in accordance with the present invention immediately after the ‘preconditioning’ and before the actual deletion because in this case, if a value of V1 lower than the value of VT0 is chosen, the discrimination phase already carries a partial but not dangerous deletion of the cells which thus shortens the actual deletion. As a whole then the deletion performed with the
method of the present invention is not basically longer than that of the known art but considerably safer.

[0042] All these operations can affect the entire memory device or blocks thereof.

[0043] The cells which are not high-gain are considered faulty and possibly signalled as such to the user of the device. In a very simple case the user will avoid using them.

[0044] A more sophisticated version of the method provides that at least the faulty cells are replaced with redundant cells. More often it happens that the entire row or column to which they belong is replaced.

[0045] In this last case, for reasons of uniformity of use of all the cells of the matrix, it is well that all the redundant cells experience on average the same life as the non-redundant cells before their replacement. To achieve this it is necessary that the preconditioning and subsequent deletion affect always also the redundant cells.

[0046] It has been seen that various 'fault' phenomena affect the memory devices during their life and among these lowering of the cell gain.

[0047] There is now explained with the aid of FIG. 6 the memory device in accordance with the present invention which is fault tolerant. It comprises:

a.) matrix MAT of memory cells having a plurality of rows and columns of which at least one row and/or column RID is redundant,

b.) decoding means RDEC, CDEC for row and/or column addresses, and

c.) control logic CL for writing, reading and deletion of the cells and control of the device components.

[0048] The memory device also comprises means for applying a voltage to the gate terminal of cell, and means for detecting a current through the cell channel.

[0049] The decoding means RDEC, CDEC comprise at least one non-volatile memory NVM for address mapping and the control logic CL comprises means TST designed to identify cell faults in the rows and/or columns and writing means WM designed to write on the non-volatile memory NVM, during normal operation of the device, addresses corresponding to said at least one redundant row and/or column RID to rectify said faults.

[0050] In the example of FIG. 6 there is a matrix MAT made up of 8 rows and 8 columns, only one redundant column RID, a 3-bit row decoder RDEC, a 3-bit column decoder CDEC, and a non-volatile memory NVM formed from 8 3-bit words, used only for mapping column addresses and included in the 3-bit column decoder CDEC.

[0051] From the control logic CL comes out the column address to be sent to the 3-bit column decoder CDEC, the row address to be sent to the 3-bit row decoder RDEC, and at least one signal DEL for the deletion to be sent to the matrix MAT. Furthermore it is connected to the input of the 3-bit row decoder RDEC and the input of the 3-bit column decoder CDEC. The means TST pilot the writing means WM which are connected in writing to the non-volatile memory NVM.

[0052] Initially the non-volatile memory NVM contains in order the following eight words: 000, 001, 010, 011, 100, 101, 110, 111.

[0053] When the means TST identify a 'fault' among those foreseen in a particular cell, they send to the writing means WM the column address corresponding to said faulty cell, e.g. 011.

[0054] The writing means WM use this address to address the non-volatile memory NVM and use as writing data the column address corresponding to the redundancy column, in the example 111, and perform a writing operation on the non-volatile memory NVM.

[0055] At the end the non-volatile memory NVM contains in order the following eight words: 000, 001, 010, 111, 100, 101, 110, 111.

[0056] In the example there is no possibility of rectifying additional 'faults'.

[0057] The design and realisation of such a control logic CL falls within the normal activities and abilities of those skilled in the art.

[0058] It is clear that control of the entire device is entrusted to the control logic CL which can be the wired or programmed type. For deletion, this can be pre-set to operate in accordance with the method of the present invention.

[0059] The means TST can be in particular individual discrimination means for the cells of the matrix MAT which can consist of logics of the wired or programmed type and operate, e.g. in accordance with the method of the present invention.

[0060] A fault tolerant memory device in accordance with the present invention can find an advantageous application in any integrated circuit where it is necessary to store data and/or programs.

Claims

1. Method of discriminating a memory cell of the single-transistor insulated gate memorisation type based on gain characterised in that it comprises the following phases:

a) carry the insulated gate of the cell in a charge state such that by applying a first reading voltage (V1) to the gate terminal of the cell by means of successive programming and/or deletion and verification phases there is detected a first reading current (I(V1)) through the cell channel about equal to a first value (I1),

b) apply a second reading voltage (V2) to the gate terminal of the cell, said second reading
voltage (V2) differing from said first reading voltage (V1),
c) detect a second current (I(V2)) through the cell channel corresponding to the second reading voltage (V2),
d) compare the value of the second reading current (I(V2)) with a second value (I2), and
e) associate the cell alternatively with a first or a second class of cells based on the outcome of said comparison.

2. Method in accordance with claim 1 in which said second reading voltage (V2) is higher than said first reading voltage (V1) and in which said second value (I2) is higher than said first value (I1) and in which said cell is associated with a first class of high-gain cells if from said comparison it proves that said second reading current (I(V2)) is higher than said second value (I2) and otherwise is associated with a second class of low-gain cells.

3. Method according to claim 1, further comprises at least one series of successive deletion and individual verification phases of the cell deletion state, said individual verification phases affecting only the high-gain cells.

4. Method in accordance with claim 3 in which said discrimination phase takes place in accordance with the method set forth in claims 1 or 2 before said series of successive deletion and verification phases.

5. Method in accordance with claim 3 or 4 in which the cells not high-gain are considered faulty.

6. Method in accordance with claim 5 in which at least said faulty cells are replaced by redundant cells.

7. Method in accordance with claim 6 in which said redundant cells experience on average the same life as the non-redundant cells before said replacement.

8. Memory device of the type comprising:
   a.) matrix (MAT) of memory cells having a plurality of rows and columns of which at least one row and/or column (RID) is redundant,
   b) decoding means (RDEC,CDEC) for row and/or column addresses,
   c.) control logic (CL) for writing, reading and deletion of the cells and control of the device components,
   d) means for applying a voltage to the gate terminal of cell, and
e) means for detecting a current through the cell channel,
characterised in that said decoding means (RDEC, CDEC) comprise at least one non-volatile memory (NVM) for mapping said addresses and that said control logic (CL) comprises means (TST) designed to identify cell faults in said rows and/or columns by comparing the cells' gains and writing means (WM) designed to write on said non-volatile memory (NVM) addresses corresponding to said at least one redundant row and/or column (RID) to rectify said faults.

9. Device in accordance with claim 8 in which said control logic (CL) comprises additionally discrimination means (TST) for said cells on the basis of gain and designed to pilot said writing means (WM).

10. Device in accordance with claim 9 in which said control logic (CL) operates for deletion in accordance with the method set forth in one of the claims from 3 to 7.

11. Integrated circuit comprising a memory device for storing data and/or programs characterised in that said memory device is the type set forth in claims 8 to 10.

Patentansprüche

1. Verfahren zum Unterscheiden einer Speicherzelle des Ein-Transistor-Speichertyps mit isoliertem Gate auf der Basis ihrer Verstärkung dadurch gekennzeichnet, daß es die nachstehenden Schritte aufweist:
   a) Bringen des isolierten Gates der Zelle in einen Ladezustand derart, daß durch Anlegen einer ersten Lesespannung (V1) an den Gateanschluß der Zelle mittels sukzessiver Programmierungs- und/oder Lösch- und Verifikationsphasen ein erster Lesestrom (I(V1)) durch den Zellenkanal etwa gleich einem ersten Wert (I1) detektiert wird,
   b) Anlegen einer zweiten Lesespannung (V2) an den Gateanschluß der Zelle, wobei sich die zweite Lesespannung (V2) von der ersten Lesespannung (V1) unterscheidet,
   c) Detektieren eines zweiten Lesestroms (I(V2)) durch den Zellenkanal, welcher der zweiten Lesespannung (V2) entspricht,
   d) Vergleichen des Werts des zweiten Lesestroms (I(V2)) mit einem zweiten Wert (I2), und
e) Zuordnen der Zelle alternativ zu einer ersten oder zweiten Klasse von Zellen auf der Basis des Vergleichsergebnisses.

2. Verfahren nach Anspruch 1, in welchem die zweite Lesespannung (V2) höher als die erste Lesespannung (V1) ist, und in welchem der zweite Wert (I2) höher als der erste Wert (I1) ist, und in welchem die Zelle einer ersten Klasse von Zellen mit hoher Verstärkung zugeordnet wird, wenn sich aus dem Vergleich erweist, daß der zweite Lesestrom (I(V2)) höher als der zweite Wert (I2) ist, und ansonsten einer zweiten Klasse von Zellen mit niedriger Verstärkung zugewiesen wird.

3. Verfahren nach Anspruch 1, welches ferner mindestens eine Reihe sukzessiver Lösch- und individueller Verifikationsphasen des Zellenlöschzustandes aufweist, wobei die- individuellen Verifikationsphasen nur die Zellen mit hoher Verstärkung betreffen.


5. Verfahren nach Anspruch 3 oder 4, in welchem die Zellen ohne hohe Verstärkung als fehlerhaft betrachtet werden.

6. Verfahren nach Anspruch 5, wobei mindestens die fehlerhaften Zellen durch redundante Zellen ersetzt werden.

7. Verfahren nach Anspruch 6, in welchem die redundanten Zellen im Durchschnitt denselben Lebensablauf wie die nicht-redundanten Zellen vor der Ersatzsetzung aufweisen.

8. Speichervorrichtung des Typs, welcher aufweist:
   a.) eine Matrix (MAT) aus Speicherzellen mit mehreren Zeilen und Spalten, wovon mindestens eine Zeile und/oder Spalte (RID) redundant ist,
   b.) eine Dekodiereinrichtung (RDEC, CDEC) für Zeilen- und/oder Spaltenadressen,
   c.) eine Steuerlogik (CL) zum Beschreiben, Lesen und Löschen der Zellen und Steuern der Vorrichtungskomponenten,
   d.) eine Einrichtung zum Anlegen einer Spannung an den Gateanschluß einer Zelle, und
e.) eine Einrichtung zum Detektieren eines Stroms durch den Zellenkanal,
dadurch gekennzeichnet, daß die Dekodiereinrichtung (RDEC, CDEC) mindestens einen nicht-flüchtigen Speicher (NVM) zum Zuordnen der Adressen aufweist, und daß die Steuerlogik (CL) eine Einrichtung (TST) aufweist, die für die Identifizierung von Zellenfehlern in den Zeilen und/oder Spalten durch Vergleichen der Zellenverstärkungen ausgelegt ist, und eine Schreibereinrichtung (WM), die zum Beschreiben des nicht-flüchtigen Speichers (NVM) mit Adressen, die der mindestens einen redundanten Zeile und/oder Spalte RID entsprechen, ausgelegt ist, um die Fehler zu beheben.

9. Vorrichtung nach Anspruch 8, in welcher die Steu erlogik (CL) eine zusätzliche Unterscheidungseinrichtung (TST) für die Zellen auf der Basis der Verstärkung aufweist und dafür ausgelegt ist, die Schreibereinrichtung (MW) zu steuern.

10. Vorrichtung nach Anspruch 9, in welcher die Steu erlogik (CL) beim Löschen gemäß dem in einem der Ansprüche 3 bis 7 beschriebenen Verfahren arbeitet.

11. Integrierte Schaltung, welche eine Speichervorrichtung zum Speichern von Daten und/oder Programmen aufweist, dadurch gekennzeichnet, daß die Speichervorrichtung der in den Ansprüchen 8 bis 10 beschriebene Typ ist.

Revendications

1. Procédé en vue de discriminer une cellule de mémoire du type à mémorisation par grille isolée à un seul transistor, en fonction du gain, caractérisé en ce qu’il comprend les phases suivantes : a) porter la grille isolée de la cellule dans un état de charge de sorte qu’en appliquant une première tension de lecture (V1) à la borne de la grille de la cellule au moyen des phases successives de programmation et/ou de suppression et de vérification, un premier courant de lecture (I(V1)) est détecté dans le canal de la cellule sensiblement égal à une première valeur (I1), b) appliquer une seconde tension de lecture (V2) à la borne de la grille de la cellule, ladite seconde tension de lecture (V2) étant différente de ladite première tension de lecture (V1), c) détecter un second courant (I(V2)) dans le canal de la cellule correspondant à la seconde tension de lecture (V2), d) comparer la valeur du second courant de lecture (I(V2)) à une seconde valeur (I2), et e) associer la cellule alternativement à une première ou une seconde classe de cellules en fonction du résultat de cette comparaison.
2. Procédé selon la revendication 1 dans lequel ladite seconde tension de lecture (V2) est supérieure à ladite première tension de lecture (V1) et dans lequel ladite seconde valeur (I2) est supérieure à ladite première valeur (I1) et dans lequel ladite cellule est associée à une première classe de cellules à gain élevé si le résultat de cette comparaison prouve que ledit second courant de lecture (I(V2)) est supérieur à une seconde valeur (I2) et, autrement, est associée à une seconde classe de cellules à faible gain.

3. Procédé selon la revendication 1, comprenant en outre au moins une série de phases successives de suppression et de vérification individuelle de l'état de suppression de la cellule, lesdites phases de vérification individuelles n'affectant que les cellules à gain élevé.

4. Procédé selon la revendication 3 dans lequel ladite phase de discrimination a lieu selon le procédé décrit dans les revendications 1 ou 2 avant ladite série de phases successives de suppression et de vérification.

5. Procédé selon la revendication 3 ou 4 dans lequel les cellules qui ne sont pas à gain élevé sont considérées comme défectueuses.

6. Procédé selon la revendication 5 dans lequel au moins lesdites cellules défectueuses sont remplaçées par des cellules redondantes.

7. Procédé selon la revendication 6 dans lequel lesdites cellules redondantes connaissent en moyenne la même vie que les cellules qui ne sont pas redondantes avant ledit remplacement.

8. Dispositif de mémoire du type comprenant :

   a.) une matrice (MAT) de cellules de mémoire présentant une pluralité de lignes et de colonnes parmi lesquelles au moins une ligne et/ou une colonne (RID) est redondante,

   b.) un moyen de décodage (RDEC, CDEC) pour les adresses de lignes et/ou de colonnes,

   c.) une logique de commande (CL) afin d'écrire, lire et supprimer les cellules et commander les composants du dispositif,

   d.) un moyen en vue d'appliquer une tension à la borne de la grille de la cellule, et

   e.) un moyen en vue de détecter un courant dans le canal de la cellule,

   caractérisé en ce que ledit moyen de décodage (RDEC, CDEC) comprend au moins une mémoire non volatile (NVM) afin de mettre en correspondance lesdites adresses et en ce que ladite logique de commande (CL) comprend un moyen (TST) conçu afin d'identifier les défauts de cellule dans lesdites lignes et/ou colonnes en comparant le gain des cellules et un moyen d'écriture (WM) conçu afin d'écrire sur ladite mémoire non volatile (NVM) des adresses correspondant à ladite ou les dites ligne et/ou colonne redondante (RID) en vue de rectifier lesdits défauts.

9. Dispositif selon la revendication 8 dans lequel ladite logique de commande (CL) comprend par ailleurs un moyen de discrimination (TST) pour lesdites cellules en fonction du gain et conçues afin de piloter ledit moyen d'écriture (WM).

10. Dispositif selon la revendication 9 dans lequel la logique de commande (CL) fonctionne pour la suppression selon le procédé décrit dans l'une des revendications 3 à 7.

11. Circuit intégré comprenant un dispositif de mémoire en vue de stocker des données et/ou des programmes caractérisé en ce que ledit dispositif de mémoire est du type décrit dans les revendications 8 à 10.