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(54) Integrated circuitry for checking the utilization rate of redundancy memory elements in a semiconductor memory device

Integrierte Schaltung zur Überwachung der Benutzung von Redunanzspeicherbauelementen in einer Halbleiterspeichereinrichtung

Circuit intégré de contrôle de l'utilisation des éléments de mémoire redondantes dans un dispositif de mémoire à semi-conducteurs

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Description

The present invention relates to an integrated circuitry for checking the utilization rate of redundancy memory elements in a semiconductor memory device.

In the manufacture of semiconductor memories defects are frequently encountered that afflict a limited number of memory elements in a memory matrix. The reason for the high probability of defects of this type resides in that in a semiconductor memory device the greatest part of the chip area is occupied by the memory matrix, moreover it is in the memory matrix, and not in the peripheral circuitry, that the manufacturing process characteristics are usually pushed to limits.

In order to avoid that the presence of a limited number of defective matrix memory elements on many millions forces the rejection of the entire chip, and therefore to increase the manufacturing process yield, the technique is known of providing for the manufacture of a certain number of additional memory elements, commonly called "redundancy memory elements", to be used as a replacement of those matrix memory elements that, during testing of the memory device, prove defective: the selection circuits, with which the integrated component must necessarily be provided, and which allow the above mentioned functional replacement of a defective matrix memory element with a redundancy memory element are indicated as a whole with the name of "redundancy circuitry", while the set of redundancy memory elements and circuitry is defined for short as "redundancy".

The redundancy circuitry comprises programmable non-volatile memory registers suitable to store those address configurations corresponding to the defective matrix memory elements: such registers are programmed once and for all during the memory device testing, and must retain the information stored therein even in absence of the power supply.

Each non-volatile memory register must therefore be made up of a number of programmable memory cells at least equal to the number of address bits which allows the selection of the matrix memory elements. Each memory cell of a memory register is therefore dedicated to store the logical state of a particular address bit of the address configuration corresponding to a defective matrix memory element, and comprises at least one programmable non-volatile memory element, a circuit for programming the memory element, a circuit for reading the information stored in the memory element and a circuit for comparing said information with the current logical state of the address bit associated to the memory cell.

Since however even unprogrammed non-volatile memory registers, associated to unused redundancy memory elements, store a particular address configuration, i.e. they store that particular address configuration corresponding to the unprogrammed condition of the memory cells, when a non-defective matrix memory element is addressed whose address coincides with the logical configuration of the memory cells in an unprogrammed memory register, the redundancy memory element associated to said unprogrammed register will be selected instead of the non-defective matrix memory element. If in a memory device two or more redundancy memory elements are not used, since the unprogrammed condition is the same for all the memory cells of the non-volatile memory registers, addressing the non-defective matrix memory element whose address coincides with the configuration of the unprogrammed memory cells would cause said two or more redundancy memory elements to be selected simultaneously.

To prevent such unacceptable simultaneous selection, each non-volatile memory register is provided with an additional programmable memory cell (called "guard memory cell" or "control memory cell") which allows the selection of the associated redundancy memory element only in the case it is programmed. This however causes a significant increase in the overall chip area.

In order to evaluate the degree of effectiveness of the manufacturing process, or of a given fabrication lot of memory device chips, it is useful to know for each chip how many redundancy memory elements have been utilized to replace defective matrix memory elements, in other words to perform a "resources check".

Documents W082/02793 and DE-A-4 226 070 show examples of circuitries with indication of redundancy memory elements in use.

According to a known technique, this can be done by putting the memory device in a particular test mode in which all the selection signals for the redundancy memory elements generated by the non-volatile memory registers are ORed together and the resulting signal is supplied to one output buffer driving an output pad of the memory device; the memory device is then sequentially supplied with all the possible address configurations; each time an address configuration corresponding to a defective matrix memory element which has been replaced by a redundancy memory element is supplied to the memory device, the corresponding non-volatile register will activate the selection signal for the redundancy memory element, and this occurrence will be detected by the testing machine by sensing the logical state of said output pad. A given non-volatile memory register will activate the corresponding selection signal if and only if the current address configuration supplied to the memory device coincides with that stored in it, and if the respective guard memory cell is programmed.

This is a lengthy procedure, especially for dense memory devices, wherein the possible address configurations can be several millions; furthermore, the testing machine must keep track of the number of times the output pad changes its logical state.

In a pending European Patent Application in the name of the same Applicant, a redundancy circuitry is described wherein no guard memory cells are required in the non-volatile memory registers; this is achieved by
means of the generation of an inhibition signal which inhibits the activation of the selection signals for the redundancy memory elements each time the memory device is supplied with an address configuration coincident with the logical state stored in a non-programmed non-volatile memory register.

In view of the state of art described, the object of the present invention is to realize an integrated circuitry for checking the utilization rate of redundancy memory elements in a semiconductor memory device, which is suitable for being used in conjunction with a redundancy circuitry in which no guard memory cells are provided to the non-volatile memory registers, and which allows a reduction in the time requested by a testing machine to carry out the resources check operation.

According to the present invention, such object is attained by means of an integrated circuitry for checking the utilization rate of redundancy memory elements in a semiconductor memory device, comprising a matrix of memory elements and a redundancy circuitry which comprises a plurality of programmable non-volatile memory registers, each of which is programmable to store an address of a defective memory element in the matrix which must be replaced by the redundancy memory element associated to the non-volatile register and is supplied with address signals to generate a redundancy selection signal for the selection of the associated redundancy memory element when said address signals coincide with the address stored therein, combinatorial circuit means supplied with said address signals and supplying the non-volatile memory registers with an inhibition signal for inhibiting the generation of the respective redundancy selection signals when said address signals coincide with the address stored in a non-programmed non-volatile memory register, characterized in that it comprises multiplexing circuit means, controlled by a control signal generated by a control circuitry of the memory device, for transmitting said redundancy selection signals to output pads of the memory device when said control signal is activated, said control signal being also supplied to said combinatorial circuit means to prevent when activated the generation of said inhibition signal.

Thanks to the present invention, it is possible for a testing machine to perform a "resources check" operation of a memory device by just supplying it with an address configuration coincident with the address stored in a non-programmed non-volatile memory register of the redundancy circuitry, and by sensing the logical state of the output pads of the memory device. The time required to carry out the "resources check" is thus greatly reduced, since it is not necessary to sequentially supply the memory device with all the possible address configurations. As already described, "resources check" is useful to assess the technological degree of defectiveness, for statistical analysis regarding the average use of redundancy memory elements, so that the number of such elements can be optimized, and to analyse the existence of local critical states.

The features of the present invention will be made more evident by the following detailed description of two particular embodiments, illustrated as non-limiting examples in the annexed drawings, wherein:

Figure 1 is an electrical schematic diagram of a part of a semiconductor memory device with an integrated circuitry according to a first embodiment of the present invention:

Figure 2 is an electrical schematic diagram of a non-volatile memory register for a redundancy circuitry of the semiconductor memory device of Figure 1:

Figure 3 is a schematic block diagram of a memory cell of the non-volatile memory register of Figure 2.

Figure 4 is an electrical schematic diagram of a part of a semiconductor memory device with an integrated circuitry according to a second embodiment of the invention.

As shown in Figure 1, a semiconductor memory device according to a first embodiment of the present invention comprises a redundancy circuitry which is integrated in a memory device chip and comprises a plurality of non-volatile memory registers 1, each associated to a respective redundancy memory element (not shown).

In practical implementations of redundancy, providing for the existence of rows ("word lines") or columns ("bit lines") or both rows and columns of redundancy memory elements, each non-volatile memory register 1 is associated to a respective redundancy row or column. This is however not of concern to the present invention, and in the following description it will be assumed that each non-volatile memory register 1 is associated to a redundancy memory element.

As also shown in Figure 1, each non-volatile memory register 1 is supplied with address signals A0-An, taken from an address signals bus ADD; the address signals bus ADD also supplies decoding circuits (not shown) for the selection of a particular memory element in the memory matrix.

As shown in Figure 2, each non-volatile memory register 1 comprises a plurality of programmable non-volatile memory cells MCO-MCn; each of said cells MCO-MCn is supplied with one of the address signals A0-An and comprises in a per-se known way, as shown in Figure 3, at least one programmable non-volatile memory element 6, a first circuit 5 for programming said memory element 6, a second circuit 7 for reading the information stored in the non-volatile memory element 6 and a third circuit 8 for comparing said information with the current logical state of the respective address signal A0-An. All the memory cells MCO-MCn of a given non-volatile memory register 1 are also supplied with a signal PGM (not shown in Figure 1) supplied by a control circuitry 4 of the memory device to enable the programming of the memory element 6; different non-volatile
memory registers 1 are supplied with different signals PGM, so that one register 1 is programmable at a time. Each memory cell MCO-MCN has an output signal CMP0-CMPn which is activated whenever the current logical state of the respective address signal A0-An coincides with the logical state stored in the non-volatile memory element 6 of the cell MCO-MCN.

Each non-volatile memory register 1 further comprises a redundancy memory element selection circuit 2 which is supplied with all the signals CMP0-CMPn and generates a signal RS used to select one redundancy memory element and to deselect a defective matrix memory element whose address coincides with the address configuration stored in the non-volatile register 1.

The redundancy circuitry also comprises a combinatorial circuit 3 supplied with the address signals A0-An and generating a signal CHKN which forms one input of a NAND gate 9; a second input of the NAND gate 9 is supplied with a signal DIS which is generated by the control circuitry 4. An output signal DIS of the NAND gate 9 is individually supplied to all the redundancy memory element selection circuits 2 of the non-volatile memory registers 1.

All the output signals RS of the non-volatile memory registers 1 are grouped together to form a redundancy selection signals bus RSBUS; this bus is normally provided in the memory device, wherein it runs from the non-volatile registers 1 to the memory matrix 10 wherein the redundancy memory elements are physically obtained.

The redundancy selection signals bus RSBUS also supplies a first input channel of a multiplexing circuit 11; a second input channel of the multiplexing circuit 11 is supplied with a read data bus RDBUS in which all the signals generated by a per-se known sensing circuitry 12 are grouped together; the sensing circuitry 12 is used to read the information stored in the addressed memory elements when the memory device is operated in reading condition. An output channel of the multiplexing circuit 11 is connected to an output data bus ODBUS which supplies a buffer circuitry 13; each signal in the ODBUS supplies a respective output buffer in the buffer circuitry 13; each output buffer drives a respective output pad 17 of the memory device. The signal CHKN also constitutes a control signal for the multiplexing circuit 11: when CHKN is activated, the output channel of the multiplexing circuit 11 is connected to the first input channel, so that the selection signal bus RSBUS is transmitted to the buffer circuitry 13; when instead CHKN is not activated, the output channel of the multiplexing circuit 11 is connected to the second input channel, so that the read data bus RDBUS is transmitted to the buffer circuitry.

At the end of the manufacturing process of the memory device, all the programmable non-volatile memory elements 6 included in the memory cells MCO-MCN of all the non-volatile memory registers 1 are in a well known and defined logical state, i.e. in the virgin or non-programmed state.

During the memory device testing, the address configurations corresponding to defective matrix memory elements are programmed into respective non-volatile memory registers 1; each time a defective matrix memory element is encountered, the testing machine puts the memory device in a condition such that the control circuitry 4 activates one signal PGM, to enable the programming of the cells MCO-MCN of a given non-volatile memory register 1; in this way any successive attempt to address said defective matrix memory element will automatically cause a redundancy memory element to be addressed. At the end of this phase, it is possible that some redundancy memory elements are left unused, and the associated non-volatile memory registers 1 are therefore left in their unprogrammed state.

When the memory is operated in normal reading condition, the control circuitry 4 keeps the signal CHKN in the high logical level; in such condition, the logical state of the signal DIS at the output of the NAND gate 9 depends on the logical state of the signal DIS, as will be explained later on; the output channel of the multiplexing circuit 11 is connected to the second input channel, i.e. the output data bus ODBUS is connected to the read data bus RDBUS, so that the data stored in the addressed matrix memory elements, read by the sensing circuitry 12, are transferred to the buffer circuitry 13 and then to respective output pads 17. If a defective matrix memory element is addressed, the non-volatile register 1 wherein its address has been programmed during testing recognizes such address and activates the signal RS, to deselect the defective matrix memory element and simultaneously to select a redundancy memory element. If the current address configuration supplied to the memory device coincides with the address stored in a non-programmed non-volatile memory register, the combinatorial circuitry 3 recognizes the event and activates the signal DIS; this in turn causes the signal DIS' to be activated, so that the activation of all the signals RS is inhibited. This prevents, if two or more non-programmed non-volatile memory registers 1 are present in the memory device, the associated redundancy memory elements from being simultaneously selected.

If it is desired to perform a *resources check* for the memory device, this must be put in the testing environment; the testing machine puts the memory device in a particular test mode in which the control circuitry 4 drives the signal CHKN to the low logical state; this causes the signal DIS' to go to the low logical state, independently on the state of the signal DIS, and also causes the output channel of the multiplexing circuit 11 to be connected to the redundancy selection signals bus RSBUS. The memory device is then supplied with an address configuration A0-An coincident with the logical state stored in non-programmed non-volatile registers 1. Even if such address configuration is recognized by the combinato-
rial circuitry 3, the activation of the signal DIS is inhibited; all the non-programmed non-volatile registers 1, associated to unused redundancy memory elements, will therefore activate the respective signal RS: the programmed non-volatile registers 1, associated to redundancy memory elements which have been utilized to replace defective matrix memory elements, will instead not activate the respective signals RS. The number of activated signals in the RSBUS will therefore correspond to the number of unused redundancy memory elements. Since the activation of the CHKN signal has caused the output channel of the multiplexing circuit 11 to be connected to the RSBUS, this will be transmitted to the buffer circuitry 13, and hence to the output pads 17. Each signal in the RSBUS is thus associated to a respective output pad 17, and it is therefore possible for the testing machine, by sensing the logical state of the output pads 17, to know which and how many unused redundancy memory elements are present in the memory device.

In the described embodiment, the number of signals in the ODBUS must be at least equal to the number of signals in the RSBUS, i.e. to the number of redundancy memory elements. It is however possible, with minor modifications, to utilize the structure according to the invention even in the case the number of redundancy memory elements is greater than the number of signals available in the ODBUS of the memory device; this can be done for example by splitting the RSBUS into two distinct buses, and using a multiplexing circuit with three input channels; for the selection of which of the input channels must be connected to the output channel (i.e. to the ODBUS), the control circuitry 4 must in this case supply the multiplexing circuit with two distinct signals, instead of the single signal CHKN. To carry out the "resources check" operation, the signals of the two redundancy selection signals buses are sequentially supplied to the buffer circuitry 13.

In Figure 4 a second embodiment of the invention is shown, suitable for a memory device in which the memory matrix is divided in sectors individually addressable; such architecture is used for example in Flash EEPROM devices. Each sector is provided with redundancy memory elements; to increase the reparationability rate, and thus the process yield, defective matrix memory elements in a given sector can be made redundant without causing non-defective matrix memory elements of other sectors having identical addresses to be simultaneously made redundant. This is obtained by providing each sector with a respective set 14 of non-volatile memory registers, and by submitting the selection of a redundancy memory element to a sector address decoding.

As shown in Figure 4, each set 14 comprises an equal number of non-volatile memory registers 1, supplied with address signals A0-An which also supplies a decoding circuitry (not shown) for the selection of a particular matrix memory element in each sector. All the output signals RS of the non-volatile registers 1 of a given set are grouped together to form a local redundancy selection signals bus RSBUS', which is supplied to an input channel of a multiple switch 16; the output channel of the multiple switch 16 is connected to the redundancy selection signals bus RSBUS, already encountered in the description of the previous embodiment. Each multiple switch 16 is controlled by a signal SS supplied by a sector address decoding and selection circuit 15 which is supplied by sector address signals An+1-Ak taken from the address signals bus ADD.

During a "resources check", the control circuitry 4 drives the signal CHKN to the low logical state, and the activation of the signal DIS is therefore prevented; the multiplexing circuit 11 connects the RSBUS to the ODBUS, and thus to the buffer circuitry 13.

The memory device is then supplied with an address configuration wherein the address signals A0-An are in a logical state coincident with the logical state stored in non-programmed non-volatile registers 1; all the non-programmed non-volatile registers 1 in all the sets 14 will therefore activate their output signals RS; the sector address signals An+1-Ak are sequentially changed to address one different sector at a time, so that only one RSBUS' is connected, via the respective multiple switch 16, to the RSBUS. By sensing the logical state of the output pads 17, it is thus possible to know which and how many redundancy memory elements in each sector have not been utilized to replace defective matrix memory elements.

Claims

1. Integrated circuitry for checking the utilization rate of redundancy memory elements in a semiconductor memory device, comprising a matrix of memory elements and redundancy circuitry which comprises a plurality of programmable non-volatile memory registers (1), each of which is programmable to store an address of a defective memory element in the matrix which must be replaced by the redundancy memory element associated to the non-volatile register (1) and is supplied with address signals (A0-An) to generate a redundancy selection signal (RS) for the selection of the associated redundancy memory element when said address signals (A0-An) coincide with the address stored therein, combinatorial circuit means (3,9) supplied with said address signals (A0-An) and supplying the non-volatile memory registers (1) with an inhibition signal (DIS) for inhibiting the generation of the respective redundancy selection signals (RS) when said address signals (A0-An) coincide with the address stored in a non-programmed non-volatile memory register (1), characterized in that it comprises multiplexing circuit means (11), controlled by a control signal (CHKN) generated by a control circuitry (4).
of the memory device, for transmitting said redundancy selection signals (RS) to output pads (17) of the memory device when said control signal (CHKN) is activated, said control signal (CHKN) being also supplied to said combinational circuit means (3,9) to prevent when activated the generation of said inhibition signal (DIS').

2. Integrated circuitry according to claim 1, characterized in that when said control signal (CHKN) is deactivated said multiplexing circuit means (11) transmit to said output pads (17) signals (RDBUS) generated by a sensing circuitry (12) for reading the memory elements in the matrix.

3. Integrated circuitry according to claim 1, said matrix of memory elements being divided in respective non-volatile memory elements associated to respective non-volatile memory registers (1) in the redundancy circuitry, characterized in that said integrated circuitry comprises select sector circuit means (15) supplied with sector address signals (An+1-Ak) and generating sector selection signals (SS) controlling switching means (16) supplied with said redundancy selection signals (RS) and supplying said multiplexing circuit means (11) with a set of said selection signals (RS) which are generated by the non-volatile memory registers (1) associated to redundancy memory elements of the sector currently addressed.

4. Integrated circuitry according to claim 1 or 2, characterized in that each programmable non-volatile memory register (1) comprises a number of programmable memory cells (MC0-MCn) equal to the number of said address signals (A0-An), each memory cell (MC0-MCn) being supplied with one address signal and generating an output signal (CMP0-CMPn) when the logical state of said address signal correspond to the logical state stored in the memory cell (MC0-MCn), each non-volatile memory register (1) further comprising selection circuit means (2) supplied with the output signals (CMP0-CMPn) of the memory cells (MC0-MCn) for generating said redundancy selection signal (RS), said selection circuit means (2) being also supplied with said inhibition signal (DIS') which prevent when activated the generation of said redundancy selection signal (RS).

Patentansprüche

1. Integrierte Schaltung zur Überwachung der Benutzungsraten von Redundanzspeichereinrichtungen in einer Halbleiterspeichereinrichtung, mit einer Matrix von Speicherelementen und einer Redundanzschaltung, die aufweist eine Mehrzahl von programmierbaren nichtflüchtigen Speicherregistern (1), von denen jeder programmierbar ist zum Speichern einer Adresse eines defekten Speicherelementes in der Matrix, das durch das mit dem nichtflüchtigen Register (1) verknüpfte Redundanzspeicherelement ersetzt werden muß, und mit Adreßsignalen (A0 - An) beliefert wird zum Erzeugen eines Redundanzauswahlsignales (RS) zum Auswählen des zugehörigen Redundanzspeicherelementes, wenn die Adreßsignale (A0 - An) mit der darin gespeicherten Adresse übereinstimmen, ein Kombinationsschaltmittel (3, 9), das mit den Adreßsignalen (A0 - An) beliefert wird und die nichtflüchtigen Speicherregister (1) mit einem Verhinderungssignal (DIS') beliefert zum Verhindern der Erzeugung der entsprechenden Redundanzauswahlsignale (RS), wenn die Adreßsignale (A0 - An) mit der in einem nichtprogrammierten nichtflüchtigen Speicherregister (1) gespeicherten Adresse übereinstimmen, dadurch gekennzeichnet, daß sie ein Multiplexschaltmittel (11) aufweist,

das durch ein von einer Steuerschaltung (4) der Speichereinrichtung erzeugtes Steuersignal (CHKN) gesteuert wird, zum Übertragen der Redundanzauswahlsignale (RS) zu Ausgangsanschlußflcken (17) der Speichereinrichtung, wenn das Steuersignal aktiviert ist, wobei das Steuersignal (CHKN) auch zu dem Kombinationsschaltmittel (3, 9) zum Verhindern, wenn es aktiviert ist, der Erzeugung des Verhinderungssignales (DIS') geliefert wird.

2. Integrierte Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß, wenn das Steuersignal (CHKN) desaktiviert ist, das Multiplexschaltmittel (11) zu den Ausgangsanschlußflcken (17) Signale (RDBUS) überträgt, die von einer Erfassungsschaltung (12) zum Lesen der Speicherelemente in der Matrix erzeugt sind.

3. Integrierte Schaltung nach Anspruch 1, bei der die Matrix von Speicherelementen in individuell adressierbare Matrixsektoren unterteilt ist, je der Sektor mit entsprechenden Redundanzspeicherelementen versehen ist, die mit entsprechenden nichtflüchtigen Speicherregistern (1) in der Redundanzschaltung verknüpft sind, dadurch gekennzeichnet, daß die integrierte Schaltung ein Sektorauswahlschaltmittel (15) aufweist, das mit Sektoradresseignalen (An+1-Ak) beliefert
wird und Auswahlsignale (SS) erzeugt, die ein Schaltmittel (16) steuern, das mit allen der Redundanzauswahlsignale (RS) belieft wird und das Multiplexschaltmittel (11) mit einem Satz der Aus-

wahlssignale (RS) beliefert, die von den nichtflüchtigen Speicherregistern (1) erzeugt sind, die mit Redundanzspeicherelementen des geganwärzig adressierten Sektors verknüpft sind.

4. Integrierte Schaltung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes programmierbare nichtflüchtige Speicherregister (1) eine Zahl von programmierbaren Speicherzellen (MC0 - MCn) gleich der Zahl der Adreßsignale (AO - An) aufweist, wobei jede Speicherzelle (MC0 - MCn) mit einem Adreßsignal beliefert wird und ein Ausgangs-

ignal (CMP0 - CMPn) erzeugt, wenn der logische Zustand des Adreßsignalen dem in der Speicher-

zelle (MC0 - MCn) gespeicherten logischen Zu-

stand entspricht, jedes nichtflüchtige Speicherregi-

ster (1) weiter ein Auswahlschaltmittel (2) aufweist, das mit den Ausgangssignalen (CMP0 - CMPn) der Speicherzelle (MC0 - MCn) zum Erzeugen des Redundanzauswahlsignales (RS) beliefert wird, das Auswahlschaltmittel (2) ebenfalls mit dem Ver-

hindergungssignal (DIS) beliefert wird, das, wenn es aktiviert ist, die Erzeugung des Redundanzaus-

wahlsignales (RS) verhindert.

Revendications

1. Circuit intégré destiné à la vérification du taux d’utilisation d’éléments de mémoire à redondance dans un dispositif de mémoire à semi-conducteur, comprenant une matrice d’éléments de mémoire et un circuit de redondance qui comprend plusieurs re-

gistres programmables (1) de mémoire permanente, chacun étant programmable afin qu’il conserve une adresse d’un élément défectueux de mémoire de la matrice qui doit être remplacé par l’élément de mémoire de redondance associé au registre per-

manent (1) et recevant des signaux d’adresse (A0-An) pour la création d’un signal de sélection de redondance (RS) destiné à la sélection d’un élé-

ment associé de mémoire de redondance lorsque les signaux d’adresse (A0-An) coïncident avec l’adresse mémorisée, et un dispositif (3, 9) à circuit combinatoire recevant les signaux d’adresse (A0-An) et transmettant aux registres (1) de mémoi-

re permanente un signal d’inhibition (DIS) destiné à inhiber la création des signaux respectifs de sé-

lection de redondance (RS) lorsque les signaux d’adresse (A0-An) coïncident avec l’adresse mé-

morisée dans un registre non programmé (1) de mémoire permanente, caractérisé en ce qu’il com-

prend un dispositif (11) à circuit de multiplexage, commandé par un signal de commande (CHKN) créé par un circuit de commande (4) du dispositif de mémoire afin qu’il transmette les signaux (RS) de sélection de redondance à des plages (17) de sortie du dispositif de mémoire lorsque le signal de commande (CHKN) est activé, le signal de com-

mande (CHKN) étant aussi transmis au dispositif (3, 9) à circuit combinatoire afin que, lorsqu’il est acti-

vé, il empêche la création du signal d’inhibition (DIS*).

2. Circuit intégré selon la revendication 1, caractérisé en ce que, lorsque le signal de commande (CHKN) est désactivé, le dispositif (11) à circuit de multi-

plexage transmet aux plages de sortie (17) des si-

gnaux (RDBUS) créés par un circuit de détection (12) pour la lecture des éléments de mémoire dans la matrice.

3. Circuit intégré selon la revendication 1, la matrice d’éléments de mémoire étant divisée en secteurs de matrice adressables individuellement, chaque secteur ayant des éléments respectifs de mémoire de redondance associés à des registres respectifs (1) de mémoire permanente dans le circuit de re-

dondance, caractérisé en ce que le circuit intégré comprend un dispositif (15) à circuit de sélection de secteur recevant les signaux d’adresse de secteur (An+1-Ak) et créant des signaux de sélection de secteur (SS) commandant un dispositif de commu-

nation (16) qui reçoit tous les signaux de sélection de redondance (RS) et transmet au dispositif (11) à circuit de multiplexage un ensemble de signaux de sélection (RS) qui sont créés par les registres (1) de mémoire permanente associés aux éléments de mémoire de redondance du secteur actuellement adressé.

4. Circuit intégré selon la revendication 1 ou 2, carac-

tériisé en ce que chaque registre programmable (1) de mémoire permanente comprend un certain nom-

bre de cellules (MC0-MCn) de mémoire programmable égal au nombre des signaux d’adresse (A0-An), chaque cellule de mémoire (MC0-MCn) re-

cevant un signal d’adresse et créant un signal de sortie (CMP0-CMPn) lorsque l’état logique du si-

gnal d’adresse correspond à l’état logique conservé dans la cellule de mémoire (MC0-MCn), chaque re-

gistre (1) de mémoire permanente comprenant en outre un dispositif (2) à circuit de sélection qui reçoit les signaux de sortie (CMP0-CMPn) des cellules de mémoire (MC0-MCn) pour la création du signal de sélection de redondance (RS), le dispositif (2) à cir-

cuit de sélection recevant aussi le signal d’inhibition (DIS) qui, lorsqu’il est activé, empêche la création du signal de sélection de redondance (RS).
Fig. 4