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(54) Transceiver circuit for an integrated circuit
Übertragungsempfängerschaltkreis für eine integrierte Schaltung
Circuit pour la réception de transmission pour un circuit intégré

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Description

This invention relates to transceiver circuits suitable for use on integrated circuits.

As conventional integrated circuits become denser, i.e. more active devices per square centimetre, and faster, the required heat dissipation per square centimetre becomes greater and greater. This would be less of a problem if it meant that integrated circuits would be spaced further apart in order to dissipate this heat, but the direction of current integrated circuit technology is to space the integrated circuit chips closer and closer together. By spacing the integrated circuit chips as closely as possible, capacitive and inductive loading of output lead lines and the problems of driving output lead lines are reduced. Previous designs accepted the high heat densities of conventional integrated circuit logic connected in multi-chip modules and expended large amounts of energy and special purpose equipment, such as large heat sinks and liquid or cryogenic cooling, to cool the multi-chip modules. Expending substantial amounts of money on cooling multi-chip modules could be eliminated and energy saved if the logic on the multi-chip modules simply dissipated less heat to start with.

JP-A-0.2246624 discloses an output buffer circuit in which the output impedance can be adjusted in an attempt to achieve a more constant value for both high and low output signals. However, the manner in which the output impedance of the buffer circuit of this document can be adjusted is disadvantageously limited.

It is an object of the present invention to provide a digital integrated circuit that has a low power consumption.

Therefore, according to the present invention, there is provided a transceiver circuit for an integrated circuit having a pad located therein, a receiving circuit connected to the pad for receiving digital data signals therefrom, a transmitting circuit connected to the pad for transmitting digital data signals to the pad, characterized by output resistance control means connected to said transmitting circuit and arranged to dynamically retain said output resistance of the transmitting circuit at a constant value during data signal transmission from said transmitting circuit.

It will be appreciated that a transceiver circuit according to the invention has the advantage of low power consumption and consequently low heat generation, since the output resistance control arrangement enables the elimination of termination resistors to terminate integrated circuit I/O (input-output) lines. Furthermore, this advantage is achieved without compromising data handling speed.

One embodiment of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a partially broken away block diagram of an integrated circuit and an I/O transceiver circuit thereof according to the present invention; Fig. 2 is a schematic of the transmitter, the receiver, and the reference voltage supply portions of Fig. 1, according to one embodiment of the invention; Fig. 3 is a block diagram of a phase locked loop that is used as the output resistance controller portion of Fig. 1, according to one embodiment of the invention; Fig. 4 is a logic diagram of the phase detector portion of the phase locked loop of Fig. 3; Fig. 5 is a schematic diagram of the charge pump portion and a low pass filter portion of the phase locked loop of Fig. 3; Fig. 6 is a block diagram of the voltage controlled oscillator portion of the phase locked loop of Fig. 3; Fig. 7 is a schematic diagram of one stage of a multiple stage voltage controlled oscillator according to the invention; and Fig. 8 is a schematic diagram of the voltage controller portion of the phase locked loop of Fig. 3.

Referring now to Fig. 1, a portion of an integrated circuit 10 is shown. Integrated circuit 10 has a number of substantially similar input/output (I/O) transceiver circuits of which a representative I/O transceiver circuit 12 is shown. For the sake of simplicity and brevity, only I/O transceiver circuit 12 will be described.

I/O transceiver circuit 12 is designed for use with high speed, low power integrated circuits such as are used in multi-chip modules. I/O transceiver circuit 12 is especially designed to transmit and receive digital data with a reduced voltage difference between a logic HIGH and a logic LOW than standard CMOS and TTL digital integrated circuits, yet maintain an acceptable noise margin of at least 400 millivolts. I/O circuit 12 is typically connected by a non-terminated bi-directional bus line 14 to a similar I/O circuit (not shown). Those skilled in the digital integrated circuit art will recognize that reduced voltage difference between logic levels and the non-terminated line provide for a reduced amount of power delivered by the I/O transceiver 12, a reduced amount of power dissipated by the I/O transceiver 12 and a higher data transfer speed. These attributes are all very desirable for multi-chip modules assemblies and sub-assemblies, although these attributes are also useful for other applications than multi-chip module assemblies.

The bi-directional line 14 connects to I/O transceiver 12 at an I/O pad 16 located on the integrated circuit 10 (through an integrated circuit lead that is not shown for simplicity). Within the I/O transceiver 12, I/O pad 16 connects to a transmitter 20 by line 18 and to a receiver 24 by line 22. Transmitter 20 receives data for transmission on data line 26 from internal logic (not shown) of the integrated circuit 10. Receiver 24 receives data signals from pad 16 through line 22, processes these data signals into data signals outputted on data output line 28 to internal logic (not shown) of the integrated circuit 10. The data mode of I/O transceiver 12 is determined
by an ENABLE signal inputted to transmitter 20 on line 30.

I/O transceiver 12 operates on binary levels that are separated by a reduced voltage separation. Because of this reduced separation, it is desirable to reduce variations in the receiving threshold voltage and the transmitting output resistance of the transceiver 12. Receiver 24 is connected to a reference voltage circuit 32 by line 34. Reference voltage circuit 32 accurately sets the threshold voltage of receiver 24 and of any other similar receiver (not shown) of the integrated circuit 10. Transmitter 20 is connected to an output resistance controller circuit 40 by line 42. Output resistance controller circuit 40 controls the output resistance of the transmitter 20 to a constant value of resistance. A transmitter with a small constant value of output impedance has been determined by simulations to be the best way from a noise aspect to drive the non-terminated bus line 14.

The use of reference voltage circuit 32 to control the input threshold switching level and output resistance controller circuit 40 to control the output driving resistance enables the use binary logic levels separated by only 1.0 volts with a noise margin of 0.4 volts.

Referring now to Fig. 2, a specific embodiment of the invention shown in Fig. 1 will be described. The receiver 24 and reference voltage circuit 32 will first be briefly described. The receiver 24 includes a first series summing amplifier having a first input which is connected to the input pad 16 and a second input which is connected to the output line 34 of a control voltage generating means 32. The reference voltage circuit 32, which sets a highly stable, accurate threshold voltage for the receiver 24, includes a second series summing amplifier having a first input connected to a voltage divider R1, R2 which supplies a reference voltage, and a second input connected to the line 34. The second series summing amplifier includes series-connected FETs having transconductances matched to corresponding FETs in the first series summing amplifier.

Transmitter 20 has an input for data signals to be transmitted connected to line 26. Data signals on line 26 are connected commonly to the gates of NFET 50 and PFET 52. NFET 50 has its source connected to circuit ground and its drain connected to the drain of PFET 52. The source of PFET 52 is connected to the output of output resistance control circuit 40 via line 42. FETs 50, 52 form a CMOS inverter, which inverts and amplifies the inputted data signals and conveys the inverted and amplified data signals by line 53 to the gates of NFET 55 and PFET 56. PFET 55 has its source connected to circuit ground and its drain connected to the drain of PFET 56. The source of PFET 56 is connected to the output of output resistance control circuit 40 via line 42. FETs 55, 56 form a second CMOS inverter which inverts and amplifies the inputted data signals a second time and conveys the twice amplified and inverted data signals along line 57 to one input of an output driver 60.

The inverted and amplified data signals from FETs 50, 52 are also conveyed by line 53 to a second input of output driver 60. Thus, output driver 60 has a first input that is the data signal once inverted and a second input that is the same data signal once inverted. This means the data on the two inputs will always be inverted relative to each other.

Output driver 60 has a gate of NFET 62 and a gate of PFET 78, which together form the first input, connected to line 57. The drain of NFET 62 is connected to the pad 16 by line 18. The source of PFET 78 is connected through an enabling PFET 82 to the output resistance controller voltage on line 42. The source of NFET 62 and the drain of PFET 78 are connected to a gate of NFET 64. The drain of NFET 64, like the drain of NFET 62 is connected to pad 16. The source of NFET 64 is connected to VOL, which in the preferred embodiment is 1.0 volts. When the logic level on data input line 26 is a logic low, line 57 is also a logic low, PFET 78 is turned on and NFET 62 is turned off. For such a situation, the output resistance control voltage will be switched onto the gate of NFET 64, causing NFET 64 to conduct and pull the voltage of pad 16 to substantially VOL.

Output driver 60 also has a gate of NFET 66 and a gate of PFET 80, which together form the second input, connected to line 53. The drain of NFET 66 is connected to VOH, which in the preferred embodiment is 2.0 volts. The source of PFET 80 is connected through enabling PFET 84 to the output resistance controller voltage on line 42. The source of NFET 66 and the drain of PFET 80 are connected to the gate of NFET 68. The drain of NFET 68, like the drain of NFET 66, is connected to VOH. The source of NFET 68 is connected to pad 16 by line 18. When the data signal on line 26 is a logic high, the inverted signal on line 53 will be a logic low, NFET 66 will be turned off and PFET 67 will be turned on. For that condition, the output resistance control voltage will be switched onto the gate of NFET 68 and NFET 68 will conduct, pulling up the voltage level of pad 16 to substantially VOH.

For a logic high level data signal on line 26, (shown in Fig. 1) transmitter 20 outputs substantially VOH to pad 16. For a logic low level on line 26, transmitter 20 outputs substantially VOL to pad 16. With such characteristics, transmitter 20 is called a non-inverting transmitter.

The previous discussion assumed that the transmitter 20 is enabled, i.e., the logic level on line 30 was a logic high. Line 30 conducts the enable signal to commonly connected gates of NFET 70 and PFET 72. NFET 70 has its source connected to circuit ground and its drain connected to the drain of PFET 72. The source of PFET 72 is connected to the output of output resistance control circuit 40 via line 42. FETs 70, 72 form a CMOS inverter, which inverts and amplifies the logic high input enable signal and conveys the amplified and inverted signal, at this point a logic low, by line 58 to PFET 82 and also by line 59 to PFET 84 and NFETs 67, 63. PFETs 82 and 84 are turned off by the logic high on line 58. PFETs 82 and 84 are placed in a conducting state by
the logic low on line 58, and such conduction supplies NFETs 63, 67 with the high voltage level that is outputted from output resistance controller 40 on line 42.

When the transmitter 20 is disabled, i.e. when the logic level on line 30 is a logic low, FETs 70, 72 invert the logic low to a logic high on line 58. A logic high on the gates of PFETs 82, 84 will turn them off and remove the positive voltage supply from NFETs 63, 67. Further, the logic high on the gates of NFETs 63, 67 will turn them on, thereby shorting the drains of output NFETs 64, 68 to their respective gates and causing these output NFETs 64, 68 to act as diodes.

Referring now to Fig. 3, the output resistance controller 40 will be described. The output resistance controller 40 includes a phase locked loop which is connected to an off-chip reference clock (not shown) as an accurate, stable source of digital pulse signals. The off-chip reference clock is received on an input of a buffer 100, to shape the input digital pulses and remove as much noise as possible therefrom. The buffer 100 has an output which is connected to a first input of a phase detector 102. Phase detector 102 has a second input which comes from a local VCO via a divide by N circuit, as will be explained below.

Referring now to Fig. 4, a preferred embodiment of the phase detector 102 is shown. The circuit of Fig. 4 uses all NAND gates with two inverters, one on each of the outputs. This preferred embodiment is for a CMOS implementation. Those of average skill in the art will recognize that other types of phase detector could also be used for CMOS or other logic family implementations. This embodiment is preferred because it detects frequency as well as phase, and thus prevents harmonic locking as phase locked loops are known to be prone to.

Phase detector 102 has two outputs as well as two inputs. The first output 103 is true if the local VCO frequency must go up to match the reference clock input in frequency. The second output 104 is true if the local VCO frequency must go down to match the reference input frequency.

Referring back to Fig. 3, the phase detector outputs 103 and 104 are connected to up and down inputs of a charge pump 106. The output signals on outputs 103 and 104 represent phase error signals, as is well known in the art of phase locked loops. The charge pump 106 is a type of amplifier that pumps electric charge into or out of a low pass filter 108 attached to its output as a function of the error signals on outputs 103 and 104. Referring briefly to Fig. 5, a preferred embodiment of the charge pump 106 and the low pass filter 108 are shown. The charge pump 106 receives the digital error signals from phase detector outputs 103, 104, processes and amplifies these error signals and outputs an error current to low pass filter 108. The low pass filter 108 averages the error current and integrates it into a relatively long term averaged control voltage at an output terminal 109 connected to an output capacitor Co.

Referring now to Figs. 3 and 8, the output 109 of the low pass filter 108 is connected to an input 111 of a control voltage circuit 110. Control voltage stage 110 has a differential amplifier stage formed by FETs 112, 113. The input 111 is connected to the gate of FET 112. FET 113 has its gate connected to the output of the control voltage circuit 110 through a feedback compensation network formed by the parallel combination of Rcomp and Ccomp. FETs 112 and 113 are a high speed type to increase the gain bandwidth product of the circuit 110 in order to allow high speed tracking of the error signal from the low pass filter 108. The output signal of the differential amplifier is taken from the drain of FET 112 and connected to the gate of output FET 114, which is connected in a common source configuration with its output load resistance being provided by FET 116. The control voltage circuit 110 takes the error voltage from low pass filter 108, which is a low power and high impedance circuit, and outputs the amplified error signal at a higher power level and at a lower impedance level. This is important because this amplified error signal is the output resistance control voltage that is supplied to the driver 20 via line 42. This amplified error signal is connected to VCO 120 (shown in Figs. 3 and 6).

Referring now to Figs. 3 and 6, the VCO 120 will be described. As shown in Fig. 6, VCO 120 is made up of three identical special inverter stages 120A, 120A' and 120A'' connected in series. Each of these stages has a respective input 126, 126' and 126'', and a respective output 170, 170' and 170''. The output 170 is connected to the input 126. The output 170' is connected to the input 126'. The output 170'' is connected back to the input 126, thereby forming a ring oscillator. Those skilled in the art will recognize that similar ring oscillators can be formed with any odd number of stages greater than three.

Referring now to Fig. 7, each of the special inverter stages 120A, 120A' and 120A'' will be described. Each of the special inverter stages 120A, 120A' and 120A'' has FETs 121, 122, 123, and 124 that are connected in series as a four FET inverter stage. FETs 121 and 124 have their gates connected to each other and also to the threshold control voltage on line 34 (shown in Fig. 2). FETs 122 and 123 have their gates connected to each other and to line 126 which supplies negative feedback, as will be explained. Connected in this manner, PFET 122 and NFET 123 operate as a CMOS inverter whose threshold logic level is set by the threshold control voltage on line 34. The output of this inverter is taken from a junction 125 of the drain of PFET 122 with the drain of the NFET 123. The junction 125 is connected by line 127 to the gates of PFET 152 and NFET 150 which are connected in series in a CMOS inverter configuration, which will be explained in detail below.

PFET 152 has its source connected to line 42, which has the control voltage from voltage control 110 (see Figs. 3 and 7) thereon. The drain of PFET 152 is connected to the drain of NFET 150. The source of NFET 150 is connected to circuit ground. The inverter
formed by FETs 150, 152 inverts and amplifies any signal input on line 127. This inverted and amplified signal is conveyed by line 153 to the gates of NFET 155 and PFET 156. NFET 155 has its source connected to circuit ground and its drain connected to the drain of PFET 156. The source of PFET 156 is connected to the control voltage outputted by the voltage controller 110 via line 42. FETs 155, 156 form another CMOS inverter which inverts and amplifies the inputted signal further and conveys the thrice amplified and inverted data signals along line 157 to one input of a power driver 160.

The inverted and amplified signal from FETs 150, 152 are also conveyed by lines 153, 158 to a second input of power driver 160. Thus, power driver 160 has a first input that is the signal inputted on line 157 twice inverted and a second input on line 158 that is the same data signal once inverted. This means the data on these two inputs will always be inverted relative to each other.

Power driver 160 has a gate of NFET 162 and a gate of PFET 163, which together form the first input, connected to line 157. The drain of NFET 162 is connected to an output line 170. The source of PFET 163 is connected to the voltage controller 110 on line 42. The source of NFET 162 and the drain of PFET 163 are connected to a gate of NFET 164. The drain of NFET 164, like the drain of NFET 162 is connected to output line 170. The source of NFET 164 is connected to VOL, which in the preferred embodiment is 1.0 volts. Including the CMOS inverter formed by FETs 121-124, when the logic level on input line 126 is a logic high, line 157 is a logic low, PFET 163 is turned on and NFET 62 is turned off. For such a situation, the control voltage from the voltage controller 110 will be switched onto the gate of NFET 164, causing NFET 164 to conduct and pull the voltage of output line 170 towards VOL.

Power driver 160 also has a gate of NFET 166 and a gate of PFET 167, which together form the second input, connected to line 158. The drain of NFET 166 is connected to VOH, which in the preferred embodiment is 2.0 volts. The source of PFET 167 is connected to the control voltage from the voltage controller 110 on line 42. The source of NFET 166 and the drain of PFET 167 are connected to the gate of NFET 168. The drain of NFET 168, like the drain of NFET 166, is connected to VOH. The source of NFET 168 is connected to output line 170. Including the CMOS inverter formed by FETs 121-124, when the signal on line 126 is a logic low, the twice inverted signal on line 158 will be a logic low. NFET 166 will be turned off and PFET 167 will be turned on. For that situation, the control voltage from the voltage controller 110 will be switched onto the gate of NFET 168 causing NFET 168 to conduct and pull up the voltage level of output line 170 towards VOH.

As mentioned previously with respect to Fig. 6, the output 170° of special inverter stage 120A is feedback to input 126 of special inverter stage 120A to form the VCO 120, which is a ring oscillator. The frequency of oscillation of this ring oscillator is determined by the propagation and delay characteristics of the individual stages of the ring. In addition to the characteristic delay associated with power driver 160, each stage also has a capacitor, C_{freq}, connected from its output to circuit ground. Connected in this manner, the characteristic series resistance of each power driver, which is essentially the series resistance of output NFETs 164 and 168, forms an RC timing network with its respective capacitor C_{freq}. By taking a nominal series output resistance for each stage and preselecting a capacitance of C_{freq} for each stage to provide a frequency of oscillation that is nominally the same as the frequency of the off-chip reference clock, the free running frequency of the VCO 120 is determined. If the off-chip clock at a frequency that is lower than the natural frequency of the VCO 120, the VCO frequency may be run at N times the off-chip reference clock value and divided by N as shown in Fig. 3.

In operation, since C_{freq} has a constant value and the off-chip clock has a constant frequency, the phase locked loop 40 (shown in Fig. 3) will control the power driver series resistance to be a constant value by means of the control voltage on line 42. Further, since the configuration of the power driver 160 is selected to be the substantially the same as the configuration of the output driver 60, by connecting the same control voltage on line 42 to equivalent connections of output driver 60, i.e. the drains of FETs 56, 63, and 67 (shown in Fig. 3), the output resistance of output driver 60, as well as any other output driver that is similarly connected, will be controlled to a constant value also.

Thus, it will now be understood that there has been disclosed a new and novel input/output circuit for multi-chip module applications which includes direct connection to unterminated output bus lines. Also, both the receiver and the transmitter are controlled to have sufficient noise margins in order to operate at reduced logic voltage levels to reduce power dissipation. While the invention has been particularly illustrated and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form, details, and applications may be made therein within the scope of the invention as defined in the appended claims. For example, the VOH and VOL could be varied from the preferred values of 2.0 volt and 1.0 volt and still reduce power dissipation.

**Claims**

1. A transceiver circuit for an integrated circuit having a pad (16) located therein, a receiving circuit (24) connected to the pad (16) for receiving digital data signals therefrom, a transmitting circuit (20) connected to the pad (16) for transmitting digital data signals to the pad (16), characterized by output resistance control means (40) connected to said transmitting circuit (20) and arranged to dynamically retain said output resistance of the transmitting
circuit (20) at a constant value during data signal transmission from said transmitting circuit (20).

2. A transceiver circuit according to Claim 1, characterized in that said output resistance control means (40) includes a phase locked loop.

3. A transceiver circuit according to Claim 2, characterized in that said phase locked loop includes a voltage controlled oscillator (120), in that said transmitting circuit (20) has an output stage (60) and the resistance of said transmitting circuit (20) is substantially the same as the resistance of said output stage; in that said voltage controlled oscillator (120) has an output stage (160) that is substantially the same as said transmitting circuit output stage and has an output resistance that is substantially the same as said transmitting circuit resistance; in that said voltage controlled oscillator output stage resistance controls a frequency of operation of said phase locked loop and said phase locked loop tends to maintain a predetermined frequency by an error signal that is fed back to said voltage controlled oscillator (120) to maintain the resistance thereof at a constant value; and in that said error signal is also connected to said transmitting circuit output stage (60) to maintain the resistance thereof at a similar constant value.

4. A transceiver circuit according to Claim 3, characterized in that said voltage controlled oscillator includes a plurality of series-connected inverter stages (120A, 120A', 120A") connected in a feedback loop.

3. Sende-Empfang-Einrichtung nach Anspruch 2, dadurch gekennzeichnet, daß der genannte Phasenregelkreis einen spannungsgeregelter Ozillator (120) beinhaltet, dadurch, daß die genannte Senderschaltung (20) eine Ausgangsstufe (60) hat und der Widerstand der genannten Senderschaltung (20) im wesentlichen der Widerstand der genannten Ausgangsstufe ist; dadurch, daß der genannte spannungsgeregelter Ozillator (120) eine Ausgangsstufe (160) hat, die im wesentlichen dieselbe ist wie die genannte Ausgangsstufe der Senderschaltung, und einen Ausgangswiderstand, der im wesentlichen dieselbe ist wie der Widerstand der genannten Senderschaltung; dadurch, daß der Ausgangsstufenwiderstand des genannten spannungsgeregelter Ozillators eine Betriebsfrequenz des genannten Phasenregelkreises steuert und der genannte Phasenregelkreis dazu neigt, eine vorbestimmte Frequenz durch ein Fehlersignal zu halten, das zurück zu dem genannten spannungsgeregelter Ozillator (120) gespeist wird, um dessen Widerstand auf einem konstanten Wert zu halten; und dadurch, daß das genannte Fehlersignal auch auf die genannte Senderschaltungs-Ausgangsstufe (60) angeschlossen ist, um deren Widerstand auf einem ähnlichen konstanten Wert zu halten.

4. Sende-Empfang-Einrichtung nach Anspruch 3, dadurch gekennzeichnet, daß der genannte spannungsgeregelter Ozillator eine Mehrzahl von in Reihe geschalteten Inverterstufen (120A, 120A', 120A") beinhaltet, die in einem Rückführkreis miteinander verbunden sind.

Patentansprüche

1. Sende-Empfangs-Einrichtung für eine integrierte Schaltung mit einer darin befindlichen Kontaktstelle (16), einer mit der Kontaktstelle (16) verbundenen Empfängerschaltung (24) zum Empfangen von digitalen Datensignalen von dieser, einer mit der Kontaktstelle (16) verbundenen Senderschaltung (20) zum Senden von digitalen Datensignalen zu der Kontaktstelle (16), gekennzeichnet durch ein Ausgangswiderstand-Regelungsmittel (40), das an die genannte Senderschaltung (20) angeschlossen ist und die Aufgabe hat, den genannten Ausgangswiderstand der Senderschaltung (20) während der Datensignalversendung von der genannten Senderschaltung (20) auf einem konstanten Wert dynamisch zu halten.

2. Sende-Empfangs-Einrichtung nach Anspruch 1, dadurch gekennzeichnet, daß das genannte Ausgangswiderstand-Regelungsmittel (40) einen Phasenregelkreis beinhaltet.

Revisions

1. Circuit émetteur-récepteur pour un circuit intégré sur lequel est disposé un contact (16), ayant un circuit récepteur (24) connecté au contact (16) pour recevoir des signaux de données numériques provenant de celui-ci, un circuit émetteur (20) connecté au contact (16) pour transmettre des signaux de données numériques au contact (16), caractérisé par des moyens de commande de résistance de sortie (40) connectés audit circuit émetteur (20) et disposés de manière à maintenir de manière dynamique ladite résistance de sortie du circuit émetteur (20) à une valeur constante pendant la transmission de signal de données par ledit circuit émetteur (20).

2. Circuit émetteur-récepteur selon la revendication 1, caractérisé en ce que lesdits moyens de commande de la résistance de sortie (40) comprennent une boucle à verrouillage de phase.

3. Circuit émetteur-récepteur selon la revendication 2, caractérisé en ce que ladite boucle à verrouillage
de phase comprend un oscillateur commandé en tension (120), en ce que ledit circuit émetteur (20) a un étage de sortie (60) et la résistance dudit circuit émetteur (20) est sensiblement la résistance dudit étage de sortie ; en ce que ledit oscillateur commandé en tension (120) a un étage de sortie (160) qui est sensiblement le même que ledit étage de sortie du circuit émetteur et a une résistance de sortie qui est sensiblement la même que ladite résistance du circuit émetteur ; en ce que ladite résistance de l'étage de sortie de l'oscillateur commandé en tension commande une fréquence de fonctionnement de ladite boucle à verrouillage de phase et ladite boucle à verrouillage de phase tend à maintenir une fréquence prédéterminée par un signal d'erreur qui est renvoyé audit oscillateur commandé en tension (120) pour maintenir la résistance de celui-ci à une valeur constante ; et en ce que ledit signal d'erreur est également connecté audit étage de sortie du circuit émetteur (80) pour maintenir la résistance de celui-ci à une valeur constante similaire.

4. Circuit émetteur-récepteur selon la revendication 3, caractérisé en ce que ledit oscillateur commandé en tension comprend une pluralité d'étages inverseurs connectés en série (120A, 120A', 120A") connectés dans une boucle de rétro-action.
FIG. 1

OUTPUT RESISTANCE CONTROLLER

TO OTHER I/O TRANSMITTERS

DATA IN
ENABLE
DATA OUT

RECEIVER

PAD

BIDIRECTIONAL LINE

REFERENCE VOLTAGE

TO OTHER I/O RECEIVERS