Nonvolatile semiconductor memory that eases the dielectric strength requirements

Nichtflüchtiges Halbleiterspeicherbauelement, welches die Anforderungen an dessen Spannungsfestigkeit verringert

Mémoire non-volatile à semi-conducteur qui facilite les conditions de rigidité diélectrique

References cited:

Description

[0001] The present invention relates generally to electrically erasable nonvolatile semiconductor memories, and more particularly to a nonvolatile semiconductor memory of the configuration that eases the dielectric strength requirements.

[0002] Electrically rewritable nonvolatile memories include, for example, E²PROM; and among others, flash memory having total or selective total erasure capabilities has been attracting attention in recent years because of its high bit-density capabilities.

The memory cell of the flash memory has a two-layered gate structure consisting of a control gate and a floating gate, in which information storage is accomplished by utilizing the property that when prescribed voltages are applied to the control gate, drain, and source, the current flowing between the drain and the source varies depending on whether or not a charge is stored on the floating gate. Generally, in flash memories, injecting a charge into the floating gate is called writing.

[0003] For writing, a high voltage VPP (about 12 V) is applied to the control gate, about 6 V is applied to the drain, and 0 V is applied to the source. Under these conditions, electrons flowing through the memory cell encounter a high electric field near the drain, and some of the electrons, accelerated by this field, gain enough energy to overcome the energy barrier of the gate insulating film and are injected into the floating gate. Since the floating gate is electrically isolated from other circuit regions, the injected charge can be stored thereon semi-permanently.

[0004] For reading, a supply voltage VCC (about 5 V) is applied to the control gate, about 1 V is applied to the drain, and 0 V is applied to the source. The threshold voltage of the cell transistor varies depending on the presence or absence of a charge on the floating gate, so that the current flowing through the selected memory cell varies accordingly. By sensing and amplifying this current, the information is read out.

[0005] There are two main methods of erasure: one is the channel erasure method in which the charge stored on the floating gate is drawn into the channel, i.e., into the substrate or a well, and the other is the source erasure method in which the charge is drawn into the source.

[0006] In channel erasure, 0 V is applied to the control gate, the drain and source S are left open, and a high voltage VPP (about 12 V) is applied to the channel (p-well). This causes the charge stored on the floating gate to be drawn into the channel. In source erasure, the high voltage VPP is applied to the source, and the channel is left opened or connected to ground.

[0007] The recent trend for semiconductor devices has been toward lower supply voltages, and the reduction of supply voltages has also been pushed forward for flash memories. The lower voltage design also requires the reduction of the high voltage applied to the channel or source for erasure. In a single-voltage device, a booster circuit is used to produce the high voltage, but the problem here is that when the supply voltage is reduced, the booster circuit must be made larger accordingly.

[0008] In the source erasure method, since a high potential is applied to the source, the source diffusion layer must be formed with a greater depth to provide enough dielectric strength to sustain the high potential. This has impeded the effort to reduce the cell area.

[0009] Furthermore, for selective erasure, the circuit must be designed so that the source connection line (VSS line) can be set partially at a different potential. This requires line isolation and the addition of an extra drive circuit, and the chip size is increased accordingly.

[0010] To overcome these problems, there has been proposed a negative voltage application erasure method in which a negative voltage is applied to the control gate to allow a reduction in the positive voltage applied to the channel or source. This method is becoming predominant for erasure.

[0011] Usually, the negative voltage VBB to be applied to the control gate is set to about -10 V, and the supply voltage VCC of 5 V is applied to the channel or source.

[0012] The basic operation of the flash memory has been described above. Nonvolatile memories, such as flash memory, require a high-voltage power supply in addition to the conventional power supply; therefore, for circuits operating at high voltages, high-voltage transistors need to be fabricated in addition to normal-voltage transistors.

[0013] Depletion-mode transistors as well as enhancement-mode transistors are widely used in power supply circuits and the like. The above two types of transistor are distinguished from one another based on the presence or absence of a channel with zero gate bias. In an enhancement-mode device, no channel exists with zero gate bias; in a depletion-mode device, the channel exists with zero gate bias.

[0014] In the case of the depletion-mode transistor, however, since the channel is formed when no gate bias is applied, as described above, the control by the gate bias is complex compared with the enhancement-mode transistor. Therefore, circuit design is usually done based on enhancement-mode devices.

[0015] This does not, however, preclude the use of depletion-mode transistors from the circuit design; depending on applications, far more efficient circuit design may be done using depletion-mode devices rather than using enhancement-mode ones. Constant-voltage sources and signal switching devices (transfer gates) are specific examples.

[0016] Erasure of a flash memory is accomplished by drawing electrons from the floating gate into the channel or into the source by making use of the quantum tunnel effect. However, the current (tunneling current) caused by the electrons being drawn varies exponentially with
the field strength between the floating gate and the channel or the source. As previously noted, for semiconductor devices including flash memories, the trend is toward lower supply voltages, and furthermore, increasing numbers of semiconductor devices are being designed for use with a single power supply. In the flash memory erasure methods using the negative voltage application method, the supply voltage VCC is directly applied to the channel or to the source. In the case of a semiconductor device designed for use with a 3-volt single power supply, for example, if this supply voltage were directly applied to the channel or to the source, the resulting field strength would be smaller than that with a 5-volt power supply. As described above, the field strength between the floating gate and the channel or the source greatly affects the tunneling current. To obtain the same erasure efficiency as the 5-volt devices, an electric field of the same strength as when a 5 V supply voltage is applied must be applied to the tunnel oxide film; if the 3 V supply voltage is applied to the channel or the source, a large negative voltage, which is large in terms of the absolute value, will have to be applied to the control gate. This means application of a large voltage to the oxide film of each transistor used in a booster circuit that generates the large negative voltage, which causes a problem in that it puts extra demands on the voltage withstandin characteristic (reliability) of the transistor.

In semiconductor devices, such as flash memories, that require high voltages, normal-voltage and high-voltage circuits are mixed in the same circuitry. Two kinds of transistors, i.e. 5-volt transistors and 12-volt transistors, are formed in a selective manner, the 12-volt devices being formed in only part of the whole integrated circuit. This, however, increases the complexity of processing and makes the fabrication more difficult.

As previously described, effective circuit design can be realized using depletion-mode transistors for such a power supply circuit as described above. To implement a depletion-mode transistor, a wafer process-like technique is usually used. That is, a large number of charges of the same polarity as the charges that form the channel are distributed in the channel region of a MOS transistor. For example, in the case of an n-channel depletion-mode transistor, the device is formed so that its channel region predominantly contains charges of negative polarity; conversely, a p-channel depletion-mode transistor is formed so that charges of positive polarity are predominant in its channel region. In practice, to provide the MOS transistor channel region with the above charge profile, p- or n-type impurities are ionized and accelerated by a field for injection into the channel region. This technique is generally called ion implantation.

Ion implantation is not only used for the formation of depletion-mode transistors, but the same technique is also used for forming n-channel and p-channel enhancement-mode transistors usually used as circuit elements. However, since enhancement-mode and depletion-mode devices require different charge distributions in the channel region, the charge distribution in the channel region is adjusted by varying the ion dose, the kind of ion implant, the field strength, etc. This means that the fabrication of depletion-mode transistors inevitably involves increased kinds of ion implants in the wafer processing steps. An increased number of processing steps causes such problems as increased complexity of the wafer process and increased time for process setup, leading finally to increased costs of the semiconductor devices.

EP-A-0 520 505 discloses a non-volatile semiconductor memory in which a negative voltage is applied to the control gate and a positive voltage is applied to the source so that charges in the control gate are extracted by means of F-N tunnel current injected into the source.

US-A-4 417 263 discloses a single n-channel transistor having a source connected to a well, providing a voltage regulating circuit of a MOS integrated circuit.

US-A-4 675 557 discloses a voltage level conversion circuit in which a plurality of series connected CMOS FETs located in respective p-wells form a voltage divider used to establish an operating voltage.

TOSHIKATSU JINBO ET AL: 'A 5-V-ONLY 16-MB FLASH MEMORY WITH SECTOR ERASE MODE' IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 27, no. 11, 1 November 1992, pages 1547-1553, XP000320441 discloses a non-volatile semiconductor memory according to the preamble of accompanying claim 1. In a channel erase operation, an internal negative high voltage (about -13v) generated by a negative charge-pumping circuit and a positive pulse (Vcc), are applied to the control gate and the channel respectively.

According to the present invention, there is provided a nonvolatile semiconductor memory circuit which comprises: a plurality of memory cells, each of said memory cells including a floating gate, a control gate, a drain, a source, and a channel formed between said drain and said source; a negative voltage generating means whose generated negative voltage is applied to said control gate for drawing a charge stored in said floating gate out of said floating gate when stored data is erased electrically; and positive erasure voltage generating means which generates a positive voltage applied to said channel in an erase operation, whereby charge stored in said floating gate is drawn into said channel; characterised in that said positive erasure voltage generating means comprises a charge pump booster circuit and generates a positive voltage higher than the supply voltage during said erase operation.

An embodiment of the present invention may provide a nonvolatile semiconductor memory circuit, designed to operate with a low-voltage, single power supply and employing a negative voltage erasure method, wherein large stress is prevented from being applied to the gate oxide film of each transistor used in a booster.
A nonvolatile semiconductor memory circuit embodying the invention is a semiconductor memory in which the stored data can be erased electrically, each storage element of the memory comprising a control gate, a floating gate, a source, and a drain, wherein for erasure a negative voltage generated by negative voltage generating means is applied to the control gate.

For erasure, a voltage higher than the supply voltage is generated by positive erasure voltage generating means, and this erasure voltage is applied to the channel.

According to the constitution of the invention, a higher voltage than the supply voltage is generated by the charge pump booster circuit of the positive erasure voltage generating means and is applied to the channel for erasure, thus achieving high voltage application despite the low-voltage power supply. Therefore, the voltage to be applied to the control gate need not be increased in terms of absolute value. Since a large voltage is not applied to the transistor used in the negative voltage generating means, the problem of dielectric breakdown strength can be avoided.

The present invention will be more clearly understood from the description as set forth below with reference to the accompanying drawings, wherein:

Fig. 1 is a diagram showing a transistor cell structure of a flash memory;
Figs. 2A and 2B are diagrams for explaining read and write methods for the flash memory;
Fig. 3 is a diagram for explaining a channel erasure method utilizing high voltage application;
Fig. 4 is a diagram for explaining a source erasure method utilizing high voltage application;
Fig. 5 is a diagram for explaining a channel erasure method utilizing a negative voltage application method wherein a negative voltage is applied to the control gate;
Fig. 6 is a diagram for explaining a source erasure method utilizing the negative voltage application method;
Fig. 7 is a diagram showing the basic functional constitution of the invention;
Fig. 8 is a diagram showing an arrangement useful for understanding the invention;
Fig. 9 is a block diagram showing the constitution of an embodiment;
Fig. 10 is a diagram showing the circuit constitution of a negative-voltage charge pump circuit of the embodiment;
Fig. 11 is a circuit diagram showing a negative charge pump and a negative bias application circuit;
Fig. 12 is a time chart showing a signal applied to the negative bias application circuit and voltage changes of some nodes of the negative bias application circuit;
Fig. 13 is a time chart showing timing signals for writing of the first embodiment;
Fig. 14 is a time chart showing timing signals for erasure of the first embodiment; and
Fig. 15 is a diagram showing a cross-sectional structure of a negative bias application circuit in the first embodiment.

Before proceeding to a detailed description of the preferred embodiment of the present invention, current nonvolatile semiconductor memories will be described, with reference to the accompanying drawings relating thereto, for a clearer understanding of the differences between current devices and the present invention.

Fig. 1 is a diagram showing an example of a memory cell structure for the flash memory. As shown, the memory cell has a two-layered gate structure consisting of a control gate (CG) 101 and a floating gate (FG) 102, in which information storage is accomplished by utilizing the property that when prescribed voltages are applied to the control gate 101, drain (D) 104, and source (S) 103, the current flowing between the drain 104 and the source 103 varies depending on whether or not a charge is stored on the floating gate 102. Generally, in flash memories, the logic value "H" represents an erased state, i.e., the state in which no charge is stored on the floating gate 102, and the logic value "L" represents the state in which a charge is stored on the floating gate 102. Injecting a charge into the floating gate 102 is called writing.

The following describes how information write, read, and erase operations are performed on the memory cell having the structure shown in Fig. 1. Figs. 2A and 2B show the conditions of voltages applied to the various portions of the flash memory cell for information read and write operations: Fig. 2A for a write operation and Fig. 2B for a read operation.

For writing, a high voltage VPP (about 12 V) is applied to the control gate (CG), about 6 V applied to the drain(D), and 0 V applied to the source (S). Under these conditions, electrons flowing through the memory cell encounter a high electric field near the drain (D), and part of the electrons, accelerated by this field, gain enough energy to overcome the energy barrier of the gate insulating film and are injected into the floating gate (FG). Since the floating gate (FG) is electrically isolated from other circuit regions, the injected charge can be stored thereon semipermanently.

For reading, a supply voltage VCC (about 5 V) is applied to the control gate (CG), about 1 V applied to the drain (D), and 0 V applied to the source (S). The threshold voltage of the cell transistor varies depending on the presence or absence of charge on the floating gate (FG), so that the current flowing through the selected memory cell varies accordingly. By sensing and amplifying this current, the information is read out.

There are two main methods of erasure: one is the channel erasure method in which the charge
stored on the floating gate 102 is drawn into the channel, i.e. into the substrate or a well, and the other is the source erasure method in which the charge is drawn into the source the latter not forming part of the claimed invention.

**[0036]** Fig. 3 shows the conditions of voltages applied to the various portions when erasure is done by applying a high voltage to the channel, and Fig. 4 shows the conditions when erasure is done by applying a high voltage to the source.

**[0037]** As shown in Fig. 3, in channel erasure, 0 V is applied to the control gate CG, the drain D and source S are left open, and a high voltage VPP (about 12 V) is applied to the channel (p-well). This causes the charge stored on the floating gate FG to be drawn into the channel. In source erasure, as shown in Fig. 4, the high voltage VPP is applied to the source, and the channel (the substrate p-sub in the illustrated example) is left open or connected to ground.

**[0038]** As described above, the recent trend for semiconductor devices has been toward lower supply voltages, and the reduction of supply voltages has also been pushed forward for flash memories. The lower voltage design also requires the reduction of the high voltage applied to the channel or source for erasure. In a single-voltage device, a booster circuit is used to produce the high voltage, but the problem here is that when the supply voltage is reduced, the booster circuit must be made larger accordingly.

**[0039]** In the source erasure method, since a high potential is applied to the source S, the source diffusion layer must be formed with a greater depth to provide enough dielectric strength to sustain the high potential. This impedes the effort to reduce the cell area.

**[0040]** Furthermore, for selective erasure, the circuit must be designed so that the source connection line (VSS line) can be set partially at a different potential. This requires the line isolation and the addition of an extra drive circuit, and the chip size is increased accordingly.

**[0041]** To overcome these problems, there has been proposed a negative voltage application erasure method in which a negative voltage is applied to the control gate CG to allow a reduction in the positive voltage applied to the channel or source the latter not forming part of the claimed invention. This method is becoming a predominant method for erasure.

**[0042]** Figs. 5 and 6 are diagrams showing the conditions for channel erasure and source erasure the latter not forming part of the claimed invention, respectively, utilizing the negative voltage application method. Usually, the negative voltage VBB to be applied to the control gate CG is set to about -10 V, and the supply voltage VCC of 5 V is applied to the channel or source.

**[0043]** Erasure of a flash memory is accomplished by drawing electrons from the floating gate into the channel or into the source the latter not forming part of the claimed invention by making use of the quantum tunnel effect. However, the current (tunneling current) caused by the electrons being drawn varies exponentially with the field strength between the floating gate and the channel or the source. As previously noted, for semiconductor devices including flash memories, the trend is toward lower supply voltages, and furthermore, increasing numbers of semiconductor devices are being designed for use with a single power supply. In the flash memory erasure methods using the negative voltage application method, as shown in Figs. 5 and 6, the supply voltage VCC is directly applied to the channel or to the source the latter not forming part of the claimed invention. In the case of a semiconductor device designed for use with a 3-volt single power supply, for example, if this supply voltage were directly applied to the channel or to the source the latter not forming part of the claimed invention, the resulting field strength would be smaller than that with a 5-volt power supply. As described above, the field strength between the floating gate and the channel or the source greatly affects the tunneling current. To obtain the same erasure efficiency as in 5-volt devices, an electric field of the same strength as when a 5 V supply voltage is applied must be applied to the tunnel oxide film; if the 3 V supply voltage is applied to the channel or the source, a large negative voltage, which is large in terms of the absolute value, will have to be applied to the control gate. This means application of a large voltage to the oxide film of each transistor used in a booster circuit that generates the large negative voltage, which causes a problem in that it puts extra demands on the voltage withstand voltage of the transistor.

**[0044]** Figs. 7 is a diagram showing the basic functional configuration of the invention as set forth in the accompanying claims, and fig. 8 shows an arrangement useful for understanding the invention.

**[0045]** As shown in Fig. 7, the nonvolatile semiconductor memory according to the invention is a semiconductor memory in which the stored data can be erased electrically, each storage element of the memory comprising a control gate (CG) 101, a floating gate (FG) 102, a source (S) 103, and a drain (D) 104, wherein for erasure a negative voltage generated by negative voltage generating means 120 is applied to the control gate (CG) 101.

**[0046]** For erasure, a voltage higher than the supply voltage is generated by positive erasure voltage generating means 140, and this erasure voltage is applied to the channel.

**[0047]** According to the configuration of the invention, a voltage higher than the supply voltage is generated by the positive erasure voltage generating means 140 and applied to the channel for erasure, thus achieving high voltage application despite the low-voltage power supply. Therefore, the voltage to be applied to the control gate 101 need not be increased in terms of absolute value. Since a large voltage is not applied to the transistor used in the negative voltage generating means 120, the
Next, the operation of this embodiment will be explained.

[0048] Fig. 9 is a block diagram showing the configuration of a power supply system used for writing and erasure of a flash memory according to an embodiment; Fig. 10 is a circuit diagram showing a portion of Fig. 9 in more detail; Fig. 11 is a circuit diagram showing a negative-voltage charge pump 156 and a negative bias application circuit 158 of Figs. 9 and 10; Fig. 12 shows waveforms for explaining the operations of a negative bias application circuit; Figs. 13 and 14 are timing charts for the signals shown in Figs. 9 and 10; and Fig. 15 is a diagram showing a cross-sectional structure of a negative bias application circuit.

[0049] In Fig. 9, the numeral 151 indicates a command register, 152 indicates a status register, 153 indicates a write/erase switching circuit, and 157 indicates a write/erase timing generating circuit. Flash memories, in general, are constructed so that the write/erase operations and verify operations subsequent thereto are automatically performed just by issuing a command. By an external command signal, data stored in the command register 151 is output and fed to the status register 152, in accordance with which data the write/erase switching circuit switches the various elements into the ready state for a write or erase operation, and the write/erase timing generating circuit supplies control signals, E, /E, and S1 - S6, to the various elements to perform the specified operation. These control signals are shown in Fig. 6 for write and erase operations, respectively.

[0050] To generate voltages larger than the supply voltage in terms of absolute value, necessary for the write and erase operations, a word line positive charge pump 154, a drain positive charge pump 155, and a negative charge pump 156 are provided. The word line positive charge pump 154 is a circuit that generates a high voltage of the order of 12 V for application to the word line to which the control gate of the cell selected for writing is connected. This voltage is applied to a row decoder 164 via a first positive bias application circuit 160. The negative charge pump 156 is a circuit that generates a negative voltage of the order of -10 V for application to a word line 162 during an erase operation. This voltage is applied to the word line via a negative bias application circuit 158. The drain positive charge pump 155 is a circuit that generates a positive voltage of the order of 6 V for application to the drain during a write operation. This voltage is applied via a second positive bias application circuit 159 and a common bus 163 to the bit line to which the cell to be written into is connected. In this embodiment, the drain positive charge pump 155 is used as a booster circuit to generate a voltage applied to the channel for erasure. Therefore, during an erase operation, the positive voltage output from the drain positive charge pump 155 is applied to an erasure channel control 165 via a third positive bias application circuit.

[0051] Fig. 10 is a diagram showing a portion of the circuit of this embodiment in more detail. The reference numerals correspond to those used in Fig. 9. The numeral 171 indicates a matrix array of memory cells, and 175 indicates a well. The numeral 172 indicates a switch array interposed between the bit lines and the common bus line 163. The numeral 174 indicates a gate circuit which is interposed between a word line and the row decoder 164 and which automatically works to disconnect the row decoder 164 from the word line when the negative voltage is applied to the word line via the negative bias circuit 158 during an erase operation. The high voltage from the first positive bias circuit is applied to a power supply terminal VRD of the row decoder 164.
described with reference to Figs. 13 and 14.

In a read operation, S4 - S6 are fixed to either "H" or "L". All the charge pumps are put in the deenergized state. The supply voltage VCC is applied via VRD to the row decoder 164, and the word line is connected to VCC or to ground voltage VSS according to whether it is in the select or the deselct state.

In a write operation, S4 and S6 are fixed to either "H" or "L", and a clock signal is supplied as signal S5, as shown in Fig. 13. Since the levels of S3 and /S3 are fixed, the negative charge pump remains deenergized; on the other hand, since clock signals are supplied as S1, /S3 and S2, /S2, both positive charge pumps 154 and 155 are put in an operating state. As a result, the high voltage is fed to the terminal VRD, so that the word line selected by the row decoder 164 rises to the high voltage while the other word lines remain at 0 V. The positive voltage from the drain positive charge pump 155 is supplied via the second positive bias circuit 159 to the common bus line 163; this positive voltage is applied to the bit line selected by the column decoder.

Since the sources of all the memory cells are grounded, the high voltage is applied to the control gate of the memory cell selected by the address signal and the positive voltage is applied to its drain, with its source and channel grounded, thus accomplishing the writing.

In an erase operation, as shown in Fig. 14, S5 is fixed, and clock signals are supplied as S4 and S6 so that the drain positive charge pump 155 and the negative charge pump 156 are put in an operating state.

As a result, the negative voltage from the negative charge pump 156 is applied via the negative bias circuit 158 to the word line, and the positive voltage from the drain positive charge pump 155 is applied to the well 175 via the third positive bias circuit 161 and via the channel control 165, thus accomplishing the erase.

As described, according to the above embodiment, since the positive voltage is applied to the well 175 during an erase operation, an electric field necessary for erasure can be applied to the tunnel oxide film by applying the negative voltage of the same magnitude as in a previous device to the word line. It is therefore not necessary to supply a negative voltage of a large absolute value to the word line.

In the embodiment, the positive erase voltage is applied to the well for erasure.

Fig. 15 is a diagram showing a cross-sectional structure of the negative bias circuit 158, wherein 181 indicates a polysilicon gate, 182 indicates a gate oxide film, 183 and 184 indicate diffused layers, 185 indicates a well contact, 186 to 188 indicate aluminum connections, 189 indicates an n-well, and 190 indicates a p-substrate. The following describes how the thickness of the gate oxide film 182 is improved by the present invention.

Suppose here that the coupling coefficient of the flash memory is 0.5, the thickness of the tunnel oxide film is 10 nm and the electric field between the floating gate or channel, necessary for erasure, is 100 MV/cm. When the supply voltage is 5 V, if this voltage is to be applied to the well for erasure, a voltage of -10 V will have to be applied to the control gate to achieve the above condition. In Fig. 15, if the potential of the well 189 is at 0 V, the gate oxide film 182 will be subjected to a maximum voltage of 10 V. If the maximum stress field of the transistor of Fig. 15 is 3 MV/cm, the gate oxide film will be required to have a thickness of not less than 35 nm.

On the other hand, if a boosted voltage of 7 V is applied to the channel of the flash memory cell, the control gate need only be supplied with -6 V. Accordingly, the thickness of the gate oxide film 182 of Fig. 15 can be reduced to 20 to 25 nm.

Thus, in the present embodiment, since no large stress is applied to the gate film of each transistor used in the negative charge pump and negative bias circuit, there is no need to form special high-voltage transistors, and thus, the device reliability is improved. Furthermore, as is apparent from the description given so far, the charge pump for generating the positive voltage applied to the drain for writing can also be used as the charge pump for generating the positive voltage applied to the channel for erasure; therefore, no increase in the circuit size is required.

As described above, according to the invention, since there is no need to apply a negative voltage of a large absolute value to the cell control gate for erasure, large stress is not applied to the gate oxide film of each transistor used in the booster circuit provided to generate the negative voltage, the effect being that special high-voltage transistors need not be formed so that the device reliability is increased.

In this specification (including the claims), the terms "positive voltage" and "negative voltage" are used to denote voltages having relatively opposite polarities; they do not necessarily restrict the present invention to use with any absolute polarities of voltage. Moreover, the expression "conventional supply voltage" is not restricted to any particular value of voltage.

Claims

1. A nonvolatile semiconductor memory circuit which comprises:

   a plurality of memory cells, each of said memory cells including a floating gate (102), a control gate (101), a drain (104), a source (103), and a channel formed between said drain and said source;

   a negative voltage generating means (140) whose generated negative voltage is applied to said control gate (101) for drawing a charge stored in said floating gate (102) out of said floating gate when stored data is erased elec-
trically; and positive erasure voltage generating means (140) which generates a positive voltage applied to said channel in an erase operation, whereby charge stored in said floating gate is drawn into said channel;

**characterised in that** said positive erasure voltage generating means (140) comprises a charge pump booster circuit and generates a positive voltage higher than the supply voltage during said erase operation.

2. A nonvolatile semiconductor memory circuit according to claim 1, wherein said memory cells are formed in a well which is formed in said substrate.

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Patentansprüche

1. Nichtflüchtige Halbleiterspeicherschaltung mit:

   einer Vielzahl von Speicherzellen, wobei jede der Speicherzellen ein schwimmendes Gate (102), ein Steuergate (101), ein Drain (104), eine Source (103) und einen zwischen dem Drain und der Source gebildeten Kanal enthält; einem Negativenspannungserzeugungsmittel (140), dessen erzeugte negative Spannung auf das Steuergate (101) angewendet wird, um eine Ladung, die in dem schwimmenden Gate (102) gespeichert ist, aus dem schwimmenden Gate herauszuziehen, wenn gespeicherte Daten elektrisch gelöscht werden; und einem Positivlöschspannungserzeugungsmittel (140), das eine positive Spannung erzeugt, die bei einer Löschoperation auf den Kanal angewendet wird, wodurch eine Ladung, die in dem schwimmenden Gate gespeichert ist, in den Kanal gezogen wird;

   dadurch gekennzeichnet, daß das Positivlöschspannungserzeugungsmittel (140) eine Ladungspumpverstärkerschaltung umfaßt und während der Löschoperation eine positive Spannung erzeugt, die höher als die Zufuhrsspannung ist.

2. Nichtflüchtige Halbleiterspeicherschaltung nach Anspruch 1, bei der die Speicherzellen in einer Mulde gebildet sind, die in dem Substrat gebildet ist.

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Revendications

1. Circuit de mémoire à semiconducteur non volatile qui comprend :

   une pluralité de cellules de mémoire, chacune

   desdites cellules de mémoire incluant une grille flottante (102), une grille de commande (101), un drain (104), une source (103) et un canal qui est formé entre ledit drain et ladite source ;

   un moyen de génération de tension négative (140) dont la tension négative générée est appliquée sur ladite grille de commande (101) pour tirer une charge qui est stockée dans ladite grille flottante (102) hors de ladite grille flottante lorsque des données stockées sont effacées élec- tiquement : et un moyen de génération de tension d’effacement positive (140) qui génère une tension positive qui est appliquée sur ledit canal lors d’une opération d’effacement et ainsi, une charge qui est stockée dans ladite grille flottante est tirée à l’intérieur dudit canal,

   caractérisé en ce que ledit moyen de génération de tension d’effacement positive (140) comprend un circuit de suramplification de pompe de charge et génère une tension positive qui est supérieure à la tension d’alimentation pendant ladite opération d’effacement.

2. Circuit de mémoire à semiconducteur non volatile selon la revendication 1, dans lequel lesdites cellules de mémoire sont formées dans un puits qui est formé dans ledit substrat.
Fig. 2A

WRITE

VPP (APPROX. 12V)

Fig. 2B

READ

VCC (APPROX. 5V)

BIT LINE

(CG FG) (APPROX. 1V)
Fig. 3

[Diagram of a semiconductor device with labeled components and connections]
Fig. 4
Fig. 5
Fig. 8

NEGATIVE VOLTAGE GENERATING MEANS

ERASURE POSITIVE VOLTAGE GENERATING MEANS

POWER SUPPLY (VOLTAGE VS)
Fig. 13

WRITE

E 0
/IR VCC
S1 0
/IS1
S2
/IS2
S3
/IS3
S4
S5
S6

Fig. 14

ERASURE

E VCC
R VCC
S1 0
/IS1 VCC
S2
/IS2
S3
/IS3
S4
S5
S6