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(54) Equalizer for data receiver apparatus
Entzerrer für eine Datenempfangsvorrichtung
Égaliseur pour un appareil de réception de données

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(73) Proprietor: MITSUMASA ELECTRIC INDUSTRIAL CO., LTD.
Kadoma-shi, Osaka-fu, 571 (JP)

(72) Inventors:
- Uesugi, Mitsuru
  Midori-ku, Yokohama-shi (JP)
- Tsubaki, Kazuhisa
  Yokohama-shi (JP)
- Honma, Koutchi
  Yokohama-shi (JP)

(74) Representative: Smith, Norman Ian et al
F.J. CLEVELAND & COMPANY
40-43 Chancery Lane
London WC2A 1JQ (GB)

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Description

BACKGROUND OF THE INVENTION

This invention relates to an equalizer incorporated in a data receiver apparatus used in, for example, a digital mobile radio telephone system.

An equalizer of this kind is described in IEEE Global Telecommunications Conference & Exhibition, Dallas, Texas, November 27-30, 1989. Conference Record Vol.1 of 3, pp.95-101. Such a prior art equalizer will be first described before describing the present invention in detail later.

Fig. 1 shows the structure of one form of a burst signal processed by an equalizer incorporated in a data receiver apparatus used in, for example, a digital mobile radio telephone system, and Fig. 2 shows the waveform of an impulse response of a transmission channel. This impulse response includes not only that of an impulse signal transmitted from a transmitting antenna and directly received by a receiving antenna but also that of the impulse signal reflected by, for example, a building and then received by the receiving antenna with a delay time. Fig. 3 shows the structure of the prior art equalizer incorporated hitherto in the data receiver apparatus. Practically, two equalizers, each of which is as shown in Fig. 3, are used in the data receiver apparatus. In Fig. 3, a received signal is applied from an input terminal 1 to a plurality of delay elements 2. Outputs from a plurality of weighting elements 3 respectively having different weight coefficients are applied to an adder 4, and the output from the adder 4 is applied to a comparator 5 to appear as an output 6 from the equalizer. At the same time, the output 6 from the equalizer is applied to a plurality of delay elements 9 associated with a plurality of weighting elements 10.

The operation of the prior art equalizer shown in Fig. 3 will now be described. Referring to Fig. 3, the received signal is stored in a delay line of each of the delay elements 2 (six samples in the arrangement shown in Fig. 3), and, after the outputs appearing at individual taps are multiplied by the weight coefficients of the weighting elements 3 respectively, the outputs from the weighting elements 3 are added together by the adder 4. Thus, a digital filter of FIR (finite impulse response) type provides an output in which waveform distortion due to the signal transmission through the transmission channel is compensated. The comparator 5 acts to convert the output from the FIR type digital filter into the corresponding amplitude. (For example, in the case of GMSK modulation, the comparator 5 generates its output +1 when its input is positive and -1 when its input is negative.) This output from the comparator 5 provides the output 6 of the equalizer and is stored in a delay line of each of the delay elements 9.

After the outputs appearing at individual taps are multiplied by the weight coefficients of the weighting elements 10 respectively, the outputs from the weighting elements 10 are added together by the adder 4. Thus, a digital filter of IIR (infinite impulse response) type provides an output in which waveform distortion due to the signal transmission through the transmission channel is compensated. In Fig. 3, the digital filter of the FIR type and that of the IIR type are indicated by the blocks 11 and 12 surrounded by broken lines respectively.

The IIR type digital filter referred to above is effective only for waveform distortion due to waveform components (23 to 26 in Fig. 2) appearing after a main waveform component 22 (the component having the highest power level) relative to time. On the other hand, the FIR type digital filter is effective for both the components appearing after and before the main waveform component relative to time. However, the IIR type digital filter is more effective than the FIR type digital filter for the components appearing after the main waveform component relative to time.

Suppose now the case where the equalizer having the structure shown in Fig. 3 is used to deal with a burst signal in which a reference signal part is interposed between a former half data part and a latter half data part as shown in Fig. 1. In the burst signal shown in Fig. 1, both the former and latter half data are voice data subjected already to error correction coding, and the reference signal is in the form of a fixed pattern determined to meet the system. The reference signal part used in the burst signal is a digital pattern of "1" or "0". In the equalizer, the initial values of the weight coefficients of the weighting elements are determined on the basis of the reference signal. Thus, the latter half data part is equalized in a direction as shown by the arrow B in Fig. 1, while the former half data part is equalized in a direction as shown by the arrow A which is opposite to the direction B relative to time t. Therefore, in such a case, it is necessary to use two equalizers each having the structure shown in Fig. 3. Further, in Fig. 3, the range of signal waveform delays is selected to be, for example, 5T, where T represents the length of time of one symbol and is the reciprocal of the bit rate in the case of a binary modulation, such as, the GMSK modulation. That is, T = 5μ when the bit rate = 200 kb/s.

The value of T is so selected, the maximum number of taps required for the FIR type digital filter is 6, because this digital filter is effective for waveform distortion due to both the waveform components appearing after and before the main waveform component relative to time. On the other hand, the maximum number of taps required for the IIR type digital filter is 5, because this digital filter is effective only for waveform distortion due to the components appearing after the main waveform component relative to time. Thus, taking into consideration the condition of the signal transmission channel, it is necessary to provide the maximum number of taps for each of these digital filters. Therefore, in this case, each of the two equalizers includes the 6-tap FIR type digital filter and the 5-tap IIR type digital filter.

As described above, the FIR type digital filter and the IIR type digital filter are combined to form the prior art
equalizer incorporated in the data receiver apparatus. Therefore, the equalizer can compensate both the waveform distortion due to the components appearing after the main waveform component relative to time and that due to the components appearing before the main waveform component relative to time.

However, the prior art equalizer incorporated in the data receiver apparatus has had such various problems that, because the equalizer requires the large number of taps, the number of signal processing is correspondingly increased, and difficulty is encountered for reducing the power consumption and size of the equalizer.

EP-A-0260678 describes an equalizer which comprises a plurality of delay elements and a plurality of weighting elements for multiplying the signal stored in each delay element by a weight coefficient. The weighting elements are connected by switches to an adder, the output of which is fed to a discriminator.

It is an object of the present invention to provide an equalizer for use in a data receiver apparatus, in which the number of required taps is reduced without impairing the effect of compensation of waveform distortion due to signal transmission through a transmission channel, which reduces the number of times of required arithmetic and logical processing to about half of the prior art value, and which facilitates the desired reduction of the power consumption and size.

According to the present invention which attains the above object, the total number of the taps is reduced to about half of the prior art value by disposing a plurality of selector switches in line with the delay lines of the equalizer, so that the number of taps of the FIR and IIR type digital filters can be allocated to be optimized to deal with each burst signal.

According to the present invention there is provided an equalizer for use in a data receiver apparatus comprising:

a plurality of delay elements storing a data signal transmitted through a signal transmission channel and received by a receiving antenna;

a plurality of weighting elements multiplying the signal successively stored in said plural delay elements by their weight coefficients respectively;

an adder adding the output signals from said plural weighting elements; and

discriminator converting the result of addition by said adder into a predetermined amplitude;

characterised in that
a plurality of selector switches are connected between the delay elements and can be selectively switched over to allocate the optimum number of taps which produce the data signal from said delay elements for each burst signal which is contained in the received data signal, and the equalizer includes a controller for controlling switching of said selector switches by estimating the impulse response of the signal transmission channel.

The selector switches disposed in line with the delay lines of the equalizer are used to allocate the number of taps to be optimum for each burst signal, so that the total number of the taps can be reduced to about half of the prior art value, thereby reducing the number of times of required arithmetic and logical processing to about half of the prior art value and attaining the desired reduction of the power consumption and size of the equalizer.

The invention will be described now by way of example only, with particular reference to the accompanying drawings. In the drawings:

Fig. 1 shows the structure of one form of a burst signal.

Fig. 2 is a waveform diagram showing an impulse response of a data signal transmission channel.

Fig. 3 is a block diagram showing the structure of a prior art equalizer incorporated hitherto in a data receiver apparatus.

Fig. 4 is a block diagram showing the structure of an embodiment of the equalizer of the present invention suitable for use in a data receiver apparatus.

Fig. 5 shows the structure of a data receiver apparatus in which two equalizers embodying the present invention are incorporated.

Figs. 6A and 6B illustrate two forms of a channel impulse response.

Fig. 7 is a block diagram showing in detail the relation between the controller and one of the equalizers shown in Fig. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 4 is a block diagram showing the structure of an embodiment of the equalizer of the present invention suitable for use in a data receiver apparatus, and, in Fig. 4, like reference numerals are used to designate like parts appearing in Fig. 3. Referring to Fig. 4, an input signal is applied through a signal input terminal 1 to a plurality of delay elements 2. Outputs from a plurality of weighting elements 3 are applied to an adder 4, and the output from the adder 4 is applied to a comparator 5 to appear as an output 6 from the equalizer. At the same time, the output 6 from the equalizer is applied to another delay element 8. The equalizer according to the present invention further comprises a plurality of
selector switches 7a to 7e disposed in line with the respective delay elements 2.

Fig 5 shows the structure of a data receiver apparatus in which two equalizers 33 and 34 each having the structure as shown in Fig 4 are incorporated. Referring to Fig 5, an RF signal received by an antenna 30 is converted into its baseband signal by a demodulator 31. The RF signal referred to herein is a digital signal. The baseband signal is temporarily stored in a memory 32 before it is applied to the equalizers 33, 34, and a controller 35. The controller 35 controls the selector switches 7 in the equalizers 33 and 34 in response to the baseband signal stored in and applied from the memory 32. An error corrector 36 carries out error correction and decoding of the baseband signal, because the RF signal received by the antenna 30 has been subjected already to error correction coding at the signal transmitter. The digital signal subjected to the error correction and decoding in the error corrector 36 is then decoded into its original voice signal by a voice signal decoder 37 to appear as an output of the data receiver apparatus.

The operation of the data receiver apparatus shown in Fig 5 will now be described. First, an RF signal received by the antenna 30 is demodulated by the demodulator 31 into its baseband signal. Then, the demodulated baseband signal is temporarily stored in the memory 32. This is because the input signal consists of a former half data part, a reference signal part and a latter half data part continuously arrayed from the left toward the right on the time base.

Therefore, after storing the baseband signal in the memory 32, the latter half data part is equalized in the order of from the reference signal part to the latter half data part in the direction of the arrow B in Fig 1, while the former half data part is equalized in the order of from the reference signal part to the former half data part in the direction of the arrow A which is opposite to the direction of progress of the time t. It is apparent that the equalizers 33 and 34 carry out selective equalization of the former half data part and the latter half data part only.

Suppose now the case where these equalizers 33 and 34 are used to deal with a burst signal in which a reference signal part is interspersed between a former half data part and a latter half data part as shown in Fig 1. Herein, the reference signal is a known signal, and its auto-correlation is represented by an impulse signal as shown in Fig 6A. Therefore, when the correlation between the input of the equalizers 33, 34 and the pattern of the reference signal that is the known signal is taken, the result is as shown in Fig 6A when the input is free from waveform distortion. On the other hand, when the input includes a waveform component reflected from an obstacle existing in the signal transmission channel, the result will be as shown in Fig 6B. That is, the channel impulse response can be estimated. In Fig. 6B, the symbol α indicates the signal transmitted from the transmitting antenna and directly received by the receiving antenna, while the symbol β indicates the signal reflected by, for example, a building and received by the receiving antenna with a time difference Δt. Therefore, when the channel impulse response is detected, the desired impulse response of each of the equalizers 33 and 34 is determined so that the result of convolution between the detected channel impulse response and the desired equalizer impulse response becomes as close to the channel impulse response shown in Fig 6A as possible, thereby determining the initial values of the weight coefficients of the weighting elements. More concretely, the matrix is prepared on the basis of the auto-correlation of the input of the equalizers 33, 34, and for each impulse response of the impulsive signal is detected in the equalizer input and the known signal so as to determine the initial values of weight coefficients by solving the matrix. The input signal is equalized by the use of these initial values of the weight coefficients so determined. These initial values are determined for each burst signal.

When the range of the signal waveform delays in the impulse response of the signal transmission channel is, for example, 5T as shown in Fig 2, the maximum number of required taps is 6 in the case of the FIR type digital filter and 5 in the case of the IIR type digital filter. Thus, the range of the signal waveform delays differs depending on the condition of the signal transmission channel, and the maximum number of the required taps of each of the equalizers 33 and 34 differs also depending on the condition of the signal transmission channel. Suppose now that the impulse response of the signal transmission channel is, for example, as shown in Fig 2. In such a case, wave components 23 to 26 are delayed by 4T from the main waveform component 22 relative to time, and the waveform component 21 is advanced by 1T from the main waveform component 22 relative to time. In this case, the FIR type digital filter having 2 taps and the IIR type digital filter having 4 taps can satisfactorily deal with the latter half data part of the burst signal, while the FIR type digital filter having 5 taps and the IIR type digital filter having 1 tap can satisfactorily deal with the former half data part of the burst signal. This is because, in the case of the equalizer for equalizing the latter half data part of the burst signal in the order of from the reference signal part to the latter half data part in the direction of the arrow B in Fig 1, the FIR type digital filter which is effective for cancelling the waveform component 21 appearing before the main waveform component 22 (whose power level is highest of all) relative to time requires the number of taps larger than p + 1 at least, where p is the number of waveform components appearing before the main waveform component 22 relative to time, while the IIR type digital filter which is effective for cancelling the waveform components 23 to 26 appearing after the main waveform component 22 relative to time requires the number of taps larger than q at least, where q is the number of waveform components appearing after the main waveform component 22 relative to time. On the other hand, the equalizer dealing with the former half data part of the burst signal equalizes in the order of from the reference signal part to the former half data part in the direction of the arrow A in Fig 1, that is, in the relation inverted with respect to time. Therefore, the number of taps of each of its digital filters is determined by inverting the impulse response shown in Fig 2 with respect to time.
Thus, when the numbers of taps of the FIR type and IIR type digital filters forming the equalizer dealing with the latter half data part of the burst signal are A and B respectively, and those of the FIR type and IIR type digital filters forming the equalizer dealing with the former half data part of the burst signal are C and D respectively, these equalizers can operate to exhibit the performance equivalent to that of the prior art equalizer when the values of A, B, C and D are selected to satisfy the relations A + B = C + D = 6, A + C = 7 and B + D = 5 (A, C = 1 to 6, and B, D = 0 to 5).

Therefore, each of the two equalizers is designed to include the selector switches 7 as shown in Fig. 4. It is considered herein that the range of signal waveform delays is nT (n: a natural number). According to such a consideration, the above relations among A, B, C and D are now expressed as A + B = C + D = n + 1, A + C = n + 2, and B + D = n (A, C = 1 to n + 1, and B, D = 0 to n). Thus, whereas the total number of taps of the prior art equalizer is 2X (2n + 1), the total number of taps of the two equalizers used in the present invention is 2X (n + 1) which is about half of the prior art value.

The manner of switch-over of the selector switches 7 will be described by reference to Fig. 7. In Fig. 7, the equalizer 34 controlled by the controller 35 is used to deal with the latter half data part of the burst signal. Referring to Fig. 7, an impulse response estimator 41 estimates the channel impulse response, and, on the basis of the estimated channel impulse response, a tap shaping determiner 42 determines the shaping of the taps. The output of the tap shaping determiner 42 is applied to a switch controller 43 which controls the selector switches 7. Describing in more detail, the channel impulse response estimator 41 computes the cross-correlation between the received signal (temporarily stored in and outputted from the memory 32) and the known signal (the fixed value), and the result of computation of the cross-correlation is regarded as the channel impulse response. In response to the output from the channel impulse response estimator 41, the tap shaping determiner 42 detects the timing of appearance of the main waveform component 22 (having the highest power level) with respect to time, and, on the basis of the detected timing of the main waveform component 22 (which appears as a second waveform component in Fig. 2), determines the respective numbers of taps to be shaped to the FIR type and IIR type digital filters. Table 1 shows the number of taps shaped to each of the FIR type and IIR type digital filters together with the position of each of the selector switches 7a to 7e, by way of example. The switch controller 43 controls the position of each of the selector switches 7a to 7e in the equalizer according to the result of the tap shaping determined by the tap shaping determiner 42 as shown in Table 1. Also, when the number of required taps of the FIR type digital filter in the equalizer dealing with the latter half data part of the burst signal is so determined, the number of required taps of the IIR type digital filter in the equalizer dealing with the latter half data part of the burst signal, and those of the FIR type and IIR type digital filters forming the equalizer dealing with the former half data part of the burst signal can be primarily determined. Therefore, the information regarding the number of required taps of the FIR type digital filter only of the equalizer dealing with the latter half data part of the burst signal need be supplied from the tap shaping determiner 42 to the switch controller 43. Fig. 7 shows that the selector switch 7b only is set in its "upper" position, and, in this case, the number of taps of the FIR type digital filter is 2, while that of the IIR type digital filter is 4. In Fig. 7, these digital filters are indicated by the blocks surrounded by the broken lines 13 and 14 respectively.

<table>
<thead>
<tr>
<th>Number of taps</th>
<th>Position of selector switches 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>0 low low low low low</td>
</tr>
<tr>
<td>5</td>
<td>1 low low low low up</td>
</tr>
<tr>
<td>4</td>
<td>2 low low low up low</td>
</tr>
<tr>
<td>3</td>
<td>3 low low up low low</td>
</tr>
<tr>
<td>2</td>
<td>4 up low low low low</td>
</tr>
<tr>
<td>1</td>
<td>5 up low low low low</td>
</tr>
</tbody>
</table>

Therefore, the selector switches 7 shown in Fig. 4 operate relative to each other as shown in Table 1 according to the condition of the signal transmission channel so that the numbers of taps of the FIR type and IIR type digital filters are shaped respectively to meet the relations described above. The output signal from the memory 32 is stored in the delay lines of the delay elements 2, and, after the outputs from the individual taps are multiplied by the weight coefficients of the respective weighting elements 3, the outputs from the weighting elements 3 are added together in the adder 4, so that the adder 4 provides the output in which waveform distortion due to signal transmission through the signal transmission channel is compensated by the function of the FIR type digital filter. The output from the adder 4 is converted into the predetermined amplitude by the discriminator 5. (In the case of, for example, the GMSK modulation,
the discriminator 5 generates its output 1 and -1 when its input is positive and, negative respectively.) The discriminator output appears as the output 6 from the equalizer and is, at the same time, fed back through the delay element 8, so that waveform distortion due to signal transmission through the transmission channel is also compensated by the function of the IIR type digital filter.

It will be understood from the foregoing description of the embodiment of the equalizer according to the present invention that the number of taps of the IIR type digital filter and that of the IIR type digital filter are shaped by the function of the selector switches 7 each time the burst signal is received. Therefore, the present invention is advantageous in that the total number of the required taps of the equalizer can be reduced to about the half of the prior art value.

Claims

1. An equalizer for use in a data receiver apparatus comprising:

   a plurality of delay elements (2) storing a data signal transmitted through a signal transmission channel and received by a receiving antenna;
   a plurality of weighting elements (3) multiplying the signal successively stored in said plural delay elements by their weight coefficients respectively;
   an adder (4) adding the output signals from said plural weighting elements; and
   a discriminator (5) converting the result of addition by said adder into a predetermined amplitude;

   characterised in that
   a plurality of selector switches (7) are connected between the delay elements (2) and can be selectively switched over to allocate the optimum number of taps which produce the data signal from said delay elements for each burst signal which is contained in the received data signal, and the equalizer includes a controller (35) for controlling switching of said selector switches (7) by estimating the impulse response of the signal transmission channel.

2. An equalizer according to claim 1 including
   feedback paths including a delay element (8) for feeding back the output signal of said discriminator to the respective output terminals of said plural delay elements.

3. An equalizer according to claim 2, wherein said controller (35) is arranged to switch only one of said plural selector switches (7) to said feedback paths by estimating an impulse response of the signal transmission channel to provide a feedback value.

4. A data receiver apparatus including:

   a memory (32) storing a received signal transmitted through a signal transmission channel and demodulated into its baseband signal by a demodulator (31);
   an equalizer (33, 34) equalizing the received signal demodulated into its baseband signal;
   an error corrector (36) correcting any error included in the output signal from said equalizer; and
   a voice decoder (37) decoding the voice data of the signal subjected to the error correction by said error corrector, wherein
   said equalizer is an equalizer according to any preceding claim in which said plurality of delay elements (2) successively delay the input signal applied from said memory; and
   said plurality of weighting element (3) multiply the input signal from said memory and the successively delayed output signals from said plural delay elements by their weight coefficients respectively.

5. A data receiver apparatus according to claim 4, wherein said controller (35) controls switching of said plural selector switches (7) for estimating the impulse response of the signal transmission channel.

Patentansprüche

1. Entzerrvorrichtung zur Verwendung in einer Datenempfangsleitung aufweisend:

   eine Mehrzahl von Verzögerungselementen (2), die ein Datensignal speichern, welches durch einen Signal-
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übertragungskanal übertragen und durch eine Empfangsantenne empfangen wurde; eine Mehrzahl von Gewichtungselementen (3), die das Signal, welches sukzessive in den mehreren Verzögerungselementen gespeichert ist, jeweils mit ihren Gewichtungskoefizienten multiplizieren; eine Addiereinrichtung (4), die die Ausgangssignale von den mehreren Gewichtungselementen addiert; und einen Diskriminator (5), der das Ergebnis der vom Addierer durchgeführten Addition in eine vorbestimmte Amplitude umsetzt:

dadurch gekennzeichnet, daß eine Mehrzahl von Wahlsschaltern (7) zwischen die Verzögerungselemente (2) geschaltet sind und selektiv hinübergeschaltet werden können, um die optimale Anzahl von Abgriffstellen zuzuweisen, welche das Datensignal von den Verzögerungselementen für jedes Signalbündel erzeugen, welches in dem empfangenen Datensignal enthalten ist und die Entzerrvorrichtung eine Steuereinrichtung (35) zum Steuern des Schaltens der Wahlsschalter (7) enthält, und zwar durch Berechnen der Impulsantwort des Signalübertragungskanals.

2. Entzerrvorrichtung nach Anspruch 1, die ein Verzögerungselement (6) enthaltende Rückführwege zum Zurückführen des Ausgangssignals des Diskriminators zu den jeweiligen Ausgangsanschlüssen der mehreren Verzögerungselemente enthält.

3. Entzerrvorrichtung nach Anspruch 2, bei der die Steuereinrichtung (35) angeordnet ist, um lediglich einen der mehreren Wahlsschalter (7) auf die Rückführwege zu schalten, und zwar durch Berechnen der Impulsantwort des Signalübertragungskanals, um einen Rückführwert zu liefern.

4. Datenempfangsverrichtung aufweisend:

eine Speichereinrichtung (32), welche ein empfangenes Signal speichert, das durch einen Signalübertragungskanal übertragen und durch einen Demodulator (31) in sein Basisbandsignal demoduliert wurde; eine Entzerrvorrichtung (33, 34), welche das empfangene, in sein Basisbandsignal demodulierte Signal entzerrt;
eine Fehlerkorrektureinrichtung (36), welche jeglichen Fehler korrigiert, der im Ausgangssignal von der Entzerrvorrichtung enthalten ist; und

eine Tondokierereinrichtung (37), welche die Tondaten des Signals dekodiert, welches der Fehlerkorrektur durch die Fehlerkorrekturereinrichtung unterzogen wurde, wobei die Entzerrvorrichtung eine Entzerrvorrichtung nach einem beliebigen vorstehenden Anspruch ist, bei der die mehreren Verzögerungselemente (2) sukzessive das von der Speichereinrichtung zugeführte Eingangssignal verzögern; und
die mehreren Gewichtungselemente (3) das Eingangssignal von der Speichereinrichtung und die sukzessive verzögerten Ausgangssignale von den mehreren Verzögerungselementen jeweils mit ihren Gewichtungskoeffizienten multiplizieren.

5. Datenempfangsverrichtung nach Anspruch 4, bei der die Steuereinrichtung (35) das Schalten der mehreren Wahlsschalter (7) zum Berechnen der Impulsantwort des Signalübertragungskanals steuert.

Revidierungen

1. Égaliseur destiné à être utilisé dans un appareil de réception de données, comprenant:

plusieurs éléments à retard (2) mémorisant un signal de données transmis par une voie de transmission de signaux et reçu par une antenne réceptrice;
plusieurs éléments de pondération (3) multipliant, respectivement par leurs coefficients de pondération, le signal mémorisé successivement dans lesdits éléments à retard;
un addionneur (4) additionnant les signaux de sortie desdits éléments de pondération; et
un discriminateur (5) convertissant le résultat de l'addition effectuée par ledit addionneur en une amplitude prédéterminée;

caractérisé en ce que plusieurs commutateurs sélecteurs (7) sont montés entre les éléments à retard (2) et peuvent être commutés sélectivement pour affecter le nombre optimal de prises produisant le signal de données à partir desdits éléments à retard pour chaque signal en salve qui est contenu dans le signal de données reçu, et
2. Égaliseur selon la revendication 1, comprenant des boucles de rétroaction contenant un élément à retard (8) pour réinjecter le signal de sortie dudit discriminateur aux bornes de sortie respectives d’édits éléments à retard.

3. Égaliseur selon la revendication 2, dans lequel ladite unité de commande (35) est agencée de façon à ne commuter que l’un d’édits commutateurs sélecteurs (7) sur d’édits boucles de rétroaction en estimant une réponse impulsionnelle de la voie de transmission de signaux pour fournir une valeur de rétroaction.

4. Appareil de réception de données, comprenant:

- une mémoire (32) qui mémorise un signal reçu, transmis par une voie de transmission de signaux et démodulé en son signal dans la bande de base par un démodulateur (31);
- un égaliseur (33,34) qui égalise le signal reçu, démodulé en son signal dans la bande de base;
- un correcteur d’erreurs (36) qui corrige une erreur éventuellement contenue dans le signal de sortie dudit égaliseur; et
- un décodeur vocal (37) qui décide les informations vocales du signal soumis à la correction d’erreur effectuée par ledit correcteur d’erreurs.

5. Appareil de réception de données selon la revendication 4, dans lequel ladite unité de commande (35) commande la commutation d’édits commutateurs sélecteurs (7) pour estimer la réponse impulsionnelle de la voie de transmission de signaux.