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Semiconductor lateral insulated gate bipolar transistor
Lateraler, bipolärer Halbleitertransistor mit isolierter Steuerelektrode
Transistor semi-conducteur bipolaire latéral à grille isolée

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EP-A- 0 097 442
EP-A- 0 238 749
EP-A- 0 361 589
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EP-A- 0 345 380
EP-A- 0 371 785

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Description

The invention relates to a semiconductor lateral insulated gate bipolar transistor and more specifically to a lateral trench-gate bipolar transistor (LTGBT) device suitable for power integrated circuit applications.

In the field of power integrated circuits, device designers seek to achieve devices with low on-resistance, fast switching times and high breakdown voltage. One category of devices which has exhibited considerable promise in these areas is the insulated-gate bipolar transistor (IGBT), a class of devices which incorporates the insulated-gate structure of a conventional majority-carrier MOS device, and additionally uses minority carrier conduction for conductivity modulation. Representative prior-art IGBT devices are shown in EP O 111 803, EP O 372 391, EP O 371 785 and DE 3620677. Examples of other types of structures, using various trench configurations, are shown in U.S. Patent No. 4,546,357 and EP O 047 392.

Although minority-carrier IGBT devices have received considerable attention because of their favourable performance characteristics when used in high-power applications, these devices have heretofore suffered from an important drawback. In particular, conductivity-modulated power devices tend to "latch up" at high current densities, a problem which is exacerbated when high voltages are also present. Since high-current and/or high voltage conditions are always encountered in power devices, a way is needed to provide conductivity-modulated power devices with high resistance to Latch up. Absent such an improvement, these devices will tend to "latch up" in a manner similar to that exhibited by thyristors, such that they will be unable to be turned "off". This may result in temporary, or even permanent, damage to the devices.

A major cause of latch-up can be found in the hole current in the channel region below the source, which is a result of the fact that the source/channel contact is located at the side remote from the drain/anode, as can be seen e.g. in EP O 371 785.

A prior-art solution to this problem has been to increase the doping of the channel region in IGBT devices. This lowers the channel resistance, and therefore the voltage drop across the channel during conduction, resulting in a more latch-up resistant device. However, a major drawback of this technique is that the threshold voltage of the device is thereby increased, typically to a level where it is difficult to provide a sufficient gate turn-on voltage. Furthermore, this expedient only reduces, but does not eliminate, the problem.

Accordingly, a substantial need exists for a device which will incorporate the inherent advantages of conventional IGBT devices, while at the same time affording substantially improved resistance to latch up.

It is therefore an object of the present invention to provide an IGBT device having low on-resistance, fast switching characteristics, and high breakdown voltage, while at the same time offering substantially improved resistance to latch-up in high-power and/or high-voltage circuit applications.

It is a further object of the invention to provide an IGBT device with the aforementioned advantages which is also simple and compact in construction, and capable of being fabricated in SOI technology.

In accordance with a first aspect of the invention, these objects are achieved by a new configuration of a semiconductor device, hereinafter referred to as a "Lateral Trench-Gate Bipolar Transistor" (LTGBT) device, which comprises

a semiconductor substrate of a first conductivity type having a major surface,
a semiconductor substrate surface layer of a second conductivity type opposite that of the first located on said major surface,
a trench extending entirely through said surface layer, surrounding a portion of said surface layer thereby defining an island in said surface layer and having an inner sidewall, an outer sidewall and a floor, the inner sidewall bounding said island, a dielectric layer covering the sidewalls and floor of said trench,
a gate region lying within said trench on said dielectric layer and comprising a conductive material, a surface-adjoining channel region of said first conductivity type located in said island of said surface layer and adjoining said inner sidewall of said trench,
a surface-adjoining first device region located in a central portion of said island of said surface layer and spaced apart from said channel region,
a surface-adjoining second device region located in said channel region and comprising at least a highly-doped surface-adjoining zone of said second conductivity type adjacent said inner sidewall of said trench an electrode (A) providing an electrical connection to said first device region, and an electrode (K) providing an electrical connection to said second device region, said gate region extending in a substantially vertical direction adjacent said second device region and said channel region, whereby a substantially vertical conduction channel is induced in the channel region during operation.

In accordance with a second aspect of the invention, semiconductor lateral insulated gate bipolar transistor device comprises;

a semiconductor substrate of a first conductivity type having a major surface,
an insulating layer located on said major surface, a semiconductor surface layer of a second conductivity type opposite that of the first located on said
insulating layer, whereby the insulating layer is a buried insulating layer, a trench extending entirely through said surface layer, surrounding a portion of said surface layer thereby defining an island in said surface layer, and having an inner sidewall, an outer sidewall and a floor, the inner sidewall bounding said island, a dielectric layer covering the sidewalks and floor of said trench, a gate region lying within said trench on said dielectric layer and comprising a conductive material, a surface-adjacently connected region of said first conductivity type located in said island of said surface layer and adjoining said inner sidewalk of said trench, a surface-adjacently connected device region located in a central portion of said island of said surface layer and spaced apart from said channel region, a surface-adjacently connected second device region located in said channel region and comprising at least a highly doped surface-adjacently connected zone of said second conductivity type adjacent said inner sidewalk of said trench, an electrode (A) providing an electrical connection to said first device region, and an electrode (K) providing an electrical connection to said second device region, said gate region extending in a substantially vertical direction adjacent said second device region and said channel region, whereby a substantially vertical conduction channel is induced in the channel region during operation.

In essence, these configurations result in lateral device structures, with both the first and second device region being adjacent to the same surface, while at the same time providing a vertical conduction channel controlled by an insulated gate region extending within a trench entirely through the surface layer in a substantially vertical direction adjacent the channel region.

This unique configuration provides a lateral surface-adjacently connected path from anode to cathode for holes, and a second path which extends from the cathode, down for a short distance through the vertical conduction channel and then across in a lateral direction to the anode. Since minority carriers (holes) can flow to the cathode directly, in the lateral direction, without first flowing through the vertical conduction channel, forward bias of the cathode-channel junction is minimized. This will prevent turn-on of the parasitic npn transistor inherent in the structure, and thereby prevent latch-up, even at high current densities. Furthermore, since electron flow is initially in a downward direction, electron-hole recombination currents can now flow in the body of the device, rather than at the surface as is the case of prior art lateral insulated gate bipolar transistors. Another advantage of the proposed structures is that, since the gate-controlled channel conducting region is substantially vertical, the dimensions of this region can be optimized, while at the same time the lateral dimension of the channel region can be increased in order to provide field shaping, which results in improved high-voltage breakdown characteristics.

Additionally, since the LTGBT device can be formed on a buried insulating layer, the entire device can be easily and effectively insulated, thus making it particularly suitable for applications, such as source-follower "high side" switches, which require high-voltage insulation of the entire device.

Fig. 1 is a cross-sectional view of a lateral trench-gate bipolar transistor (LTGBT) device in accordance with a first embodiment of the invention, and Fig. 2 is a cross-sectional view of an LTGBT device fabricated on an insulating layer in accordance with a second embodiment of the invention.

It should be noted that the figures are not drawn to scale, and in particular that the vertical dimensions are exaggerated for improved clarity. Additionally, semiconductor regions of the same conductivity type are generally shown hatched in the same direction, and corresponding regions in different figures are generally designated by the same reference numerals.

Fig. 1 of the drawing shows a lateral trench-gate bipolar transistor (LTGBT) device in accordance with a first embodiment of the invention. In Fig. 1, LTGBT device 1 has a semiconductor substrate 10 of a first conductivity type, here p-type. The substrate is relatively lightly doped, with a typical doping Concentration of about 10^{14} atoms/cm^3. An epitaxial semiconductor surface layer 14 of a second conductivity type opposite to that of the first, here n-type, is provided on a first major surface 12 of the substrate, and forms a p-n junction therewith. The epitaxial layer 14 may typically have a thickness of about 2.5 microns and a charge per unit area of between 1 and 2 \times 10^{12} atoms/cm^2. A trench 16 is provided in the epitaxial surface layer 14 and extends entirely through the epitaxial layer. This trench, which may be formed by a conventional technique such as etching, can typically be about 2 microns wide and surrounds the active portion of the device.

A dielectric layer 18, which may typically be a silicon oxide film of about 0.05 microns thickness, covers the sidewalls and floor of the trench. The dielectric-covered trench contains a gate region 20 which is formed of a conductive material such as polysilicon, and which can be fabricated by a standard process such as poly refill. A gate electrode G is provided to make electrical contact to the gate region 20.

A surface-adjacently connected channel region 22 of p-type conductivity is provided in the epitaxial layer 14 adjoining the inner side wall of trench 16. The channel region 22 extends vertically through a portion of the epitaxial surface layer and extends laterally inward from the inner side wall of the trench towards a central portion of the
LTGBT device. Although the configuration of this channel region may vary greatly as a function of device design requirements, this region may typically be about 1.5 microns thick and have a doping concentration of about $10^{17}$ atoms/cm$^3$ and a length of about 20 to 25 microns in the lateral direction.

The LTGBT device of Fig. 1 further includes a surface-adjacent second device region 24, referred to as cathode region, having a highly-doped n-type surface-adjointing zone 24a adjacent the inner sidewall of trench 16 and extending downwardly through a portion of the channel region 22. In this embodiment, the cathode region further includes a second highly-doped surface-adjointing zone 24b of p-type conductivity which is provided adjacent to zone 24a and serves to enhance the connection to the channel region 22. Zones 24a and 24b of the cathode region 24 may both typically be about 0.5 microns thick and have a relatively high doping concentration of about $10^{20}$ atoms/cm$^3$. The width of zones 24a and 24b may typically be about 5 microns each, with an electrical connection to the channel region being provided by cathode electrode K, which contacts both zone 24a and zone 24b.

The LTGBT device construction is completed by a surface-adjointing first device region 26, referred to as anode region, which forms a p-n junction with the epitaxial layer 14. Anode region 26 is located in the central portion of the epitaxial layer, and is spaced apart from the channel region 22. An anode electrode A provides an electrical connection to the anode region 26. In the embodiment shown in Fig. 1, the surface-adjointing anode region includes a highly-doped p-type surface-adjointing region 26, which may typically have a thickness of about 0.5 microns and a doping concentration of about $10^{20}$ atoms/cm$^3$. Although alternative configurations are expressly within the scope of the invention. Thus, for example, the anode region may be provided as a segmented p-i-n anode, a segmented p-i-n Schottky anode or as a pure Schottky diode in order to enhance switching speed. These alternative anode structures are known in the prior art, and are described in EP-A-0 361 589, entitled SEGMENTED-ANODE LATERAL INSULATED-GATE BIPOLAR TRANSISTOR DEVICES, by MUKHERJEE et al, incorporated herein by reference. Accordingly, these features are not shown or further described herein in the interest of brevity.

The unique configuration of the channel region 22, which provides a substantially vertical conduction channel 22a between the cathode region and the underlying portion of the epitaxial layer even though the channel region as a whole is laterally oriented, permits the simultaneous optimization of several parameters which in conventional devices must be selected in a manner that results in a trade-off. Thus, for example, the substantially vertical conduction channel 22a can be kept desirably short, while the channel region itself can be extended inappropriately toward the anode region in order to improve high-voltage breakdown characteristics. In a particularly advantageous configuration, the channel region 22 extends laterally inwardly beyond cathode region zone 24b for a distance which is about 1/2 of the distance between cathode region zone 24b and anode region 26.

A second embodiment of an LTGBT device in accordance with the invention is shown in Fig. 2. This embodiment is generally similar to the configuration shown in Fig. 1, but with one important difference. Rather than having the substrate 10 and epitaxial layer 14 meet at a p-n junction at surface 12 to provide junction isolation for the device, the epitaxial surface layer and substrate may be isolated from each other by a buried insulating layer 13 provided on the substrate 10, with the epitaxial surface layer 14 being provided on the buried insulating layer. Buried insulating layer 13 may typically be a layer of about 0.5 microns of thermal silicon oxide, formed in a conventional manner. Thus, a silicon-on-insulator (SOI) LTGBT device is formed, with the device being completely oxide-insulated from all surrounding semiconductor regions. Accordingly, the structure shown in Fig. 2 is particularly suitable for high-voltage applications such as source-follower high-side switches, where the entire device must be effectively insulated to withstand high voltages without danger of breakdown.

In summary, devices in accordance with the present invention are capable of providing all of the advantages associated with prior-art LTGBT devices, while at the same time overcoming the most significant drawback of the prior structures, namely their susceptibility to potentially damaging latch-up at high current and/or high voltage levels. Furthermore, the devices disclosed herein are particularly adaptable to SOI technology, thus permitting a wide range of high-voltage circuit applications.

While the invention has been particularly shown and described with reference to several preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the scope of the invention as defined by the appended claims.

Claims

1. A semiconductor lateral insulated gate bipolar transistor device (1) comprising

   a semiconductor substrate (10) of a first conductivity type having a major surface (12),
   a semiconductor surface layer (14) of a second conductivity type opposite that of the first located on said major surface (12),
   a trench (16) extending entirely through said surface layer (14), surrounding a portion of said surface layer (14) thereby defining an island in said surface layer (14), and having an inner sidewall, an outer sidewall and a floor, the inner sidewall bounding said island,
   a dielectric layer (18) covering the sidewalls
and floor of said trench (16), a gate region (20) lying within said trench on said dielectric layer (18) and comprising a conductive material, a surface-adjointing channel region (22) of said first conductivity type located in said island of said surface layer (14) and adjoining said inner sidewall of said trench (16), a surface-adjointing first device region (26) located in a central portion of said island of said surface layer (14) and spaced apart from said channel region (22), a surface-adjointing second device region (24a, 24b) located in said channel region (22) and comprising at least a highly-doped surface-adjointing zone (24a) of said second conductivity type adjacent said inner sidewall of said trench (16), an electrode (A) providing an electrical connection to said first device region (26), and an electrode (K) providing an electrical connection to said second device region (24a, 24b), said gate region (20) extending in a substantially vertical direction adjacent said second device region (24a, 24b) and said channel region (22), whereby a substantially vertical conduction channel is induced in the channel region (22) during operation.

2. A semiconductor lateral insulated gate bipolar transistor device (1) comprising

a semiconductor substrate (10) of a first conductivity type having a major surface (12), an insulating layer (13) located on said major surface (12), a semiconductor surface layer (14) of a second conductivity type opposite that of the first located on said insulating layer (12), whereby the insulating layer (13) is a buried insulating layer, a trench (16) extending entirely through said surface layer (14), surrounding a portion of said surface layer (14) thereby defining an island in said surface layer (14), and having an inner sidewall, an outer sidewall and a floor, the inner sidewall bounding said island, a dielectric layer (18) covering the sidewalls and floor of said trench (16), a gate region (20) lying within said trench on said dielectric layer (18) and comprising a conductive material, a surface-adjointing channel region (22) of said first conductivity type located in said island of said surface layer (14) and adjoining said inner sidewall of said trench (16), a surface-adjointing first device region (26) located in a central portion of said island of said surface layer (14) and spaced apart from said channel region (22), a surface-adjointing second device region (24a, 24b) located in said channel region (22) and comprising at least a highly-doped surface-adjointing zone (24a) of said second conductivity type adjacent said inner sidewall of said trench (16), an electrode (A) providing an electrical connection to said first device region (26), and an electrode (K) providing an electrical connection to said second device region (24a, 24b), said gate region (20) extending in a substantially vertical direction adjacent said second device region (24a, 24b) and said channel region (22), whereby a substantially vertical conduction channel is induced in the channel region (22) during operation.

3. A semiconductor device as claimed in claims 1 or 2, characterized in that said surface-adjointing second device region (24a, 24b) further comprises a highly-doped surface-adjointing zone (24b) of said first conductivity type adjoining the highly-doped surface-adjointing zone (24a) of said second conductivity type, spaced apart from said inner sidewall of said trench (16) by the surface-adjointing zone (24a) of said second conductivity type, and extending downwardly through a portion of said channel region (22).

4. A semiconductor device as claimed in claims 1 or 2, characterized in that said surface-adjointing channel region (22) extends laterally inward beyond said second device region (24a, 24b) for a distance which is about one-half a distance between said second device region (24a, 24b) and said first device region (26).

5. A semiconductor device as claimed in claims 1 or 2, characterized in that said surface-adjointing first device region (26) comprises a highly-doped zone of said first conductivity type.

6. A semiconductor device as claimed in claims 1 or 2, characterized in that said surface-adjointing first device region (26) comprises a Schottky diode.

**Patentansprüche**

1. Lateraler, bipolarer Halbleitertransistor (1) mit isolierter Steuerelektrode mit:

   einem Halbleitersubstrat (10) eines ersten Leitfähigkeitsstypes, welches eine Hauptoberfläche (12) aufweist,
   einer Halbleitersubstratschicht (14) eines zweiten Leitfähigkeitsstypes, das Gegenteil der des ersten Leitfähigkeitsstypes, welche auf der Hauptoberfläche (12) vorgesehen ist,
einem sich durch die Oberflächenschicht (14) erstreckenden Graben (16), welcher einen Teil der Oberflächenschicht (14) umschließt und dadurch eine Insel in der Oberflächenschicht (14) definiert, sowie eine Innenseitenwand, eine Außenseitenwand und eine Bodenfläche aufweist, wobei die Innenseitenwand die Insel begrenzt, einer die Seitenwände und die Bodenfläche des Grabens (16) bedeckenden, dielektrischen Schicht (18), einer Gatezone (20), welche in dem Graben auf der dielektrischen Schicht (18) angeordnet ist und ein leitfähiges Material aufweist, einer an die Oberfläche angrenzenden Kanalzone (22) des ersten Leitfähigkeitsarten, welche in der Insel der Oberflächenschicht (14) und in Angrenzung an die Innenseitenwand des Grabens (16) vorgesehen ist, einer an die Oberfläche angrenzenden, ersten Bauelementzone (26), welche in einem mittleren Teil der Insel der Oberflächenschicht (14) und von der Kanalzone (22) bestrahlt ist angeordnet ist, einer an die Oberfläche angrenzenden, zweiten Bauelementzone (24a, 24b), welche in der Kanalzone (22) angeordnet ist und in Angrenzung an die Innenseitenwand des Grabens (16) zumindest eine stark dotierte, an die Oberfläche angrenzende Zone (24a) des zweiten Leitfähigkeitsarten aufweist, einer Elektrode (A), welche eine elektrische Verbindung mit der ersten Bauelementzone (26) vorsieht, sowie einer Elektrode (K), welche eine elektrische Verbindung mit der zweiten Bauelementzone (24a, 24b) vorsieht, wobei sich die Gatezone (20) in im wesentlichen vertikalrichten Richtung in Angrenzung an die zweite Bauelementzone (24a, 24b) und die Kanalzone (22) erstreckt, wobei bei Betrieb ein im wesentlichen vertikalrichten Leitungskanal in der Kanalzone (22) induziert wird.

2. Lateraler, bipolärer Halbleitertransistor mit isolierter Steuerelektrode mit:

- einem Halbleitersubstrat (10) eines ersten Leitfähigkeitsarten, welches eine Hauptoberfläche (12) aufweist,
- einer Isolierschicht (13), welche auf der Hauptoberfläche (12) angenehrt ist,
- einer Halbleiteroberflächenschicht (14) eines zweiten Leitfähigkeitsarten, das Gegenpol der des ersten Leitfähigkeitsarten, welche auf der Isolierschicht (13) angeordnet ist, wobei es sich bei der Isolierschicht (13) um eine vergrabene Isolierschicht handelt,
- einem sich durch die gesamte Oberflächenschicht (14) erstreckenden Graben (16), welcher einen Teil der Oberflächenschicht (14) umschließt und dadurch eine Insel in der Oberflächenschicht (14) definiert, sowie eine Innenseitenwand, eine Außenseitenwand und eine Bodenfläche aufweist, wobei die Innenseitenwand die Insel begrenzt, einer die Seitenwände und die Bodenfläche des Grabens (16) bedeckenden, dielektrischen Schicht (18), einer Gatezone (20), welche in dem Graben auf der dielektrischen Schicht (18) vorgesehen ist und ein leitfähiges Material aufweist, einer an die Oberfläche angrenzenden Kanalzone (22) des ersten Leitfähigkeitsarten, welche in der Insel der Oberflächenschicht (14) und in Angrenzung an die Innenseitenwand des Grabens (16) vorgesehen ist, einer an die Oberfläche angrenzenden, ersten Bauelementzone (26), welche in einem mittleren Teil der Insel der Oberflächenschicht (14) und von der Kanalzone (22) bestrahlt ist angeordnet ist, einer an die Oberfläche angrenzenden, zweiten Bauelementzone (24a, 24b), welche in der Kanalzone (22) angeordnet ist und in Angrenzung an die Innenseitenwand des Grabens (16) zumindest eine stark dotierte, an die Oberfläche angrenzende Zone (24a) des zweiten Leitfähigkeitsarten aufweist, einer Elektrode (A), welche eine elektrische Verbindung mit der ersten Bauelementzone (26) vorsieht, sowie einer Elektrode (K), welche eine elektrische Verbindung mit der zweiten Bauelementzone (24a, 24b) vorsieht, wobei sich die Gatezone (20) in im wesentlichen vertikalrichten Richtung in Angrenzung an die zweite Bauelementzone (24a, 24b) und die Kanalzone (22) erstreckt, wobei bei Betrieb ein im wesentlichen vertikalrichten Leitungskanal in der Kanalzone (22) induziert wird.

3. Halbleiteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die an die Oberfläche angrenzende, zweite Bauelementzone (24a, 24b) ferner eine stark dotierte, an die Oberfläche angrenzende Zone (24b) des zweiten Leitfähigkeitsarten in Angrenzung an die stark dotierte, an die Oberfläche angrenzende Zone (24a) des zweiten Leitfähigkeitsarten aufweist, welche durch die an die Oberfläche angrenzende Zone (24a) des zweiten Leitfähigkeitsarten von der Innenseitenwand des Grabens (16) bestrahlt ist und sich nach unten durch einen Teil der Kanalzone (22) erstreckt.

4. Halbleiteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß sich die an die Ober-
flächen angrenzende Zone (22) jenseits der zweiten Baulementzone (24a, 24b) über eine Distanz, welche etwa halb so groß wie die Entfernung zwischen der zweiten Bauelementzone (24a, 24b) und der ersten Baulementzone (26) ist, lateral nach innen erstreckt.

5. Haibleiteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die an die Oberfläche angrenzende, erste Bauelementzone (26) eine stark dotierte Zone des ersten Leitfähigkeitstyps aufweist.

10. Haibleiteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die an die Oberfläche angrenzende, erste Bauelementzone (26) eine Schottky-Diode aufweist.

2. Transistor semiconducteur bipolaire latéral à grille isolée (1) comprenant

un substrat semiconducteur (10) d'un premier type de conductivité ayant une surface principale (12),
une couche de surface semiconductrice (14) d'un deuxième type de conductivité opposé au premier située sur ladite surface principale (12),
un sillon (16) s'étendant entièrement à travers ladite couche de surface (14) définissant ainsi un lôt dans ladite couche de surface (14) et présentant une paroi latérale interne, une paroi latérale externe et un fond, la paroi latérale interne délimitant ledit lôt,
une couche diélectrique (18) recouvrant les parois latérales et le fond dudit sillon (16),
une région de porte (20) située dans ledit sillon sur ladite couche diélectrique (18) et comprenant un matériau conducteur, une région de canal avoisinant la surface (22) dudit premier type de conductivité située dans ledit lôt de ladite couche de surface (14) et avoisinant ladite paroi latérale interne dudit sillon (16),
une première région de dispositif avoisinant la surface (26) située dans une partie centrale dudit lôt de ladite couche de surface (14) et espacée de ladite région de canal (22),
une deuxième région de dispositif avoisinant la surface (24a, 24b) située dans ladite région de canal (22) et comprenant au moins une zone avoisinant la surface fortement dopée (24a) dudit deuxième type de conductivité avoisinant ladite paroi latérale interne dudit sillon (16),
eine électrode (A) fournissant une connexion électrique à ladite première région de dispositif (26) et
une électrode (K) fournissant une connexion électrique à ladite deuxième région de dispositif (24a, 24b),
ladite région de porte (20) s'étendant dans une
direction pratiquement verticale avoisinant ladite deuxième région de dispositif (24a, 24b) et ladite région de canal (22), alors qu'un canal de conduction pratiquement vertical est induit dans la région de canal (22) pendant le fonctionnement.

3. Dispositif semiconducteur selon les revendications 1 ou 2, caractérisé en ce que ladite deuxième région de dispositif avoisinant la surface (24a, 24b) comprend en outre une zone avoisinant la surface fortement dopée (24b) dudit premier type de conductivité avoisinant la surface fortement dopée (24a) du deuxième type de conductivité, espacée de ladite paroi latérale interne dudit sillon (16) par la zone avoisinant la surface (24a) dudit deuxième type de conductivité et s'étendant à travers une partie de ladite région de canal (22).

4. Dispositif semiconducteur selon la revendication 1 ou 2, caractérisé en ce que ladite région de canal avoisinant la surface (22) s'étend latéralement vers l'intérieur au-delà de ladite deuxième région de dispositif (24a, 24b) sur une distance égale à environ la moitié de la distance comprise entre ladite deuxième région de dispositif (24a, 24b) et ladite première région de dispositif (26).

5. Dispositif semiconducteur selon les revendications 1 ou 2, caractérisé en ce que ladite première région de dispositif avoisinant la surface (26) comprend une zone fortement dopée dudit premier type de conductivité.

6. Dispositif semiconducteur selon les revendications 1 ou 2, caractérisé en ce que ladite première région de dispositif avoisinant la surface (26) comprend une diode Schottky.