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(54) Circuit for reliable switching over of signal processing circuits
Schaltung zur zuverlässigen Umschaltung von signalverarbeitenden Schaltungen
Circuit de commutation fiable des circuits de traitement des signaux

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(56) References cited:
US-A- 4 377 861
US-A- 4 837 760

• NEC RESEARCH AND DEVELOPMENT. no. 94, July 1989, TOKYO JP pages 129 - 135 S.
MIYAZAWA ET AL. 'Multiprocessing System Provided with Fail-Soft Operation Function'
• INTERNATIONAL SWITCHING SYMPOSIUM 1976 25 October 1976, KYOTO, JP pages 212-4-1
• - 212-4-6 M. KARNAUGH 'DESIGN CONSIDERATIONS FOR A DIGITAL SWITCH'
• PROCEEDINGS OF THE IEEE vol. 65, no. 9, September 1977, NEW YORK US pages 1363 - 1374 S.R. TREVES 'Maintenance Strategies for PCM Circuit Switching'

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Description

The present invention relates to circuitry incorporated in a system including a plurality of signal processing circuits having an identical function for switching them over. A system including a plurality of signal processing circuits having an identical function additionally includes a standby signal processing circuit. When any one of the active signal processing circuits fails, it is replaced by the standby signal processing circuit to ensure the reliability of the system. However, this kind of system is totally shut down when the standby signal processing circuit substituting the failed circuit fails itself. While a number of standby circuits may be incorporated in the system to cope with the above occurrence, such an approach is not desirable from the cost standpoint since standby circuits are simply useless so long as the other circuits are normal.

NEC Research and Development No. 94, July 1989, Tokyo, Japan pages 129-135 discloses a multiprocessor system including a plurality of processing devices for processing a plurality of software. When any one of the processing devices fails, the other or normal processing devices deal with the signal having been processed by the failed processing device, the software that is not important is not processed.

United States Patents No. US-A-4,857,760 (REID et al.) discloses circuitry having a plurality of processing circuits for processing a plurality of time slots constituting a TDMA signal, and a standby or spare processing circuit. When an error occurs in any one of the former circuits, the latter circuit or standby circuit processes the signal having been handled by the defective circuit.

In accordance with the present invention, circuitry for switching signal processing circuits comprises n signal processing circuits each receiving an input signal having n time division multiplexed signals to thereby output a result of processing as a data signal, a selector for generating a switching signal in response to n alarm signals each being generated by respective one of the n signal processing circuits when associated one of the signal processing circuits fails, and a controller receiving a timing signal representative of a relation between the switching signal and the input signal for switching over timings at which the n signal processing circuits should process the input signal, characterised in that when a processing circuit dealing with an important time slot fails, the selector is adapted to deliver the switching signal to the controller, causing the controller to hand over the processing of the important time slot to any one of the other, normal signal processing circuits, in place of the failed circuit, in accordance with the switching signal.

Also, in accordance with the present invention, a method of switching n signal processing circuits each receiving an input signal made up of n signal processing circuits each receiving an input signal made up of n time division multiplexed signals to thereby produce a result of processing as a data signal comprises the steps of causing each of the n signal processing circuits to generate an alarm signal when failed, generating a switching signal by means of a selector in response to the alarm signal, feeding a timing signal representative of a relation between the switching signal and the input signal, and switching timings for particular ones of the n signal processing circuits to process the input signal, characterised in that when a processing circuit dealing with an important time slot fails, the selector delivers the switching signal to the controller causing the controller to hand over the processing of the important time slot to any one of the other, normal signal processing circuits, in place of the failed circuit, in accordance with the switching signal.

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description taken with the accompanying drawings in which:

Figure 1 is a block diagram schematically showing conventional circuitry for switching signal processing circuits;

Figures 2A-2D are timing charts demonstrating a specific operation of the conventional switching circuitry;

Figure 3 is a schematic block diagram showing circuitry for switching signal processing circuits embodying the present invention; and

Figures 4A-4D are timing charts representative of a specific operation of the embodiment.

To better understand the present invention, a brief reference will be made to conventional switching circuitry incorporated in a TDMA (Time Division Multiple Access) receiver by way of example, shown in Figure 1. As shown, the switching circuitry has n signal processing circuits 21-2n, a standby circuit 10, and a switching circuit 11. The n signal processing circuits 21-2n receive an input signal 1 made up of n time division multiplexed signals and produce data signals 31 - 3n, respectively. The standby circuit 10 is connected in parallel with the signal processing circuit 21 for producing a data signal 31 in response to the input signal 1. The switching circuit 11 selectively switches over the signal processing circuit 21 and standby circuit 10 with control signals 121 and 122. The input signal 1 is made up of n time slots, i.e., a time slot including system information and similar signals of primary importance for the system (referred to as an important time slot hereinafter) and time slots for handling general signals (referred to as general time slots hereinafter). The important time slot is assigned to the signal processing circuit 21 while the general time slots are each assigned to particular one of the signal processing circuits 22-2n. In response to a timing signal
shown in FIG. 2B and included in the input signal 1, the signal processing circuits 21-2n each processes the associated time slot, as shown in FIG. 2C. When the signal processing circuit 21 assigned to the important time slot fails, the switching circuit 11 delivers the control signals 121 and 122 to replace the signal processing circuit 21 with the standby circuit 10. As a result, as shown in FIG. 2D, the standby circuit 10 handles the important time slot afterwards to thereby insure the reliability of the system.

However, the problem with the conventional switching circuitry is that once the standby circuit 10 fails itself, the circuitry cannot deal with the important time slot at all, resulting in total system down. While this problem may be eliminated if a number of standby circuits are used, such an implementation is not desirable from the economy standpoint since the standby circuits are simply useless so long as the signal processing circuit are free from errors.

Referring to FIG. 3, circuitry for switching signal processing circuits embodying the present invention is shown. As shown, n signal processing circuits 21-2n output respectively data signals 31-3n in response to an input signal 1 having n signals including an important time slot and general time slots multiplexed on a time division basis. A controller 5 is connected to the signal processing circuits 21-2n and receives a timing signal 4 representative of a relation of the multiplexed input signal 1 with respect to time. The controller 5 delivers control signals 61-6n to the signal processing circuits 21-2n, respectively. The signal processing circuits 21-2n deliver respective alarm signals 71-7n to a selector 8. The selector 8 feeds a switching signal 9 matching the alarm signals 71-7n to the controller 5. The selector 8 constantly determines which of the signal processing circuits 21-2n is handling the important time slot, and it assigns the important time slot to normal one of the signal processing circuits 21-2n prior to the general time slots.

A reference will be made to FIGS. 4A-4D for describing a specific operation of the embodiment. As shown in FIG. 4A, the input signal 1 has an important time slot and general time slots multiplexed on a time division basis. The controller 5 sequentially switches the signal processing circuits 21-2n and corresponding to the input signal 1. Assume that the time slot No. 0 is the important time slot and is handled by the signal processing circuit 21, as shown in FIG. 4C. Then, as the signal processing circuit 21 fails, the circuit 21 sends an alarm signal 71 to the selector 8. In response, the selector 8 determines that the signal processing circuit 21 is handling the important time slot, while determining whether or not the other signal processing circuits are normal. Then, the selector 8 delivers a switching signal 9 to the controller 5 for causing the controller 5 to replace the processing timing of the failed signal processing circuit 21 with that of any one of the normal signal processing circuits. On receiving the switching signal 9, the controller 5 shuts down the signal processing circuit 21 represented by the alarm signal 71. At the same time, the controller 5 replaces the signal processing circuit 21 with one of the other signal processing circuits dealing with the general time slots, e.g., the signal processing circuit 22 by changing the timings for generating the control signals 61 and 62. As a result, the important time slot No. 0 is handed over to the signal processing circuit 22 afterwards.

If the signal processing circuit to handle the important time slot is sequentially replaced in the above-described manner, an occurrence that the processing of the important time slot is practically interrupted due to a failure of a signal processing circuit is almost eliminated. This is successful in preventing the whole system from being disabled.

In summary, it will be seen that the present invention provides switching circuitry including a selector and a controller which replaces, in response to alarm signals from individual signal processing circuits, the processing timing of a failed signal processing circuit with that of another signal processing circuit. Hence, the circuitry guarantees the processing of an important time slot until all the signal processing circuits fail, reducing the system down rate and thereby enhancing the reliability of the system. The circuitry of the invention will be especially desirable when the system is situated at a location too remote to effect immediate maintenance in the event of failure.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

Claims

1. Circuitry for switching signal processing circuits, comprising:

- n signal processing circuits (21-2n) each receiving an input signal (1) having n time division multiplexed signals to thereby output a result of processing as a data signal;
- a selector (8) for generating a switching signal (9) in response to n alarm signals each being generated by respective one of said n signal processing circuits when associated one of said signal processing circuits fails; and
- a controller (5) receiving a timing signal (4) representative of a relation between the switching signal and the input signal for switching over timings at which said n signal processing circuits should process the input signal, characterised in that when a processing circuit dealing with an important time slot fails, the selector is adapted to deliver the switching signal to the controller, causing the controller to hand over
the processing of the important time slot to any one of the other, normal signal processing circuits, in place of the failed circuit, in accordance with the switching signal.

2. Circuit as claimed in Claim 1, wherein said selector is adapted to constantly determine which one of said n signal processing circuits is handling a particular time slot of the input signal which includes important information and replacing on receiving the alarm signal from the one signal processing circuit, processing timing of said one signal processing circuit with processing timing of one of the other signal processing circuits which are normal.

3. A method of switching n signal processing circuits (21-2n) each receiving an input signal (1) made up of n time division multiplexed signals to thereby produce a result of processing as a data signal, said method comprising the steps of:

(a) causing each of said n signal processing circuits to generate an alarm signal (71-7n) when failed;
(b) generating a switching signal (9) by means of a selector (5) in response to the alarm signal;
(c) feeding to a controller (5) a timing signal (4) representative of a relation between the switching signal and the input signal, and
(d) switching timings for particular ones of said n signal processing circuits to process the input signal characterised in that when a processing circuit dealing with an important time slot fails, the selector delivers the switching signal to the controller, causing the controller to hand over the processing of the important time slot to any one of the other, normal signal processing circuits, in place of the failed circuit, in accordance with the switching signal.

4. A method as claimed in Claim 3, wherein step (b) comprises determining which of said n signal processing circuits is handling a particular time slot of the input signal which includes important information, and generating, on receiving the alarm signal from the signal processing circuit handling the particular time slot, the switching signal for replacing a processing timing of said signal processing circuit with processing timing of another signal processing circuit which is normal.

Patentansprüche

1. Schaltung zum Umschalten von signalverarbeitenden Schaltungen, welche aufweist:

n signalverarbeitende Schaltungen (21-2n), die jeweils ein Eingangssignal (1) mit n Zeitmultiplexsignalen empfangen, um dadurch ein Verarbeitungsergebnis als Datensignal auszugeben;

2. Schaltung nach Anspruch 1, wobei der Wähler so angepaßt ist, daß er ständig feststellt, welche von den n signalverarbeitenden Schaltungen gerade einen bestimmten Zeitschlit des Eingangssignals bearbeitet, der eine wichtige Information aufweist, und bei Empfang des Alarmsignals von der einen signalverarbeitenden Schaltung den Verarbeitungszeitpunkt der einen signalverarbeitenden Schaltung durch den Verarbeitungszeitpunkt einer der anderen, normalen signalverarbeitenden Schaltungen ersetzt.

3. Verfahren zum Umschalten von n signalverarbeitenden Schaltungen (21-2n), die jeweils ein aus n Zeitmultiplexsignalen bestehendes Eingangssignal (1) empfangen, um dadurch ein Verarbeitungsergebnis als Datensignal zu erzeugen, wobei das Verfahren die folgenden Schritte aufweist:

(a) Veranlassen, daß jede der n signalverarbeitenden Schaltungen, wenn sie ausfällt, ein Alarmsignal (71-7n) erzeugt;
(b) Erzeugen eines Umschaltsignals (9) mit Hilfe eines Wählers (8) als Reaktion auf das Alarmsignal;
(c) Einspeisen eines Zeitaktionssignals (4), das eine Beziehung zwischen dem Umschaltsignal und dem Eingangssignal darstellt, in eine Steuereinrichtung (5); und
(d) Umschalten von Zeitpunkten für bestimmte
von den n signalverarbeitenden Schaltungen zur Verarbeitung des Eingangssignals, dadurch gekennzeichnet, daß beim Ausfall einer Verarbeitungsschaltung, die einen wichtigen Zeitschutz bearbeitet, der Wähler des Um- schaltsignals an die Steuereinrichtung abgibt, wobei die Steuereinrichtung dazu dient, entsprechend dem Umschaltsignal die Verarbeitung des wichtigen Zeitschitzes anstelle der ausgefallenen Schaltung einer der anderen, normalen signalverarbeitenden Schaltungen zu übergeben.


Revendications

1. Circuiterie pour commuter des circuits de traitement de signal, comprenant :
   - n circuits de traitement de signal (21-2n), chacun recevant un signal d'entrée (1) ayant n signaux multiplexés en temps partagé de manière à sortir un résultat de traitement en tant que signal de données;
   - un sélecteur (8) pour générer un signal de commutation (9) en réponse à n signaux d'alerte, chacun étant généré par un circuit respectif desdits n circuits de traitement de signal lorsqu'un circuit associé desdits circuits de traitement de signal tombe en panne; et
   - une unité de commande (5) recevant un signal de rythme (4) représentatif d'une relation entre le signal de commutation et le signal d'entrée pour commuter des rythmes auxquels lesdits n circuits de traitement de signal doivent traiter le signal d'entrée,

   caractérisée en ce que lorsqu'un circuit de traitement s'occupant d'une tranche de temps importante tombe en panne, le sélecteur est adapté à délivrer le signal de commutation à l'unité de commande, faisant en sorte que l'unité de commande remet le traitement de la tranche de temps importante à n'importe lequel des autres circuits normaux de traitement de signal, au lieu du circuit en panne, conformément au signal de commutation.

2. Circuit selon la revendication 1, dans lequel ledit sélecteur est adapté à déterminer constamment lequel desdits n circuits de traitement de signal gère une tranche de temps particulière du signal d'entrée qui comporte des informations importantes et remplaçant, à la réception du signal d'alerte provenant de ce circuit de traitement de signal, le rythme de traitement dudit circuit de traitement de signal par le rythme de traitement d'un autre des circuits de traitement de signal qui sont normaux.

3. Procédé de commutation de n circuits de traitement de signal (21-2n), chacun recevant un signal d'entrée (1) composé de n signaux multiplexés en temps partagé de manière à produire un résultat de traitement en tant que signal de données, le dit procédé comprenant les étapes de :
   (a) génération, par chacun desdits n circuits de traitement de signal, d'un signal d'alerte (71-7n) lors d'une panne;
   (b) génération d'un signal de commutation (9) au moyen d'un sélecteur (8) en réponse au signal d'alerte;
   (c) fourniture, à une unité de commande (5), d'un signal de rythme (4) représentatif d'une relation entre le signal de commutation et le signal d'entrée; et
   (d) commutation de rythmes pour des circuits particuliers desdits n circuits de traitement de signal pour traiter le signal d'entrée, caractérisé en ce que lorsqu'un circuit de traitement s'occupant d'une tranche de temps importante tombe en panne, le sélecteur délivre le signal de commutation à l'unité de commande, utilisant l'unité de commande pour remettre le traitement de la tranche de temps importante à n'importe lequel des autres circuits normaux de traitement de signal, au lieu du circuit en panne, conformément au signal de commutation.

4. Procédé selon la revendication 3, dans lequel l'étape (b) comprend la détermination du circuit desdits n circuits de traitement de signal qui gère une tranche de temps particulière du signal d'entrée qui comporte des informations importantes et la génération, à la réception du signal d'alerte provenant du circuit de traitement de signal gérant la tranche de temps particulière, du signal de commutation pour remplacer un rythme de traitement dudit circuit de traitement de signal par le rythme de traitement d'un autre circuit de traitement de signal qui est normal.