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(54) Video coder/decoder with shift prevention for correctly decoded signal blocks

Videokodierer und -dekodierer mit Verschiebungsverhinderung für korrekt dekodierte Signalblöcke
Codeur/décodeur de vidéo avec prévention de déplacement pour les blocs de signal correctement décodés

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• ICASSP 88 Vol. II Multidimensional Signal
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resilience of a video codec for low bitrates"

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Description

The present invention relates to digital video signal processing for recording or other transmissions and, more particularly, to receivers or monitors wherein loss of synchronization causes shifting of parts of the image generated by otherwise correctly decoded video signals.

Digital coding techniques are used to reduce the amount of data for storage and/or other types of transmission of digitized video information signals. Transform coding and variable word-length coding are among well-known techniques to obtain efficient data compression. These techniques are often combined.

Loss of synchronization is a key problem in variable word-length decoding of compressed data. In the case of transformed images that are coded with variable word-length codes, many pixel blocks may pass before re-synchronization takes place. Even after a return to synchronization, it may not be possible to put the correctly decoded data in the proper position in the picture. There is thus a distortion of the decoded picture due to a shift of data. This is shown in Fig. 1, where the top and bottom parts of a tree are clearly misaligned.

A known apparatus for encoding video signals is disclosed in G. Aartsen et al: Error resilience of a video codec for low bitrates, published in ICASSP 88, Volume II, Multidimensional Signal Processing, April 11-14, 1988, New York City, USA. The known apparatus comprises first means for generating video image signals and for dividing the image signals into image signal blocks, coding means for coding the image signal blocks in a coded data stream including block codes signifying the presence of each image signal block, and grouping means connected to the coding means for grouping the coded data stream into data groups each having a preselected number of block codes, and for separating sequential data groups by synchronization signals. Loss of a block code can thus be determined.

It is an object of the present invention to provide means for inserting the synchronization signals. It is a further object of the invention to provide a decoder apparatus for decoding the coded data stream.

According to the invention, the apparatus is characterized in that the block codes are end-of-block (EOB) signals signifying the end of each image signal block, and in that the grouping means comprises separator means for separating the end-of-block signals from the coded data stream, first counting means connected to the end-of-block separator means for counting the end-of-block signals and generating a first counting signal signifying a count of \( n \) thereof, and means connected to the first counting means for generating the synchronization signals and inserting each synchronization signal into the coded data stream in response to the first counting signal.

The decoder apparatus is characterized by EOB counting means for counting the end-of-block signals between sequential ones of the synchronization signals and furnishing a missing EOB signal when the so-counted number is less than \( n \), and insertion means are connected to the EOB counting means to insert the missing number of end-of-block signals into the decoded data stream in response to said missing EOB signal. Herewith is achieved that a received encoded data stream is regenerated into a "compliant" data stream, i.e. an encoded data stream comprising the correct number of end-of-block signals in each data group. The subsequent decoder receiving said compliant data stream does not need to take account for missing EOB's. The decoder is thus simple and cost-effective, and yet automatically correctly positions the image blocks relative to one another even upon loss of an end-of-block signal.

Additional advantages and details of the present invention will become clear in light of the following description taken into conjunction with the drawings.

Figure 1 illustrates the shifting of one part of a correctly decoded image.

Figures 2, 3 and 4 illustrate in block diagram form possible interconnections of the end-of-block signal inserter according to the present invention with a variable word-length decoding system.

Figure 5 is a block diagram of the end-of-block inserter of the present invention, and

Figure 6 is a simplified block diagram of the coder of the present invention.

In a particular embodiment of a variable word-length coding-decoding system in which the present invention is applicable, the picture is divided into small two dimensional blocks which are coded sequentially. In the first step each block is transformed using the discrete cosine transform.

Thereafter, the transformed signal is quantized and variable length coded. This is described, for example, in Chen & Pratt, "Scene Adaptive Coder", IEEE Trans. on Comm., Vol. COM-32, pp. 225-232, March 1984 and in De With & Borgers, "On adaptive DCT coding techniques for digital video recording", IERE Proceedings of 7th Int. Conf. on Video, Audio & Data Recording, York (UK), March 1986, pp. 199-204. This encoding results in a bit stream which is a multiplex of amplitude and address words followed by an end-of-block (EOB) word which is an indication for the decoder that the following data belongs to the next block. In the variable word-length coder, data words with the associated EOB words are mapped to variable word-length code words. This coding scheme is used illustratively only. Application of the present invention is in no way limited thereto.

According to the present invention, the coded sequence per field or frame is divided into data groups of \( n \) blocks. This division can be accomplished in a variety of ways. At one extreme, \( n=2 \), and each end-of-block signal has an additional bit which is alternately "1" and "0". When \( n \) is larger than 2, more bits could be used
to indicate the specific position of a block in the group. However, it is only necessary to distinguish the last end-of-block signal in a group from the others. Thus a single additional bit per end-of-block word could suffice even for larger groups.

In a preferred embodiment, however, a synchronization signal or word is inserted in the data stream instead of, or after, the nth end-of-block signal. The latter embodiment will be described in detail below. Various modifications, including those mentioned above, can then be readily implemented by one skilled in the art.

For the embodiment using a synchronization signal after all end-of-block signals, the coded sequence has the following format:

\[ k \times (\text{SYNC} + n \{ \text{mi(word)} + \text{EOB} \} ) \]

where:

\[ \text{mi} = \text{number of data words in block i}, \]
\[ n = \text{number of blocks (EOB's) between two synchronization words}, \]
\[ \text{SYNC} = \text{synchronization word}, \]
\[ k = \text{number of synchronization words in a picture}. \]

It will be noted that the only additional words within the sequence are the synchronization words.

At the decoder, synchronization loss leads to information loss for an unknown amount of data, namely until the next synchronization word is recognized. The information loss may well cover several coded blocks so that a number of EOB words are missing. This results in two kinds of distortion. Channel errors may perturb the data, causing erroneous decoding of blocks which, in turn, results in a "noisy" part of the picture. This type of distortion is not addressed by the present invention. It will last until synchronization is re-established. The second kind of distortion consists of correctly decoded blocks which, after loss of synchronization, are shifted relative to the remainder of the image since their correct location cannot be determined because of the missing EOB words. This shift is extremely disturbing and can be avoided in a majority of the cases with the means of the present invention.

One way to prevent the shift of correctly decoded data is to make use of the above-mentioned synchronization words or signals. The number of EOB words between two synchronization words is known in advance, so that by counting the number of received EOB words, it is possible to insert the missing number of these words at the time the next synchronization word is decoded. This will allow correct positioning of the decoded blocks without modification of rest of decoder.

The above-mentioned solution works only if the synchronization words themselves are free of error. Since this is not necessarily the case, their resistance to such error may be improved by adding an identification to some or all of them. For example, the identification may be a modulo n counting value. The probability that k adjacent synchronization words will be distorted is significantly smaller than an error occurring in one synchronization word, even when k equals unity.

For example, if n is the number of EOB's between two synchronization words, the counter is a modulo-2 counter, and p EOB words are counted between two synchronization words both having identification 0, then the number of EOB words to be inserted is 2^n-p.

The EOB inserter of the present invention can be interconnected with the variable length decoder and the buffer memory of the conventional decoder configuration in a number of ways. Three possibilities are mentioned here.

For the first possibility, the EOB inserter 12 is connected between a variable word-length decoder (VLD) 10 and a buffer memory (MEM) 14. This is illustrated in Fig. 2. Specifically, received data is decoded in VLD 10. Output lines a, b and c of VLD 10 carry, respectively, "data valid" (DV) signals or words, data, and, on line c, synchronization and EOB words, each with associated identification signals, if any.

The data output on line b is directly applied to MEM 14. The "data valid" words on line a are combined with similar words on a line a' at the output of EOB inserter 12 in an OR-gate 13. The output of OR-gate 13 is also connected to MEM 14, to verify that data should be entered. Finally, the synchronization and EOB words decoded in VLD 10 are applied to EOB inserter 12 where they are processed as described with reference to Fig. 5 below. EOB words on output line c' of EOB inserter 12 are applied directly to MEM 14. In this system, the number of EOB's which can be inserted is limited since the variable length decoder (VLD) must decode the data from the channel in real time (fixed input rate). The only time window available for insertion of the EOB words is thus during reception of the synchronization word and the following identification bits. Therefore the maximum number of end-of-block words which may be inserted depends on the length of the synchronization word.

In the arrangement shown in Fig. 3, EOB inserter 12 is located after variable length decoder 10 and buffer memory 14', the latter two being connected in cascade in the order mentioned. Here, the number of EOB words which can be inserted is almost unlimited since the buffer holds all the decoder data before insertion. However, a larger buffer memory is required than in the system illustrated in Fig. 2, since the control inputs to the EOB inserter (see Fig. 6) must be stored.

The arrangement illustrated in Fig. 4 is the same as that illustrated in Fig. 3, except that the position of buffer memory 14" and variable length decoder 10 has been reversed. Here, buffer memory 14" is organized for a serial output and variable length decoder 10 runs at a fixed output rate. In this system, the number of EOB words which can be inserted is almost unlimited, but a complex control is required.

It is to be noted in Fig. 4 that data request signals may be transmitted directly to buffer memory 14, or via
the variable length decoder 10.

Similarly, data request signals in Fig. 3 may pass through or bypass EOB 12, as may data and "data valid" signals in Fig. 2.

Figure 5 is a more detailed diagram of the EOB inserter itself. The basic blocks illustrated in Fig. 5 are two counters. The first is an EOB word counter 20, the second is a synchronization signal counter 22. Also shown is a control block 24. The circuit of Fig. 5 receives the following signals from the variable word-length decoder 10 or memory 14. First, a signal "EOBR" (EOB received) at a terminal 26, a signal SR (synchronization signal received) at a terminal 28 and the sync identification signal (sync ID) at a terminal 30. The signal from terminal 30 is applied to one input of a comparator 32 whose other input receives the count output of counter 22. The count in counter 22 is advanced by the output of an OR-gate 34 which has a first input receiving the signal from terminal 28 and a second input receiving a signal from a control output line 36 of control unit 24.

Counter 20 has a count down input 38 which is connected to the output of an OR-gate 40. OR-gate 40 receives the EOB signal on line 26 at a first input and a signal from the output of an AND-gate 42 at a second input. The first input of AND-gate 42 receives a clock signal, while the second input receives a signal on an output line 44 of control block 24. An output 46 of control block 24 is connected to a further input PR of end-of-block counter 20. The latter has an output which is connected to an input of control block 24. The main output of control block 24 appears on a line 50, which is connected to an output buffer 52.

The EOB inserter described above works as follows:

control block 24 recognizes four different situations upon receipt of a synchronization word.

First, EOB counter 20 has counted to zero and comparator 32 indicates that the synchronization identification signal on line 30 corresponds to the output of counter 22. Under these conditions, the system is operating correctly and the signal on line 46 causes counter 20 to be set to the number n of EOB word which will precede the next synchronization signal.

Under the second condition, comparator 32 signals that the synchronization identification on line 30 corresponds to the output of counter 22, but counter 20 is not at zero. This causes a "1" to appear on line 44 and, therefore, at the output of AND-gate 42 upon receipt of the next clock signal. OR-gate 40 will then furnish an output which causes counter 20 to count down one step. In every clock period, output buffer 52 is enabled by control block 24 via line 50. Another end-of-block word is thereby inserted on the data bus under control of a "data valid" signal on line 50. When the countdown on counter 20 reaches zero, condition 1 exists and decoding of the following n variable word-length blocks begins. The clock rate must be sufficiently high that the counter has finished counting down before the next end-of-block word is received.

The third possibility is that counter 20 is at zero, but that comparator 32 signals that the output of counter 22 does not match the synchronization identification word received on line 30. Under these conditions, control block 24 outputs a signal on line 36 which, via OR-gate 34, causes the count on counter 22 to be raised by 1. Simultaneously, control block 24 resets counter 20 to the number of EOB words (n) between synchronization signals via a signal on line 46. Control block 24 then outputs a signal on line 44 to start counting down on counter 20. During each counting down step, an EOB word is transferred from buffer 52 to the data bus. If comparator 32 does not indicate equality at its two inputs after the above-mentioned increase of one count on counter 22, counter 20 is reset to n after it has reached zero, and the next n EOB words are inserted on the data bus. As soon as comparator 32 indicates coincidence at its two inputs, EOB counter 20 is reset to n and decoding of the following variable word-length block begins.

Finally, if end-of-block counter 20 is not at zero and the synchronization identification word received on line 30 does not match the count on counter 22, control block 24 first causes a count-down on counter 20 with transfer of an EOB word from buffer 52 to the data bus for each count. When counter 20 reaches a count of zero, the system operates as described under the third possibility above.

The present invention has been described with reference to a specific embodiment of an end-of-block inserter interconnected with the variable word-length decoder and its associated memory as indicated in Fig. 3. Here it must be repeated that the end-of-block signal from buffer memory 52 has to be synchronized with the outgoing data stream, i.e. the output of buffer 52 is applied, for example, to a multiplexer which also receives the data signals (the EOB signals from buffer 52 being inserted only in the event of an error as described above).

Figure 6 is a simplified diagram of the transmitter or encoding circuitry required for implementing the present invention. A block 60 includes the scanning and division into two-dimensional blocks each having an associated address and end-of-block signal. These signals are subjected to a discrete cosine transform in a stage 62. The output of stage 62 is quantized and subject to variable word-length coding in stage 64. The output of stage 64 is thus a coded stream of amplitude and address words followed by end-of-block words. The end-of-block words are extracted in stage 66. They are counted in a counter 68 which, at a predetermined count, furnishes a signal to the synchronization signal generation stage 70. An output from stage 70 causes the reset of counter 68 and an input to a counter 72 which preferably is a modulo n counter as mentioned above. The output of counter 72 is the synchronization identification signal. This, as well as the synchronization signals as such and the out-
put of stage 64 are applied to a multiplexer 74 whose output is the signal which is to be recorded or otherwise transmitted. It should also be noted that many variations of the particular embodiment illustrated in Fig. 6 are possible. For example, an identification scheme such as the one illustrated for the synchronization signal could be applied to the end-of-block signals as described above, or in addition to its application to the synchronization signals. The latter would obviate the necessity for counting down on counter 20. Other variations and changes are also possible, will be readily apparent to one skilled in the art and are intended to be encompassed in the following Claims.

Claims

1. Apparatus having first means (60) for generating video image signals and for dividing the image signals into image signal blocks, coding means (62, 64) for coding the image signal blocks into a coded data stream including block codes signifying the presence of each image signal block, and grouping means (66-74) connected to the coding means for grouping the coded data stream into data groups each having a presel ected number of block codes, and for separating sequential data groups by synchronization signals, characterized in that the block codes are end-of-block EOB signals signifying the end of each image signal block, and in that the grouping means comprises separator means (66) for separating the end-of-block signals from the coded data stream, first counting means (68) connected to the end-of-block separator means for counting the end-of-block signals and generating a first counting signal signifying a count of n thereof, and means (70, 74) connected to the first counting means for generating the synchronization signals and inserting each synchronization signal into the coded data stream in response to the first counting signal.

2. Apparatus as claimed in Claim 1, further characterized in that second counting means (72) count the synchronization signals and furnish identification signals corresponding to the number of so-counted synchronization signals, and further characterized in that an identification signal is inserted into the coded data stream with at least selected ones of the synchronization signals.

3. Apparatus as claimed in Claims 1 or 2, further characterized in that decoding means receive the coded data stream and furnish a decoded data stream grouped/divided into the data groups in response thereto, third counting means (20, 24) are coupled to the decoding means for counting the end-of-block signals between sequential ones of the synchronization signals furnishing a missing EOB signal when the so-counted number is less than n, and insertion means (52) are connected to the third counting means for inserting at least one end-of-block signal in the decoded data stream in response to the missing EOB signal.

4. Apparatus as claimed in Claim 1, wherein at least one of the end-of-block signals in a group is assigned a code word different from the others so as to constitute the synchronization signal.

5. Decoding apparatus for receiving a coded data stream comprising video image signals grouped into image signal blocks each having an end-of-block signal EOB, a plurality n of the image signal blocks constituting a data group, sequential data groups being separated by synchronization signals, characterized by EOB counting means for (20, 24) counting the end-of-block signals between sequential ones of the synchronization signals and furnishing a missing EOB signal when the so-counted number is less than n, and insertion means (52) connected to the EOB counting means for inserting the missing number of end-of-block signals into the decoded data stream in response to said missing EOB signal.

6. Decoding apparatus as claimed in Claim 5, further characterized in that the coded data stream further comprises sync identification signals distinguishing at least selected ones of the synchronization signals from at least the respective next following synchronization signals, and further comprising means for separating the sync identification signals from the coded data stream.

7. Decoding apparatus as claimed in Claim 6, further comprising means (22) for generating a local sync identification signal in response to received synchronization signals, and comparator means connected to the local sync identification signal generating means for comparing the local sync identification signal to the received sync identification signal and generating a comparator output signal only upon agreement therebetween.

8. Decoding apparatus as claimed in Claim 7, further characterized in that the insertion means insert n end-of-block signals into the decoded data stream in the absence of a comparator output signal following receipt of a synchronization signal.

Patentansprüche

1. Anordnung mit ersten Mitteln (60) zum Erzeugen von Video-Bildsignalen und zum Aufteilen der Bild-
signale in Bildsignalblöcke, mit Codierungsmitteln (62, 64) zum Codieren der Bildsignalblöcke zu einem codierten Datenstrom mit Blockcodes, die das Vorhandensein jedes Bildsignalblocks bezeichnen, und mit Gruppierungsmitteln (66-74), die mit den Codierungsmitteln verbunden sind, zum Gruppieren des codierten Datenstroms in Datengruppen, die je eine vorexplizierte Anzahl von n Blockcodes aufweisen, und zum Trennen sequentieller Daten- gruppen durch Synchronsignale, dadurch gekennzeichnet, daß die Blockcodes Ende-des-Blocks-Signale sind, die das Ende jedes Bildsignalblocks bezeichnen, und daß die Gruppierungsmittel Trennmittel (66) aufweisen zum Trennen der Ende-des-Blocks-Signale von dem codierten Datenstrom, wobei erste Zählmittel (68) mit den Ende-des-Blocks-Trennmittel verbunden sind zum Zählen der Ende-des-Blocks-Signale und zum Erzeugen eines ersten Zählsignals, das eine Zählung von n derselben bezeichnet, und Mittel (70, 74), die mit den ersten Zählmitteln verbunden sind zum Erzeugen der Synchronsignale und zum Einfügen jedes Synchronsignals in den codierten Datenstrom in Antwort auf das erste Zählsignal.

2. Anordnung nach Anspruch 1, weiterhin dadurch gekennzeichnet, daß zweite Zählmittel (72) die Synchronsignale zählen und Kennsignale liefern, die der Anzahl der auf diese Weise gezählten Synchronsignale entspricht, und weiterhin dadurch gekennzeichnet, daß in den codierten Datenstrom mit wenigstens selektierten Signalen der Synchronsignale ein Kennsignal eingefügt wird.

3. Anordnung nach Anspruch 1 oder 2, weiterhin dadurch gekennzeichnet, daß Decodemittel den codierten Datenstrom erhalten und einen decodierten Datenstrom in die datengruppen in Antwort darauf gruppiert und aufgeteilter liefern, daß Zählmittel (20, 24) mit den Decodemitteln gekoppelt sind zum Zählen von Ende-des-Blocks-Signalen zwischen sequentiellen Signalen der Synchronsignale, was ein fehlerloses Ende-des-Blocks-Signal ergibt, wenn die auf diese Weise gezählte Anzahl kleiner als n ist, und daß Einfügungsmittel (52) mit den dritten Zählmitteln gekoppelt sind zum Einfügen wenigstens eines Ende-des-Blocks-Signals in den decodierten Datenstrom in Antwort auf das fehlende Ende-des-Blocks-Signals.


7. Decodieranordnung nach Anspruch 6, weiterhin mit Mitteln (22) zum Erzeugen eines örtlichen Synchronkennsignals in Antwort auf empfangene Synchronsignale und mit Vergleichsmitteln, die mit den örtlichen Synchronkennsignalverarbeitungsmitteln verbunden sind zum Vergleichen des örtlichen Synchronkennsignals mit dem empfangenen Synchronkennsignal und zum Erzeugen eines Vergleichsanordnungsausgangssignals nur bei Übereinstimmung zwischen denselben.


Reivendications

1. Appareil comportant des premiers moyens (60) pour engendrer des signaux d'image vidéo et pour diviser les signaux d'image en des blocs de signal d'image, des moyens de codage (62, 64) pour coder les blocs de signal d'image en un train de données codées incorporant des codes de bloc signifiant la présence de chaque bloc de signal d'image, et des moyens de groupement (66-74) reliés aux moyens de codage pour grouper le train de données codées en des groupes de données chacun présentant un nombre présélectionné n de codes de bloc, et pour séparer des groupes de données séquentiellement par des signaux de synchronisation, caractérisé en ce
que les codes de bloc sont des signaux de fin de bloc signifiant la fin de chaque bloc de signal d'image, et en ce que les moyens de groupement comportent des moyens séparateurs (66) pour séparer les signaux de fin de bloc du train de données codées, des premiers moyens de comptage (68) reliés aux moyens séparateurs de fin de bloc pour compter les signaux de fin de bloc et pour engendrer un premier signal de comptage signifiant un comptage de n de ceux-ci, et des moyens (70, 74) reliés aux premiers moyens de comptage pour engendrer les signaux de synchronisation et pour insérer chaque signal de synchronisation dans le train de données codées en réaction au premier signal de comptage.

2. Appareil selon la revendication 1, caractérisé encore en ce que des deuxième moyens de comptage (72) comptent les signaux de synchronisation et qu'ils fournissent des signaux d'identification correspondant au nombre de signaux de synchronisation ainsi comptés, et caractérisé encore en ce qu'un signal d'identification est inséré dans le train de données codées avec au moins des signaux sélectionnés des signaux de synchronisation.

3. Appareil selon la revendication 2 ou 3, caractérisé encore en ce que des moyens de décodage reçoivent le train de données codées et qu'ils fournissent un train de données décodées étant groupé/divisé en les groupes de données en réaction à celui-ci, des troisièmes moyens de comptage (20, 24) sont couplés aux moyens de décodage pour compter les signaux de fin de bloc présents entre des signaux séquentiels des signaux de synchronisation fournisant un signal de fin de bloc manquant lorsque le nombre ainsi compté est inférieur à n, et des moyens d'insertion (52) sont reliés aux troisièmes moyens de comptage pour insérer au moins un signal de fin de bloc dans le train de données décodées en réaction au signal de fin de bloc manquant.

4. Appareil selon la revendication 1, dans lequel à au moins l'un des signaux de fin de bloc dans un groupe est attribué un mot de code étant différent des autres de manière à constituer le signal de synchronisation.

5. Appareil décodeur pour recevoir un train de données codées comportant des signaux d'image vidéo groupés en des blocs de signal d'image chacun présentant un signal de fin de bloc, une pluralité n de blocs de signal d'image constituant un groupe de données, des groupes de données séquentiels étant séparés par des signaux de synchronisation, caractérisé par des moyens de comptage de fin de bloc (20, 24) pour compter les signaux de fin de bloc présents entre des signaux séquentiels des signaux de synchronisation et pour fournir un signal de fin de bloc manquant lorsque le nombre ainsi compté est inférieur à n, et des moyens d'insertion (52) reliés aux moyens de comptage de fin de bloc pour insérer le nombre manquant de signaux de fin de bloc dans le train de données décodées en réaction à l'audit signal de fin de bloc manquant.

6. Appareil décodeur selon la revendication 5, caractérisé encore en ce que le train de données codées comporte encore des signaux d'identification de synchronisation distinguant au moins des signaux sélectionnés des signaux de synchronisation d'au moins les propres signaux de synchronisation suivants prochains, et comportant encore des moyens pour séparer les signaux d'identification de synchronisation du train de données codées.

7. Appareil décodeur selon la revendication 6, comportant encore des moyens (22) pour engendrer un signal d'identification de synchronisation local en réaction à des signaux de synchronisation reçus, et des moyens comparateurs reliés au signal d'identification de synchronisation local engendrant des moyens pour comparer le signal d'identification de synchronisation local au signal d'identification de synchronisation reçu et engendrant entre ceux-ci un signal de sortie comparateur seulement dans le cas de concordance.

8. Appareil décodeur selon la revendication 7, caractérisé encore en ce que les moyens d'insertion insèrent n signaux de fin de bloc dans le train de données décodées en absence d'un signal de sortie comparateur après la réception d'un signal de synchronisation.