EUROPEAN PATENT SPECIFICATION

(54) Work station having burst mode data transfer
Arbeitsplatz mit Stossbetriebdatenübertragung
Poste de travail informatique ayant la capacité de transfert de données en mode rafale

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• COMPUTER DESIGN vol. 29, no. 1, 1 January 1990, TULSA OK US pages 36 - 38, XP000085960
  J. BOND 'bus master interface chips boost mca transfer rate'

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Description

This invention relates to a work station or similar data processing system of the kind including a central processing unit (CPU) communicating with various external or peripheral units and devices.

Known work stations use a specific CPU e.g. an Intel 80386 microprocessor provided on a system board together with other chip units such as memories, various peripheral interfaces and a system bus controller. The CPU and the above mentioned units communicate with each other, partially through buffers, over a local bus comprising control, address and data lines, all units being under tight control of the CPU through the local bus.

In general, the system design is tailored for the specific CPU. This means that a large variety of chip units are required for work stations using different CPUs. The local bus also is tailored for the specific configuration. In order to maintain compatibility with other systems, detailed specifications rigidly determine the features and functions of the various units and their I/O registers. Thus, it is difficult to modify the system for expansion and improved performance.

Many such work stations are designed to allow the direct transfer of data between the system memory and external devices, particularly external devices which are connected to an external or peripheral bus. With the recent availability of high performance peripheral busses, existing work stations are frequently unable to take full advantage of the available performance features. One such peripheral bus is a Micro Channel bus which defines an enhanced Micro Channel architecture (MCA). One feature of the enhanced Micro Channel architecture is a form of high speed data transfer referred to as "streaming mode", in which a starting address only is provided followed by consecutive data elements. In this manner, many data elements may be consecutively transferred without having to transmit an address for each element. A feature of streaming mode is that it is asynchronous, i.e., it is not tied to a clock, and very fast. For example, it has a maximum data rate of 80 MB/sec. A bus master interface for MCA is discussed in Computer Design, Vol 29, no.1, pages 36 and 38. Such an interface is capable of single operation transfers increasing the peripheral transfer rates of standard DMA.

In contrast, existing work stations operate in a synchronous environment, i.e. their operations are timed by a system clock. Such a system is described in EP-A-0165600, where both a communication bus providing data communication between a computer and various peripheral units and an interrupt bus connecting each of the peripheral units and the CPU are synchronous in operating at the clock cycle of the computer. The time required to carry out transfers is frequently too slow to keep up with high performance external busses. For example, the normal transfer protocol supported by Intel processors requires at least two clock cycles per transfer. Thus, a work station which has a 20 MHZ CPU and a 32 bit (4 bytes) wide local bus can only transfer 40 MB/second.

It is an object of the present invention to provide a work station wherein rapid data transfer can be effected over a local bus, which is largely autonomous of the CPU.

Therefore, according to one aspect of the present invention, there is provided a work station, including a central processing unit (CPU) and memory means, a first interface circuit connected between an external bus and said CPU, said circuit enabling data transfer between said external bus and said memory unit by requesting access to a local bus, said local bus connecting said interface circuit, said CPU and said memory means, a system clock providing a timing signal to said CPU and first interface circuit, said timing signal defining consecutive time slots, each time slot equal to a single clock cycle, characterized in that said external bus is connected to a device which controls an asynchronous transfer of a starting address and consecutive data elements to said external bus and said local bus includes a control line group for controlling the transfer, over said local bus, of the starting address in a first time slot and consecutive data elements in consecutive time slots.

According to another aspect of the present invention, there is provided a method of data transfer between first and second units of a work station, said work station including a central processing unit (CPU), an external bus connecting said first unit and said CPU and a local bus connecting said first and second units and said CPU comprising the steps of:

- providing a timing signal which defines consecutive single clock cycle time slots;
- transferring asynchronously a starting address and consecutive data elements to said external bus;
- requesting access to said local bus by said first unit;
- and controlling transfer from said first unit over said local bus of said starting address in a first time slot and of consecutive data elements in consecutive time slots.

In brief summary, the work station of a preferred embodiment comprises highly integrated functional blocks provided with intelligence and each arranged on an integrated circuit chip. Each functional block serves as an active interface either for memory control (MIB), Micro Channel bus control (BIB) or local peripheral control (PIB). One or a plurality of MIBs or BIBs and one PIB communicate through a local bus with a selected CPU. The local bus is specifically extended as compared with the local bus of known work stations in order to provide more flexibility and improved performance. In particular the local bus according to a preferred embodiment of the invention comprises additional lines CT(0-1) for indicating the type of processor which has access to the
local bus (host P/M bus). Additionally, with a preferred embodiment up to four MIbs or BIBs may reside on the host P/M bus using a corresponding request signal BREQb(0..3) and a corresponding grant signal BGNTb (0..3) which serve to select an active functional block. Since only BIBs may be bus masters, only they need a BREQb line. As noted above, the host P/M bus routes "burst" signals generated by one of the functional blocks (BIB) to the functional blocks (MIb or PIB). This is specifically applicable for a streaming mode in read/write operations between a Micro Channel and the memory where the BIB functional block assumes the role of a bus master sending data through the MIb functional unit to the memory.

One embodiment of the invention will now be described by way of example with reference to the accompanying drawings, in which:-

Figure 1 is a schematic overall view of an embodiment of a work station according to the invention illustrating the various functional blocks and the connections therebetween;

Figures 2A to 2E, arranged as shown in Figure 2 are schematic diagrams showing in detail a host P/M bus as used to connect the various functional blocks with each other.

Figure 3 is a block diagram illustrating the units involved in a burst mode operation according to a salient feature of the present invention;

Figure 4 is a timing diagram used for an explanation of the operation of the work station according to the invention for a burst write cycle;

Figure 5 is a timing diagram used for an explanation of the operation of the work station according to the invention for a burst read cycle.

Figure 6 is a plan view of a physical implementation of a BIB block.

Figure 1 shows a preferred embodiment of a work station or data processing system according to the invention.

Basically, a CPU 10 communicates through a synchronous local or host P/M bus 20 with functional blocks 30, 40 and 50, and in particular with one or a plurality of bus interface circuits or blocks (BIB) 30 for microchannel access, with one or a plurality of memory interface circuits or blocks (MIb) 40 for memory and cache control and with a local peripheral and videographics array (VGA) interface circuit or block PIB 50. It should be noted that it is possible to provide more than one BIB 30 and more than one MIb 40.

It should be noted that different types of microprocessors may be used for the CPU 10, such as the Intel 80386, 80386SX, and 80486 microprocessors. Also, a coprocessor 12, such as a mathematical coprocessor Intel 80397, or 80397SX, may be added.

The functional blocks BIB 30, 40 and 50 provide an interface between local bus 20 and an asynchronous external bus such as a Micro Channel 32, memory 42 or various peripheral units. For example, the functional block BIB 30 is provided as an interface between the host P/M bus 20 and Micro Channel 32. Micro Channel 32 is provided with a plurality of slots 32A for attaching conventional adapter boards including adapter boards provided with a microprocessor which may act as a master in communication with other functional blocks of the work station. Furthermore, a control device 32B is connected to the Micro Channel 32 for controlling a fixed disk drive. A feature of Micro Channel architecture is that various connected devices, such as device 32B can be a bus master. As a bus master, device 32B controls the asynchronous transfer of data. For example, in the streaming mode, device 32C can place a starting address on Micro Channel 32 followed by the transmission or reception of consecutive data elements.

The functional block MIb 40 and DRAM memory 42 form a memory unit with MIb 40 forming an interface between the host P/M bus 20 and a DRAM memory 42. DRAM memory 42 may have different sizes with a presently usual size of 16 MB up to 64 MB. Furthermore, MIb 40 controls access to the usual BIOS ROM memory 42A.

Functional peripheral interface block (PIB) 50 forms an interface between the hosts P/M bus 20 and various conventional system peripheral units. All these units are well known in the art; therefore, they will not be explained in detail.

According to the preferred embodiment each of the functional blocks BIB 30, MIb 40, and PIB 50 has been specifically designed as a single microchip containing all elements such as registers and logic circuitry necessary to establish and perform communication between the host P/M bus 20 and the individual units connected to each functional block 30, 40 and 50.

As indicated in Figure 1 it should be noted that a number M of BIBs 30 and a number N of MIbs 40 may be provided all connected to the host P/M bus 20. Thus, a large variety of configurations with different CPUs and quite different memory capacities may be implemented. Each chip may be configured quite differently to match various system configurations.

It should be understood that each functional block 30, 40, 50 is provided with some intelligence offering an operation which is relatively independent from the CPU operation generally governing all functions of the system.

Basically, each functional block 30, 40, 50 includes an interface unit between the host P/M bus 20 and an individual internal transaction bus (not shown). Though the timing is based on the CPU clock all operations within the functional block such as read or write operations will be independently performed in one cycle whilst the CPU needs at least two cycles of the CPU clock. Accordingly, this type of system architecture offers a considerably improved performance in view of the reduction in wait states for the CPU resulting in a higher overall
operating speed.

The specifically extended host P/M bus 20 of the preferred embodiment of the work station of the invention is illustrated in Figures 2A to 2E in detail.

Specifically, within the block CPU 10 the conventional input/output ports of a microprocessor as Intel 80386, etc. are listed as address ports A (2..31), data ports D (0..31), byte enable ports BEb (0..3), and an address status output ADSb which indicates that a valid bus cycle definition and address are available and which is driven active in the same clock as the addresses are driven. ADSb is active low, the system clock PCLK timing signal is generated by a clock oscillator 60 (Figure 2B) and provided to the input port PCLK of the CPU 10 and the functional blocks BIB 30, MIB 40, and PIB 50. These and all other input/output ports of the CPU 10 and the signal presented there there are conventional. Thus, they will not be explained in detail.

As may be gathered from Figures 2A to 2E the functional blocks BIB 30, MIB 40, and PIB 50 are provided with similar input/output ports as the CPU. However, there are several additional ports and associated bus lines connecting corresponding parts of the functional blocks 30, 40, 50 and the CPU 10 with each other.

**Table 1**

PCLK: This clock provides the fundamental timing and the operating frequency for all the functional units which are connected to the host P/M bus. All external timing parameters are specified with respect to the rising edge of PCLK. The clock frequency may range from 16 MHz to 33 MHz according to the specified processor frequency.

A(2..31): These address lines, together with the byte enable lines BE0b-BE3b, define the physical area of memory or input/output space accessed. Address lines A31-A4 are used to drive addresses into the 80486 microprocessor to perform cache line invalidations.

D(0..31): These are the data lines. The lines D0-D7 define the least significant byte of the data bus while lines D24-D31 define the most significant byte of the data bus.

BE(0..3): The byte enables signals indicate active bytes during read and write cycles. BE3b applies to D24-D31, BE2b applies to D16-D23, BE1b applies to D8-D15, and BEOb applies to D0-D7. BEOb - BE3b are active low.

ADSb: The address status output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADSb is driven active in the same clock as the addresses are driven. ADSb is active low.

CT(0..1): The combination of the two lines included in the host P/M bus indicates the type of processor (functional block) which may be bus master on the host P/M bus. For example, CT1 = 1, and CTO = 0 may mean that the host CPU 10 is an Intel 40486 processor. It should be noted that the signals on these two lines are transmitted by the PIB 50 to each of any BIBs 30 and MIBs 40.

BFREQb(0..3): This is a host P/M bus request signal with the assumption that four BIBs 30 may be provided each being connected with the PIB 50 by one request line.

BGMb(0..3): This is a host P/M bus grant signal transmitted by the PIB 50 to one of the BIBs 30 having requested access to the host P/M bus by BREQb (0..3).

SBURST(bL)b: This signal is generated by one of the functional blocks BIB 30 of the chip set, specifically one of the BIBs 30 only if the host CPU 10 is currently not bus master, to specify a BURST operation. It is used to temporarily halt the transfer in burst mode but keeps the burst condition established. With this signal the bus master is able to stop the transfer temporarily in burst mode. (Further description see below).

BRDYb(N): This signal indicates that valid data are presented on the data lines in response to a read or the data on the line are accepted in response to a write.

BRDYBLb(N): The burst ready block is the BRDYb signal generated by one of the functional blocks of the chipset.

LOCKb: The bus lock line indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCKb is asserted. LOCKb goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked clock ends when ready is returned. LOCKb is active low. If CT0 and CT1 are set to 11, (from the PIB 50) then LOCKb is active as long as the system should remain in burst condition. This is used for MCA streaming mode.

In contrast to known systems there are various multiple signals applied to one corresponding port each of the CPU 10 the multiple signals being generated by the BIBs 30 and MIBs 40 if provided in multiplicity. Examples are RDYBLb(N) which is the RDYb (ready) signal generated by one of the functional blocks of the chip set and fed to the RDYb input port of the CPU 10. Similarly, there is a BRDYBLb signal which is the burst ready signal generated by one of the functional blocks of the chip set and fed to the BRDYb input port of the CPU.

As mentioned above in connection with the explanation of the host P/M bus 20 (Figs 2A and 2B) the SBRUST signal is generated by a BIB having been granted access to the host P/M bus 20. In this case not the host CPU but the BIB is the current bus master. During a burst mode data transmission to a selected MIB 40 in the embodiment according to Figure 3, the active BIB is able to maintain burst mode access to the host P/M bus 20 despite temporary interruptions in the data transmission. As regards the burst mode operation it should be noted that in contrast to a normal read/write operation where only one address and data stored therein are transmitted in one read/write cycle, the burst mode operation permits consecutive data or command transmission for several addresses without repeatedly
requesting access to the host P/M bus 20.

The reason for providing this SBURST feature is that there may be some discontinuity in data flow through the BiB from the Micro Channel 32 which discontinuity should, however, not result in losing access of the active BiB to the host P/M bus 20.

Referring now to Figures 1, 2A to 2E and 3, an important feature of the preferred embodiment of the work station according to the invention will be explained, with Figure 3 showing the functional blocks and units especially involved.

As explained before in connection with Figures 1 and 2A to 2E, the host P/M bus 20 comprises a plurality of lines (see Figures 2A to 2E and Table 1) connected to the respective ports of the CPU 10, for example an Intel microprocessor 80486 and one (or several) MIB(s) 40. Specifically, the host P/M bus 20 includes address lines A2 to A31 and data lines D0 to D31. Therefore, the host P/M bus 20 is adapted for parallel transfer of an address and data with a full width of 32 bits or 4 bytes each.

As a modification of the system shown in Figures 1 and 2A to 2E, the BiB 30 is not directly connected to the host P/M bus 20. As mentioned before, the BiB 30 is implemented as an integrated microchip as shown in Figure 6. As may be seen, all of the pins have a definite assignment with 64 pins assigned to a Micro Channel connection for a 64-bit or 8-byte parallel data transfer. This reduces the number of pins available for interfacing to the host P/M bus 20. Thus, a group of 32 pins, i.e. A/DO to A/D31 are assigned to transfer alternatively either addresses or data.

In order to match the configuration of the host P/M bus 20 there is provided a multiplexer/demultiplexer 70 which may be implemented in TTL technique, for example as a commercially available 74543 chip.

Basically, the unit MUX 70 has at its one side ports for connection to the group of address lines A0 to A31 and ports for connection to the group of data lines D0 to D31 of the host P/M bus 20 which means that there are in total 64 ports. At the other side, the MUX 70 is provided with 32 ports connected through lines 37 with the 32 pins A/DO to A/D31 of the BiB 30 (Figure 6) as mentioned before. Note that only address lines A2 to A31 are utilized in the BiB 30.

The MUX 70 acts as a change-over switch, routing an address presented at the ports from the BiB 30 to the group of address lines of the host P/M bus 20, and data presented thereafter by the BiB 30, after switching over under control of a corresponding control signal on line 38, to the group of data lines of the host P/M bus 20.

Figure 3 shows the SBURSTb line 41 (see Table 1) and an EADSb line 43 which are lines of the host P/M bus 20 but not shown separately in Figure 3.

As mentioned before the SBURSTb signal generated by the BiB 30 indicates to the MIB 40 that a continuous data transfer, i.e. for a plurality of addresses is intended.

The EADSb signal indicates to the CPU 10 that there is such a data transfer between the BiB 30 and the MIB 40. Thus, the CPU 10 is able to invalidate any addresses/data contained in internal caches since such data may be changed by the data transfer between BiB 30 and MIB 40 in the DRAM 42.

Referring now to Table 1 and Figures 1 to 4, the operation of the work station according to the preferred embodiment of the invention will be explained for the situation that a SBURST write cycle shall be performed with the BiB 30 being the bus master. In such a cycle data will be communicated from the BiB 30 through the MUX 70 to the host P/M bus 20 and received therefrom by the MIB 40 for storage in the DRAM 42.

In Figure 4 line (a) represents the CPU clock PCLK governing all timing within the system. Consecutive time slots are defined by single clock cycles and are shown between adjacent dotted vertical lines.

As may be gathered from line (c) a first address A0 is presented by the BiB 30 through the MUX 70 to the host P/M bus 20 taking over and holding this address A0 as indicated in line (f) for the host P/M bus address lines (HPMA). EADSb going active low indicates that a first address A0 is presented to the host P/M bus 20. For the next cycle MUX 70 switches to the group of data lines for presenting their data D0 to the host P/M bus 20 as may be seen in the HPMD line (g).

With the SBURSTb signal having gone active low at the beginning of the SBURST write cycle (line (e)), the host P/M bus 20 is locked to the data transfer by signal LOCKb (line (h)) going active low for the whole data transfer period.

It should be noted that no further address is presented by the BiB 30 through the MUX 70. Rather, there is a continuous flow of data D1...D6 out of the consecutive addresses following A0 from the BiB 30 through the MUX 70 to the group of data lines for presentation there one after the other for being written via the MIB 40 to the DRAM 42. Consecutive data elements, i.e. data elements with consecutive addresses, are provided in consecutive time slots unless there is a pause or delay in the data transfer, as will be described below.

It should be noted that for this purpose it is the MIB 40 as a slave which calculates the consecutive addresses A1...A5 for respective data D1...D5 as presented on the group of data lines and the group of address lines of the host P/M bus 20 as indicated in HPMD line (g) and HPMA line (f).

Furthermore, a signal generated by the BiB 30 on the line 38 going active low indicates the switching-over of MUX 70 from the address ports to the data ports, maintaining this state for the whole SBURST write cycle.

A further important feature of the present invention may be recognized in the middle portion of Figure 4 where it is shown that there is some delay or pause in the transfer of data D2, indicated by the SBURST signal going inactive high temporarily, for example if the source is not ready to present data, or the receiver is not ready.
to receive data. Nevertheless, data transfer is not interrupted but maintained in view of the active LOCKb signal (line (h)).

Signal BRDYb according to line (d) of the host P/M bus 20 goes active low as generated by the MIB 40 indicating that the data D2 on the bus has been accepted. A further situation is indicated in line (c) after D2 with a cycle of invalid data presented causing BRDYb signal (line (d)) going inactive high for one cycle and a delay in presenting D2 on HPMD (line (g)).

Thus, it will be appreciated that by demultiplexing addresses and data and having the MIB 40 as a slave calculate consecutive addresses, a fast data transfer is accomplished in a SBURST write mode without interruption.

In Figure 5 three types of data transfer between the BIB 30 and any other functional block as a MIB 40 are illustrated starting with a single write cycle followed by a single read cycle and with a SBURST read cycle shown in the right-hand part of Figure 5. Corresponding lines are marked with the same letters as in Figure 4.

As with the SBURST write cycle (Figure 4), the BIB 30 in a single write cycle first presents an address A1 to the MUX 70 which is in a position to present this address immediately to the group of address lines of the host P/M bus 20 according to HPMA line (f). With the MUX 70 switched to the group of data ports, data D1 of address A1 is presented to the MUX 70 and further to the group of data lines of the host P/M bus 20 according to the HPMD line (g). Thus, the requested functional block, such as the MIB 40, is now able to take over both the address A1 and the data D1 from the host P/M bus 20 for writing into the DRAM 42.

As explained with the SBURST write cycle (Figure 4), the signal ADSb line (b)) going active low indicates a valid address being presented on the host P/M bus 20 whilst RDYb signal (line (d1)) indicates a valid data transfer for the data D1.

As regards a single read cycle, again the BIB 30 as a bus master presents an address A1 through the MUX 70 to the host P/M bus 20 as indicated in lines (c) and (f). As soon as the associated data D2 is available on the group of data lines of the host P/M bus 20 (line (g)) it is presented to the MIB 30 through the MUX 70 now acting as a multiplexer in reverse direction.

As regards a SBURST read cycle illustrated in Figure 5, right-hand portion, reference is made first to the description given above in connection with Figure 4 in respect of the SBURST write cycle.

As may be gathered from Figure 5, as with a single write cycle first an address A2 is presented through the MUX 70 to the host P/M bus 20 where it is held until the associated data D2 is presented on the group of data lines (line (g)) on the host P/M bus 20 with the SBURSTb signal (line (e)) being active low through the whole SBURST read cycle.

As illustrated in line (f) consecutive addresses A1, A3 following A2 are generated by the responding MIB 40 as a slave for fetching further data D1, D2 from the DRAM memory through the MIB 40 for presenting them on the group of data lines of the host P/M bus 20 and for receipt by the BIB 30 through the MUX 70 again working as a multiplexer.

In lines (l) and (g) it is shown that there might be an extension of the cycle as indicated for A1/D1 for a time where the BRDYb signal temporarily changed to an inactive high. Data transfer will not be interrupted despite this halt of the cycle since the LOCKb signal (line (h)) stays active low over the entire SBURST read cycle.

It should be noted that both the SBURST write cycle and the SBURST read cycle are performed without involving the CPU 10, which may do other tasks in this time.

As a further important feature of the present embodiment it should be noted that in connection with the request/grant procedure of the BIB 30 the bus master function is transferred from the CPU 10 to the BIB 30 which is indicated by a dynamic change of the CT (0.1) signal (Figure 2) to "11" presented to the MBs 40 and the BIBs 30 as single CT(0.1).

With the work station of the preferred embodiment each functional block is implemented by a single microchip, preferably formed in HCMOS technique. Each microchip comprises all sub-units, such as registers and logic circuitry, required. Though the chips are standardized they may be used in a variety of system configurations since they include ample register space for configuration data such as the of CPU, operating frequency, DRAM memory space, etc.

Specifically, according to one aspect of the invention, the shortage of pins available for data transfer is overcome by the use of a multiplexer/demultiplexer, such as MUX 70.

As an example, the chip may be implemented in an ASIC package using 208 pins which may be easily placed on the system board of the work station. Figure 6 shows a plan view of the BIB ASIC package with pin assignment.

**Claims**

1. A work station, including a central processing unit (CPU) (10) and memory means (40, 42), a first interface circuit (30) connected between an external bus (32) and said CPU (10), said circuit (30) enabling data transfer between said external bus (32) and said memory unit (42) by requesting access to a local bus (20), said local bus (20) connecting said interface circuit (30), said CPU (10) and said memory means (40, 42), a system clock providing a timing signal to said CPU (10) and first interface circuit (30) said timing signal defining consecutive time slots, each time slot equal to a single clock cycle, characterized in that, said external bus (32) is connected to a device which controls an asynchronous
transfer of a starting address and consecutive data elements to said external bus (32) and said local bus (20) includes a control line group for controlling the transfer, over said local bus (20), of the starting address in a first time slot and consecutive data elements in consecutive time slots.

2. A work station according to claim 1, characterized in that said interface circuit (30) is designed as a self-contained functional block formed as an integrated circuit chip and provided with a predetermined number of connecting pins, a group thereof being assigned for communicating either addresses or data; in that said local bus (20) further includes both an address line group and a data line group each corresponding in number to said group of connecting pins of said interface circuit; and in that a multiplexer/demultiplexer (70) is connected on one side to said group of pins of said interface circuit and on the other side to both said address line group and said data line group; and in that a control line (36) extending between said interface circuit (30) and multiplexer/demultiplexer (70) is effective to switch said multiplexer/demultiplexer (70) from said address line group to said data line group under control of said interface circuit (30) through said control line (38).

3. A work station according to claim 1 or claim 2, characterized in that said memory means (40, 42) includes a memory (42), and a second interface circuit (40) connected between said local bus (20) and said memory (42) in that said control line group includes a first line (SBURST) for presenting a burst signal generated by said first interface circuit (30) as a bus master and received by said second interface circuit (40) as a slave indicating a continuous data transfer (burst mode) to follow, and in that said control line group further includes a second line (LOCK) for locking said local bus (20) for said continuous data transfer for the duration of the burst mode.

4. A work station according to claim 3, characterized in that said control line group further includes a third line (EADS) for transmitting a signal from said first interface circuit (30), to said CPU (10) indicating a burst mode data transfer between said first interface circuit (30) and said second interface circuit (40) and adapted to invalidate any data contained in a cache memory of said CPU, in accordance with addresses calculated in said second interface circuit (40).

5. A work station according to claim 3 or claim 4, characterized in that said external (32) bus is a Micro Channel bus, wherein an active to inactive transition of said BURST signal temporarily halts a transfer of data in the burst mode whilst maintaining a communication between said bus master and said slave.

6. A work station according to any of the preceding claims, characterized by: a plurality of first interface circuits (30) connected respectively between a plurality of external busses (32) and said local bus (20); and a plurality of second interface circuits (40) connected respectively between a plurality of memories (42) and said local bus (20); and in that each of said first and second interface circuits (30, 40) is designed as a self-contained functional block formed as an integrated circuit chip.

7. A work station according to any one of the preceding claims, characterized in that said local bus (20) includes lines (CT (0, 1)) connected between said CPU (10) and said first interface circuit (30) for dynamically changing a bus master function from one to the other.

8. A method of data transfer between first (30) and second (40) units of a work station, said work station including a central processing unit (CPU) (10), an external bus (32) connecting said first unit (30) and said CPU (10) and a local bus (20) connecting said first (30) and second (40) units and said CPU (10) comprising the steps of:

   providing a timing signal which defines consecutive single clock cycle time slots;
   characterized in that it further comprises

   transferring asynchronously a starting address and consecutive data elements to said external bus;
   requesting access to said local bus (20) by said first unit (30); and
   controlling transfer from said first unit (30) over said local bus (20) of said starting address in a first time slot and of consecutive data elements in consecutive time slots.

9. A method according to claim 8, characterized by the steps of: transmitting a first signal (SBURST) on said local bus (20) from said first (30) to said second (40) unit indicating a continuous data transfer; generating a second signal (LOCK) on said local bus (20) for locking said local bus (20) for continuous data transfer; presenting a starting address on said local bus (20) by said first unit (30); providing data in consecutive time slots from one of said units (30, 40) to said local bus (20), said data corresponding to said starting address and consecutive addresses; and calculating said consecutive addresses in a unit (40) receiving said data.

10. A method according to claim 9, characterized by the
steps of removing said first signal (SBURST) while maintaining said second signal (LOCK) on said local bus (20) to temporarily interrupt said data transfer.

11. A method according to claim 9 or claim 10, characterized in that said local bus (20) has a group of address lines and a parallel group of data lines, said first unit (30) having fewer input/output ports assigned to data/address transfer than the sum of said address and data lines, and in that either said data is provided by said first unit (30) at the same ports as said starting address and is demultiplexed to said data lines of said local bus (20) or said data is provided by said second unit (40) onto the data lines of said local bus (20) said data being multiplexed to the same ports of said at least one unit used for presenting said starting address to said local bus (20).

Patentansprüche

1. Arbeitsstation, aufweisend eine Zentraleinheit (CPU) (10) und eine Speichereinrichtung (40, 42), eine erste Schnittstellenschaltung (30), die zwischen einen Externbus (32) und die CPU (10) geschaltet ist, wobei die Schaltung (30) eine Datenübertragung zwischen dem Externbus (32) und der Speichereinheit (42) durch das Anfordern eines Zugriffs auf einen lokalen Bus (20) ermöglicht, wobei der lokale Bus (20) die Schnittstellenschaltung (30), die CPU (10) und die Speichereinrichtung (40, 42) verbindet, sowie einen Systemtakt, der ein Taktzeugnis dient für die CPU (10) und die erste Schnittstellenschaltung (30) bereitstellt, wobei das Taktzeugnis aufeinanderfolgende Zeitschlitze definieren, wobei jeder Zeitschlitz gleich einem einzelnen Takzyklus ist, dadurch gekennzeichnet, daß der Externbus (32) mit einer Einrichtung verbunden ist, die eine Asynchronübertragung einer Anfangsadresse und nachfolgender Datenblöcke zum Externbus (32) steuert, und der lokale Bus (20) eine Steuerungsgruppe zum Steuern der Übertragung der Anfangsadresse bei einem ersten Zeitschlitze und nachfolgender Datenblöcke bei nachfolgenden Zeitschlitzen über den lokalen Bus (20) umfaßt.

2. Arbeitsstation nach Anspruch 1, dadurch gekennzeichnet, daß die Schnittstellenschaltung (30) als eine Datenübertragung auf ein nicht-übersetztes kompatibelsignal für die CPU (10) und die erste Schnittstellenschaltung (30) bereitstellt, wobei das signal aufeinanderfolgende Zeitschlitze definieren, wobei jeder Zeitschlitz gleich einem einzelnen Takzyklus ist, dadurch gekennzeichnet, daß die Übertragung der Anfangsadresse bei einem ersten Zeitschlitze und nachfolgender Datenblöcke bei nachfolgenden Zeitschlitzen über den lokalen Bus (20) umfaßt.

3. Arbeitsstation nach Anspruch 1 oder Anspruch 2, dadurch gekennzeichnet, daß die Speichereinrichtung (40, 42) einen Speicher (42) und eine zweite Schnittstellenschaltung (40) umfaßt, die zwischen den lokalen Bussen (20) und den Speicher (42) geschaltet ist, daß die Steuerungsgruppe eine erste Leitung (SBURST) zum Anbieter eines Bootsignals umfaßt, das durch die erste Schnittstellenschaltung (30) als eine Bushauptstelle erzeugt und durch die zweite Schnittstellenschaltung (40) als eine Nebenstelle empfangen wird, während es anzeigt, eine kontinuierliche Datenübertragung (Burst-Betrieb) zu folgen; und daß die Steuerungsgruppe ferner eine zweite Leitung (LOCK) zum Sperren des lokalen Busses (20) für die kontinuierliche Datenübertragung für die Dauer des Burst-Betriebs umfaßt.

4. Arbeitsstation nach Anspruch 3, dadurch gekennzeichnet, daß die Steuerungsgruppe ferner eine dritte Leitung (EADS) zum Übertragen eines Signals von der ersten Schnittstellenschaltung (30) zur CPU (10) umfaßt, das eine Burst-Betrieb-Datenübertragung zwischen der ersten Schnittstellenschaltung (30) und der zweiten Schnittstellenschaltung (40) auslöst und ausgelegt ist, entsprechend der in der zweiten Schnittstellenschaltung (40) berechneten Adressen irgendwelche Daten, die in einem Cache-Speicher der CPU enthalten sind, ungültig zu machen.


6. Arbeitsstation nach einem der vorangehenden Ansprüche, gekennzeichnet durch eine Vielzahl erster Schnittstellenschaltungen (30), die entsprechende Datenübertragung auf ein nicht-übersetztes kompatibles Signal auf der CPU (10) umfaßt.
chend zwischen einer Vielzahl von Externbussen (32) und den lokalen Bus (20) geschaltet sind; und eine Vielzahl zweiter Schnittstellenschaltungen (40), die entsprechend zwischen einer Vielzahl von Speichern (42) und den lokalen Bus (20) geschaltet sind; und dadurch gekennzeichnet, daß jede der ersten und zweiten Schnittstellenschaltungen (30, 40) als ein unabhängiger Funktionsblock ausgelegt ist, der als ein integrierter Schaltungschip ausgebil-
det ist.

7. Arbeitsstation nach einem der vorhergehenden An-
sprünge, dadurch gekennzeichnet, daß der lokale Bus (20) Leitungen (CT (0, 1)) umfaßt, die zwischen der CPU (10) und der ersten Schnittstellenschal-
tung (30) für ein dynamisches Ändern einer Bus-
haftfunktion von einer zur anderen ge-
schaltet sind.

8. Verfahren für eine Datenübertragung zwischen er-
sten (30) und zweiten (40) Einheiten einer Arbeits-
station, wobei die Arbeitsstation eine Zentraleinheit (CPU) (10), einen Externbus (32), der die erste Ein-
heit (30) und die CPU (10) verbindet, und einen lokalen Bus (20) aufweist, der die erste (30) und die zweite (40) Einheit und die CPU (10) verbindet, das die Schritte aufweist:

- Bereitstellen eines Taktsignals, das aufein-
anderfolgende, einzelne Taktzyklus-Zeichenspitzen definiert;

dadurch gekennzeichnet, daß es ferner aufweist:

- asynchrones Übertragen einer Anfangsadresse und nachfolgender Datenbausteine zum Ex-
ternbus;
- Anfordern eines Zugriffes auf den lokalen Bus (20) durch die erste Einheit (30); und
- Steuern der Übertragung von der ersten Einheit (30) über den lokalen Bus (20) der Anfangs-
adresse bei einem ersten Zeitschlitze und auf-
einanderfolgender Dateinhalte bei aufein-
anderfolgenden Zeitschlitzen.

9. Verfahren nach Anspruch 8, gekennzeichnet durch die Schritte: Übertragen eines ersten Signals (SBburst) auf dem lokalen Bus (20) von der ersten (30) zur zweiten (40) Einheit, das eine kontinuierli-
dene Datenübertragung anzeigt; Erzeugen eines zweiten Signals (lock) auf dem lokalen Bus (20) zum Sperren des lokalen Busses (20) für eine kon-
tinuierliche Datenübertragung; Anbieten einer Anfangsadresse auf dem lokalen Bus (20) durch die erste Einheit (30); Bereitstellen von Daten in aufein-
derfolgenden Zeitschlitzen von einer der Einheiten (30, 40) für den lokalen Bus (20), wobei die Da-
ten zur Anfangsadresse und nachfolgenden Adres-

sen gehören; und Berechnen der nachfolgenden Adressen in einer Einheit (40), die die Daten empfängt.

10. Verfahren nach Anspruch 9, gekennzeichnet durch die Schritte des Empfängens des ersten Signals (SBburst) während des Beibehalts des zweiten Signals (lock) auf dem lokalen Bus (20) zum zeit-
weiligen Unterbrechen der Datenübertragung.

11. Verfahren nach Anspruch 9 oder Anspruch 10, da-
durch gekennzeichnet, daß der lokale Bus (20) eine Gruppe von Adressleitungen und eine parallele Gruppe von Datenleitungen aufweist, wobei die er-
ste Einheit (30) weniger Eingangs-/ Ausgangsan-
schlüsse aufweist, die der Daten-/ Adressenüber-
tragung zugewiesen sind, als die Summe der Adreß- und Datenleitungen, und daß entweder die Daten durch die erste Einheit (30) an den gleichen Anschlüssen wie denen der Anfangsadresse bereit-
gestellt werden und zu den Datenleitungen des lo-
kalen Busses (20) demultiplex ausgegeben wer-

Ben, oder die Daten durch die zweite Einheit (40) auf den Datenleitungen des lokalen Busses (20) be-

Revidications

1. Un poste de travail comportant une unité centrale (UC) (10) et un moyen mémoire (40, 42), un premier circuit d'interface (30) connecté entre un bus exter-

ne (32) et ladite UC (10), ledit circuit (30) permettant le transfert de données entre ledit bus externe (32) et ledit moyen mémoire (42) en demandant l'accès à un bus local (20), ledit bus local (20) connectant ledit circuit d'interface (30), ladite UC (10) et ledit moyen mémoire (40, 42), une horloge de système fournissant un signal de rythme à ladite UC (10) et au premier circuit d'interface (30), ledit signal de rythme définissant des créneaux consécutifs, cha-

cque créneau égal à un cycle d'horloge unique, ca-
ractérisé en ce que ledit bus externe (32) est con-

cécté à un dispositif qui contrôle un transfert asyn-
chrone d'une adresse de début et de données con-
sécutives audit bus externe (32) et en ce que ledit bus local (20) comporte un groupe de lignes de con-
trôle pour contrôler le transfert, sur ledit bus local (20), de l'adresse de début dans un premier cré-

neau et des données consécutives dans des cré-

neaux consécutifs.

2. Un poste de travail conformément à la revendica-
tion 1, caractérisé en ce que ledit circuit d'interface
(30) est conçu en tant que bloc fonctionnel autonome formé en tant que circuit intégré et doté d'un nombre prédéterminé de fiches de connexion, dont un groupe est affecté pour communiquer soit des adresses soit des données, en ce que ledit bus local (20) comporte encore à la fois un groupe de lignes d'adresse et un groupe de lignes de données, chacun correspondant en nombre audit groupe de fiches de connexion dudit circuit d'interface; et en ce qu'un multiplexeur/démultiplexeur (70) est connecté d'un côté audit groupe de fiches dudit circuit d'interface et de l'autre côté à la fois audit groupe de lignes d'adresse et audit groupe de lignes de données; et en ce qu'une ligne de contrôle (38) s'étendant entre lesdits circuit d'interface (30) et multiplexeur/démultiplexeur (70) sert à commuter ledit multiplexeur/démultiplexeur (70) audit groupe de lignes d'adresse audit groupe de lignes de données sous le contrôle dudit circuit d'interface (30) à travers ladite ligne de contrôle (38).

3. Un poste de travail conformément à la revendication 1 ou à la revendication 2, caractérisé en ce que ledit moyen mémoire (40, 42) comporte une mémoire (42), et un deuxième circuit d'interface (40) connecté entre ledit bus local (20) et ladite mémoire (42), en ce que ledit groupe de lignes de contrôle comporte une première ligne (SBURST) pour présenter un signal BURST (mode continu) généré par ledit premier circuit d'interface (30) en tant que maître de bus et reçu par ledit deuxième circuit d'interface (40) en tant qu'esclave indiquant un transfert de données continu (mode continu) à suivre; et en ce que ledit groupe de lignes de contrôle comporte encore une deuxième ligne (LOCK) pour verrouiller ledit bus local (20) pour ledit transfert de données continu pour la durée du mode continu.

4. Un poste de travail conformément à la revendication 3, caractérisé en ce que ledit groupe de lignes de contrôle comporte encore une troisième ligne (EADS) pour transmettre un signal dudit premier circuit d'interface (30), à ladite UC (10) indiquant un transfert de données en mode continu entre ledit premier circuit d'interface (30) et ledit deuxième circuit d'interface (40) et adapté pour invalider toutes données contenues dans une mémoire cache de ladite UC, conformément à des adresses calculées dans ledit deuxième circuit d'interface (40).

5. Un poste de travail conformément à la revendication 3 ou à la revendication 4, caractérisé en ce que ledit bus externe (32) est un bus Micro Channel, et dans quoi une transition actif-inactif dudit signal BURST (mode continu) arrête temporairement un transfert de données en mode continu tout en maintenant une communication entre ledit maître de bus et ledit esclave.

6. Un poste de travail conformément à l'une quelconque des revendications précédentes, caractérisé par: une pluralité de premiers circuits d'interface (30) connectés respectivement entre une pluralité de bus externes (32) et ledit bus local (20); et une pluralité de deuxième circuits d'interface (40) connectés respectivement entre une pluralité de mémoires (42) et ledit bus local (20); et en ce que chacun desdits premiers et deuxième circuits d'interface (30, 40) est conçu en tant que bloc fonctionnel autonome formé en tant que circuit intégré.

7. Un poste de travail conformément à l'une quelconque des revendications précédentes, caractérisé en ce que ledit bus local (20) comporte des lignes (CT (O, 1) connectées entre ladite UC (10) et ledit premier circuit d'interface (30) pour changer dynamiquement une fonction maître de bus de l'une à l'autre.

8. Une méthode de transfert de données entre les premières (30) et deuxième (40) unités d'un poste de travail, ledit poste de travail comportant une unité centrale (UC) (10), un bus externe (32) connectant ladite première unité (30) et ladite UC (10) et un bus local (20) connectant lesdites première (30) et deuxième (40) unités, et ladite UC (10) comprenant les étapes suivantes:

   la fourniture d'un signal de rythme qui définit des créneaux de cycle d'horloge uniques consécutifs;

   caractérisée en ce qu'elle comprend encore le transfert asynchrone d'une adresse de début et de données consécutives audit bus externe; la demande d'accès audit bus local (20) par ladite première unité (30); et le contrôle du transfert de ladite première unité (30) sur ledit bus local (20) de ladite adresse de début dans un premier créneau et de données consécutives dans des créneaux consécutifs.

9. Une méthode conformément à la revendication 8, caractérisée par les étapes suivantes: la transmission d'un premier signal (SBURST) sur ledit bus local (20) de ladite première (30) à ladite deuxième (40) unité indiquant un transfert de données continu; la génération d'un deuxième signal (LOCK) sur ledit bus local (20) pour verrouiller ledit bus local (20) pour un transfert de données continu; la présentation d'une adresse de début sur ledit bus local (20) par ladite première unité (30); la fourniture de données dans des créneaux consécutifs de l'une desdites unités (30, 40) audit bus local (20), lesdites données correspondant à ladite adresse de début et à des adresses consécutives; et le calcul desdites adresses consécutives dans une unité (40) re-
10. Une méthode conformément à la revendication 9, caractérisée par les étapes suivantes : le retrait du dit premier signal (SBURST) tout en maintenant le dit deuxième signal (LOCK) sur ledit bus local (20) pour interrompre temporairement ledit transfert de données.

11. Une méthode conformément à la revendication 9 ou à la revendication 10, caractérisée en ce que ledit bus local (20) a un groupe de lignes d'adresse et un groupe parallèle de lignes de données, ladite première unité (30) ayant moins de ports d'entrée/de sortie affectés au transfert de données/d'adresses que la somme desdites lignes d'adresse et de données, et en ce que soit lesdites données sont fournies par ladite première unité (30) aux mêmes ports que ladite adresse de début et sont démultiplexées auxdites lignes de données dudit bus local (20) soit lesdites données sont fournies par ladite deuxième unité (40) sur les lignes de données dudit bus local (20), lesdites données étant démultiplexées aux mêmes ports de ladite au moins une unité utilisée pour présenter ladite adresse de début audit bus local (20).
FIG. 2B

A(2..23)
D(0..31)
BEb(0..3)
A20G
ADSb
M/IOb,D/Cb,W/Rb
LOCKb
PCLK
RDYb
RDYBLb
RESET
BLASTb
EADSBLb
BRDYBLb
BRDYb
KENBLb
NMIBL
NMI
BOFFBLb
SBURSTb
REFREQb
CT(0,1)
BREQb
BGNTb
REFb
CIN
COUT
CSETUPb
PRDYb
FDCDA CKb
FDCD RQ
### FIG. 6A

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</tr>
<tr>
<td>3</td>
<td>GBAb</td>
</tr>
<tr>
<td>4</td>
<td>GDb</td>
</tr>
<tr>
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**BIB ASIC**

*(PIN ASSIGNMENT)*
### FIG. 6B

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**BIB ASIC**

**(PIN ASSIGNMENT)**