EUROPEAN PATENT SPECIFICATION

stored data protection apparatus for electronic device
Vorrichtung für elektronisches Gerät zum gespeicherten Daten-Schutz
Dispositif pour appareil électronique de protection de données stockées

Designated Contracting States: DE GB

Priority: 30.08.1990 JP 22872790

Date of publication of application: 04.03.1992 Bulletin 1992/10

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a stored data protection apparatus for an electronic device such as an electronic notebook, a pocket computer and the like, having a volatile memory which maintains stored data by a battery power supply.

2. Description of the Related Art

[0002] In general, an electronic device having a computer, for example such as an electronic notebook, a pocket computer and the like, carries a main battery for normally supplying power to both of a CPU (Central Processing Unit) and a RAM (Random Access Memory) in the device, and a back-up battery for supplying power to the RAM when the power supply voltage from the main battery is reduced or such main battery is taken out from the device for replacement, so as to prevent data stored in the RAM or other volatile memory from being destroyed.

[0003] In case that the main battery is replaced with a new one under the assistance of the back-up battery, a ringing phenomenon often occurs in power supply voltage. More particularly, the ringing phenomenon is most likely to occur when a new main battery is set in the electronic device. Such ringing phenomenon may cause the CPU of the device to run away from its instructions, so that there is a fear that wrong data is written into the RAM destroying the data having been already stored in the RAM.

[0004] In order to solve the above problem inherent in the conventional electronic device, the device is generally provided with a manually operated switch for blocking off a chip-enable signal issued from the CPU to the RAM, and a manually operated reset switch for resetting the CPU. For replacing the main battery with a new one, a user of the device has to sequentially operate these manual switches in a predetermined order.

[0005] Replacement of the main battery with a new one is performed as follows. First of all, after the device is put in a stand-by mode, the manual switch is turned off so as to block off the chip-enable signal. Then, the old main battery is replaced with a new one. After that, the reset switch is manually operated so as to reset the CPU. Finally, the manual switch is turned on to permit the chip-enable signal to be applied to the RAM. Through the above sequential manual operation conducted by the user, it is possible to prevent the stored data from being destroyed even if the CPU runs away during the replacement of the main battery.

[0006] However, since it is necessary for the user to manually operate the switches sequentially, there is a fear that the user makes some mistakes in the above manual operation causing the stored data to be destroyed. Furthermore, even when the above manual operation is properly conducted by the user, there is still a fear that the CPU runs away causing the stored data to be destroyed when the new main battery now set in the device can not supply, to the RAM, sufficient power necessary for maintaining the stored data in the RAM.

[0007] DE 3625179 A discloses protection apparatus for a device of the aforementioned type, including switching means comprising 2 switches formed by the main battery cover, operable between a first and a second position, taking the first position when the main battery is connected and being switched to the second position prior to main battery removal. In the first position, a read/write signal is connected from the CPU to the memory, and an input to a reset circuit within the CPU is left open, whereas in the second position, the read/write signal from the CPU is isolated from the memory (the memory input is tied to the ‘read’ level) and the CPU reset input is activated. Thus, before the battery is removed, the CPU is reset to prevent accesses to the memory and the read/write signal to the memory is forced to the read state. When a new battery is inserted, the CPU is reset until the switch means is operated again, whereupon the read/write signal is again connected to the memory. EP 186832 A concerns apparatus for protecting memory data during interruptions to a non-battery main supply. The apparatus generates a reset signal in response to the main supply voltage dropping to the level where battery back-up is needed. The reset signal is gated with the memory enable signal to prevent spurious accesses during the supply interruption.

SUMMARY OF THE INVENTION

[0008] It is therefore an object of the present invention to provide a stored data protection apparatus for an electronic device having a computer, by which the stored data in a volatile memory of the device can be prevented from being destroyed when a main battery is replaced with a new one.

[0009] It is an object of a preferred embodiment of the present invention to provide a stored data protection apparatus in which stored data is prevented from being destroyed even when a replaced new main battery can not supply sufficient power, to a volatile memory, necessary for maintaining the stored data in the volatile memory.

[0010] According to the present invention, a stored data protection apparatus is provided for an electronic device having a CPU and a volatile memory controlled by the CPU for storing data therein. Both of the CPU and the volatile memory are supplied power voltage from a main battery in normal operation of the device. The volatile memory is supplied power voltage from a back-up battery when the main battery is removed from the device so as to prevent the data stored in the volatile
memory from being destroyed. The apparatus has a switch operable in first and second positions, taking the first position in the normal operation of the device, and being switched from the first position to the second position when the main battery is removed from the device, a circuit for inhibiting the CPU from accessing the volatile memory when the switch is in the second position, and a circuit for releasing the inhibition of the CPU by means of the inhibiting circuit when the switch is switched from the second position to the first position.

[0011] An embodiment of the apparatus according to the present invention may further have a first detection circuit for detecting that power supply voltage from the main battery is lower than a first predetermined voltage, and a release preventing circuit for preventing the releasing circuit from releasing the inhibition of the CPU when the first detection circuit detects that the supply voltage is lower than the first predetermined value.

[0012] In a preferred embodiment of the present invention having the above construction, the switch is interlocked with a main battery housing portion of the device (in which housing portion the main battery should be received), so that the switch is switched from the first position to the second position when the main battery is removed from the housing portion of the device, whereby the inhibiting circuit automatically inhibits the CPU from accessing the volatile memory in a condition in which the switch is switched to the second position. After completion of the replacement of the main battery with a new one, and after the switch has been switched from the second position to the first position, the releasing circuit releases the CPU from the inhibitory condition thereof by the use of a reset pulse.

[0013] In addition, in the preferred embodiment, the first detection circuit determines whether or not the supply voltage from the main battery is lower than the predetermined value. In case that the supply voltage of the main battery is higher than the predetermined value, as described above, the releasing circuit automatically releases the CPU from the inhibitory condition by the use of the reset pulse. In contrast with this, in case that the supply voltage of the main battery is lower than the predetermined value, the release preventing circuit inhibits the releasing circuit from performing its releasing operation of the CPU by blocking off the reset pulse.

[0014] Consequently, it is impossible without fail for the stored data protection apparatus of the present invention to protect the stored data stored in the volatile memory from being destroyed. Therefore, in the stored data protection apparatus of the preferred embodiment for the device, there is not fear that the stored data stored in the volatile memory means is destroyed even when the user sets the main battery (having been already exhausted) in the device by mistake.

[0015] It is preferable that the switch is kept in on state during a replacement operation of the main battery and in off state in normal operation of the device.

[0016] The switch is coupled to the CPU so as to cause a reset of the CPU when the switch then turns off.

[0017] The inhibiting circuit includes a circuit for preventing an enable signal applied from the CPU from being transmitted to the volatile memory when the switch is in the second position.

[0018] The above preventing circuit include a gate connected to the CPU to receive the enable signal therefrom and a flip-flop for keeping the gate closed when the switch is in the second position.

[0019] The releasing circuit includes a circuit for resetting the flip-flop when the switch is switched from the second position to the first position.

[0020] The resetting circuit includes a pulse generation circuit for producing a pulse signal when the switch is switched from the second position to the first position.

[0021] The above preventing circuit may include a second detection circuit for detecting that power supply voltage from the back-up battery is lower than a second predetermined voltage, and a circuit for blocking the flip-flop from being reset when the second detection circuit detects that the supply voltage is lower than the second predetermined value.

[0022] Further objects and advantages of the present invention will be apparent from the following description of the preferred embodiment of the present invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Figs. 1 and 2 schematically show electrical construction of an electronic device of a preferred embodiment according to the present invention; Fig. 3 shows electrical construction of a stored data protection apparatus of the device shown in Figs. 1 and 2; and Fig. 4 shows time charts of essential signals used in the stored data protection apparatus of Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0024] Hereinbelow, a preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings.

[0025] Figs. 1 and 2 are schematic block diagrams of an electronic device, for example such as electronic notebooks, pocket computers and the like, in which a stored data protection apparatus 28 of the present invention is incorporated.

[0026] As shown in these figures, a main battery 22 is so coupled with the electronic device as to supply power source voltage to a CPU (Central Processing Unit) 20 and like elements through a diode D1, which power source voltage is further supplied to a RAM (Random Access Memory) 21 through the diode D1 and a diode D2. On the other hand, a back-up battery 23 for prevent-
ing stored data from being destroyed is so coupled with the device as to supply its power source voltage to the RAM 21 through a diode D3. Consequently, the CPU 20 receives the power source voltage supplied from the main battery 22 to perform various control operations. On the other hand, the RAM 21 receives the power source voltage supplied from each of the main battery 22 and the back-up battery 23 to maintain the stored data therein.

[0027] As is clear from Figs. 1 and 2, the device having the stored data protection apparatus 28 of the present invention is further provided with a keyboard 24 for allowing an operator to input various data to the device, a display portion 25 for showing various data, a gate array 26 for producing various signals, and a ROM (Read Only Memory) 27 for storing various programs for the CPU 20, various dictionary data and the like data. As shown in Fig. 2, the main battery 22 supplies its power source voltage to each of the display portion 25, gate array 26 and the ROM 27.

[0028] The electronic device also has the stored data protection apparatus 28 which will be described in detail later, a switch 29 disposed at a housing portion of the device, in which the main battery 22 is received. This switch 29 is so operated as to turn on manually or preferably automatically when the operation of taking out the main battery 22 from the housing portion for replacing it with a new one is carried out. For example, the switch 29 may cooperate with a cover member of the housing portion for the main battery 22 so as to turn on when the cover member is opened.

[0029] The device is further provided with voltage detection circuits 30 and 31 which output L level (low level) detection signals to the stored data protection circuit 28, respectively, when the power source voltages supplied from the main battery 22 and the back-up battery 23 are lower than a predetermined voltage necessary for maintaining the data stored in the RAM 21.

[0030] Fig. 3 is a block diagram of an embodiment of the stored data protection apparatus 28 shown in Figs. 1 and 2. Hereinafter, the stored data protection circuit 28 will be described in detail with reference to this figure.

[0031] The voltage detection circuit 30 for detecting the power source voltage of the main battery 22 (shown in Figs. 1 and 2) outputs a detection signal to each of three-inputs NAND gates 32, 33, and 34. In this example of the stored data protection apparatus 28, a reset key 35 used for manually resetting the CPU 20, and an ON key 36 used for manually initiating operation of the CPU 20 are additionally provided. When the reset key 35 and the ON key 36 are turned on, the power supply voltage from the main battery 22 is led to the NAND gates 32 and 33, respectively.

[0032] When the switch 29 is turned on, the power source voltage from the main battery 22 is led, as an output signal of the switch 29, to each of the NAND gates 32, 33, and 34 through an inverter 37. On the other hand, at this time, a pulse generation circuit 38 produces a pulse signal and feeds it to the NAND gate 34. The output signal from the switch 29 is further fed to an OFF-signal input terminal (not shown) of the CPU 20. An output terminal of the NAND gate 33 is connected to an ON-signal input terminal (not shown) of the CPU 20, so that the CPU 20 is changed to an ON mode condition upon receipt of an output signal from the NAND gate 33.

[0033] The switch 29 is kept in off (open) state when the main battery 22 is not replaced. During the operation of taking out the main battery 22 from the housing portion for replacing it with a new one, the switch 29 is manually or preferably automatically turned on. For example, when the cover member of the housing portion is opened, it will be turned on and thus the power source voltage from the main battery 22 is fed from this switch 29.

[0034] Therefore, in normal operation of the device in which the main battery 22 is not replaced, the output signal from the switch 29 is at an L level. For replacement of the main battery 22, if the cover member of the housing portion is opened, the switch 29 is turned on to produce an output signal at an H level (high level). In other words, upon replacement of the main battery 22 with a new one, the output signal produced from the switch 29 is changed in level from the L level to the H level. Then, when the main battery 22 is removed from the housing portion of the device, the output signal from the switch 29 becomes on in the L level again even when the switch 29 remains in on state.

[0035] When a new main battery 22 is set in the housing portion of the device, the output signal from the switch 29 becomes on at the H level before the switch 29 is turned off. Then, after completion of setting of the main battery 22 in the housing portion of the device, and after the switch 29 is turned off, for example by closing the cover member, the output signal from the switch 29 becomes on in the L level.

[0036] An output terminal of the NAND gate 32 is connected to an input terminal of an OR gate 39 and an input terminal of an inverter 40. On the other hand, the output terminal of the NAND gate 34 is connected to the other input terminal of the OR gate 39 and an input terminal of an inverter 41. An output terminal of the OR gate 39 is connected to a reset terminal (not shown) of the CPU 20 for resetting itself in operation.

[0037] Output terminals of the inverters 40 and 41 are connected to a pair of input terminals of a NAND gate 42, respectively. An output terminal of the NAND gate 42 is connected to an input terminal of a NAND gate 43 which has its output terminal connected to a reset terminal R of a D flip-flop 44.

[0038] The detection signal outputted from the voltage detection circuit 31 for detecting the power supply voltage from the back-up battery 23 (shown in Figs. 1 and 2) is applied to one of input terminals of a NAND gate 46 having an output terminal connected to input terminals...
of NAND gates 43 and 47.

[0039] An input terminal D of the D flip-flop 44 is connected to a data bus DATA of the device. A clock terminal CK thereof is connected to an output terminal of the NAND gate 47 having an input terminal to which clock signals CLOCK are applied from the CPU 20. An output terminal Q of the flip-flop 44 is connected to the other input terminal of the NAND gate 46 and to an input terminal of an OR gate 48. To the other terminal of the OR gate 48, a chip-enable signal CE produced from the CPU 20 or the gate array 26 is applied. An output terminal of the OR gate 48 is connected to the RAM 21. The chip-enable signal CE disables the RAM 21 from operation at H level, and enables the RAM 21 at L level.

[0040] Fig. 4 is a timing chart of essential signals used in the stored data protection apparatus 28 shown in Fig. 3. Now, the embodiment of the present invention will be described in detail with reference to Fig. 4.

[0041] In the removal operation of the main battery 22 from the electronic device, first of all, the switch 29 is turned on so that the power source voltage of the main battery 22 is supplied to the stored data protection circuit 28, whereby an OFF signal is applied to the CPU 20 causing the CPU 20 to change in an OFF mode. Namely, as is clear from Fig. 3, immediately after the switch 29 is turned on, the OFF signal is applied to the CPU 20. After completion of the removal of the main battery 22 from the device, as shown in Fig. 4, the power supply from the main battery 22 gradually decreases to zero, to make it impossible to supply the power source voltage of the main battery 22 to the stored data protection circuit 28. As a result, as shown in Fig. 4, the output signal from the switch 29 becomes in the L level or in OFF mode.

[0042] Upon receipt of the OFF signal from the switch 29, the CPU 20 performs its OFF process so as to put the device in a stand-by mode. Namely, the CPU 20 outputs data DATA and clock signals CLOCK to the stored data protection circuit 28. In the circuit 28, the data DATA and clock pulses CLOCK are applied to the input terminal D and the clock terminal CK of the D flip-flop 44, respectively, to latch the flip-flop 44. Thus a signal being in the H level is outputted from the output terminal Q of the flip-flop 44. As a result, the output signal from the OR gate 48 is fixed in the H level regardless of the presence of the chip-enable signal CE from the CPU 20 or from the gate array 26, to prevent implementation of a write cycle for the RAM 21.

[0043] Incidentally, even when the main battery 22 is removed from the device, as shown by the arrow in Fig. 2, the back-up battery 23 supplies power source voltage to the RAM 21 in place of the main battery 22 to enable the RAM 21 to protect the stored data.

[0044] After the main battery 22 is removed from the device, the power source voltage supplied from the back-up battery 23 gradually decreases due to its backup service, so that a loss of power of the battery 23 is detected by the voltage detection circuit 31. As a result, an output signal from the detection circuit 31 changes in the L level, as shown in Fig. 4, causing an output signal of the inverter 45 to change in the H level. Consequently, the NAND gate 46 produces an output signal in the L level, so that both of the NAND gates 43 and 47 have output signals fixed in the H level. Thus, both of the clock signals CLOCK from the CPU 20 and the reset signal from the NAND gate 42 are blocked off to maintain the flip-flop 44 being latched.

[0045] After completion of the replacement of the main battery 22 with a new one, the new main battery 22 supplies the power source voltage, as shown in Fig. 4. Under such circumstance, when the switch 29 is turned off for example by closing the cover member of the housing portion, the output signal from the inverter 37 is switched from the L level to the H level, causing the pulse generation circuit 38 to produce a pulse.

[0046] Now, the operation will be divided into the following two modes depending upon whether or not the power source voltage supplied from the new main battery 22 is lower than a predetermined voltage necessary for implementation of proper operation of the device.

[0047] First, in case that the power source voltage of the new main battery 22 is higher than the predetermined value, as shown in Fig. 4. The output signal from the voltage detection circuit 30 becomes in the H level, so that the above pulse produced in the pulse generation circuit 38 is applied to the reset terminal R of the D flip-flop 44 through the NAND gate 34, inverter 41, NAND gate 42, and the NAND gate 43. In addition, a reset signal shown in Fig. 4 is applied to the reset terminal of the CPU 20 through the OR gate 39, so that the D flip-flop 44 is released from its latched mode and the CPU 20 is automatically reset, to allow the chip-enable signal CE from the CPU 20 or the gate array 26 to enter the RAM 21 through the OR gate 48. As is clear from the above description, even when the CPU 20 runs away during the replacement of the main battery 22, there is no fear that the stored data stored in the RAM 21 is destroyed, because the CPU 20 is automatically reset without fail.

[0048] On the other hand, in case that the power source voltage supplied from the new battery power pack 22 is lower than the predetermined value necessary for implementation of proper operation of the device, the output signal from the voltage detection circuit 30 becomes in the L level, so that the signals from the reset key 35 and the ON key 36 are blocked off together with the pulse from the pulse generation circuit 38 by means of the NAND gates 32, 33, and 34. Consequently, the D flip-flop 44 remains latched so that the chip-enable signal CE from the CPU 20 or the gate array 26 is blocked off by the OR gate 48. Namely, in case that the power source voltage of the new main battery 22 is lower than the predetermined value, it is impossible for the user to use the device, i.e., the chip-enable signal CE is blocked off so as to protect the
stored data stored in the RAM 21 from being destroyed. Therefore, even when the user sets the main battery 22 having been already exhausted in the device by mistake, there is no fear that the stored data of the RAM 21 is destroyed.

Claims

1. A stored data protection apparatus for an electronic device, said device having a CPU (20) and a volatile memory (21) which is controlled with an enabling signal from said CPU (20) for storing data therein, both of said CPU (20) and said volatile memory (21) being supplied power from a main battery (22) when said main battery (22) is connected in said device, and said volatile memory (21) being supplied power from a back-up battery (23) when said main battery (22) is removed from said device so as to prevent the data stored in the volatile memory (21) from being destroyed, said apparatus comprising:

- a switching means (29) operable between a first position and a second position, and taking the first position when said main battery (22) is connected in said device, and being switched from the first position to the second position prior to said main battery (22) being removed from said device;
- means (28) for supplying an off signal (OFF) to the CPU (20) when said switching means (29) is switched to the second position, said CPU supplying setting signals (DATA, CLOCK) to said stored data protection apparatus and shifting the device to a standby mode upon receiving said off signal;
- means (44, 48) for inhibiting said CPU (20) from accessing said volatile memory (21) in response to said switching means (29) being in the second position, including a gate means (48) connected to said CPU (20) for receiving said enabling signal from said CPU (20) and supplying the enabling signal to said volatile memory (21) when said switching means (29) is in the first position, and a flip-flop means (44) for preventing said gate means (48) from supplying said enabling signal to said volatile memory (21) when said switching means (29) is in the second position, said switching means (29) being switched from the second position to the first position, including a pulse generating means (38) for generating a reset pulse to be supplied to said flip-flop means (44) to reset said flip-flop means (44) and to said CPU (20) to reset said CPU (20) in response to said switching means (29) being switched from the second position to the first position.

2. An apparatus as claimed in claim 1, wherein said switching means (29) includes a switch being kept in an on state during a replacement operation of said main battery (22) and in an off state when said main battery (22) is connected in said device.

3. An apparatus as claimed in claim 1 or 2, wherein said means (38, 34, 41, 42, 43) for releasing includes logic means (32, 33, 34, 39) responsive to said reset pulse and being connected to said CPU (20) so as to reset said CPU (20) in response to said switch (29) being switched from the second position to the first position.

4. An apparatus as claimed in any one of claims 1 to 3, wherein said apparatus further comprises a first detection means (30) for detecting that power supply voltage from said main battery (22) is lower than a first predetermined voltage, and a release preventing means (34) for preventing said releasing means (38, 34, 41, 42, 43) from releasing said inhibition of said CPU (20) when said first detection means (30) detects that said power supply voltage is lower than said first predetermined voltage.

5. An apparatus as claimed in claim 4, wherein said inhibiting means further includes a second detection means (31) for detecting that power supply voltage from said back-up battery (23) is lower than a second predetermined voltage, and means (43) for preventing said flip-flop means (44) from being reset when said second detection means (31) detects that said power supply voltage is lower than said second predetermined voltage.

Patentansprüche

1. Vorrichtung zum Schutz von gespeicherten Daten für ein elektronisches Gerät mit einer zentralen Verarbeitungseinheit CPU (20) und einem flüchtigen Speicher (21), der mit einem Vorbereitungssignal von der CPU (20) gesteuert wird, um darin Daten zu speichern, wobei sowohl die CPU (20) als auch der flüchtige Speicher (21) von einer Hauptbatterie (22) mit Energie versorgt werden, wenn die Hauptbatterie (22) in dem Gerät angeklemt ist, und der flüchtige Speicher (21) von einer Pufferbatterie (23)
mit Energie versorgt, wenn die Hauptbatterie (22) von dem Gerät entfernt ist, um zu verhindern, dass die in dem flüchtigen Speicher (21) gespeicherten Daten gelöscht werden, wobei die Vorrichtung aufweist:

eine zwischen einer ersten Position und einer zweiten Position betätigungsfähige Schalteinrichtung (29) die die erste Position einnimmt, wenn die Hauptbatterie (22) in dem Gerät angeklemmt ist, und die von der ersten Position in die zweite Position geschaltet wird, bevor die Hauptbatterie (22) von dem Gerät entfernt wird;

eine Einrichtung (28) zum Zuführen eines Aus-Signals (AUS) an die CPU (20), wenn die Schalteinrichtung (29) in die zweite Position geschaltet ist, wobei die CPU Setzsignale (DATA, CLOCK) an die Vorrichtung zum Schutz von gespeicherten Daten zuführt und beim Empfang des Aus-Signals das Gerät in einen Bereitschaftsmodus schaltet;

1. Dispositif servant à protéger des données stockées, pour un appareil électronique, ledit dispositif ayant une unité centrale (20) et une mémoire volatile (21) qui est commandée par un signal de validation fourni par ladite unité centrale (20) pour y stocker des données, ladite unité centrale (20) et ladite mémoire volatile (21) étant toutes deux alimentées en électricité depuis une batterie principale (22) lorsque ladite batterie principale (22) est connectée dans ledit appareil, et ladite mémoire volatile étant alimentée en électricité par une batterie d’appoint (23) lorsque ladite batterie principale est retirée dudit appareil afin d’empêcher la destruction des données stockées dans la mémoire volatile (21), ledit dispositif comportant:

2. Vorrichtung nach Anspruch 1, bei der die Schalteinrichtung (29) einen Schalter umfaßt, der während eines Austauschvorgangs der Hauptbatterie (22) in einem Ein-Zustand gehalten ist, und der in einem Aus-Zustand gehalten ist, wenn die Hauptbatterie (22) in dem Gerät angeklemmt ist.

3. Vorrichtung nach Anspruch 1 oder 2, bei der die Einrichtungen (38, 34, 41, 42, 43) zum Freigeben Logikeinrichtungen (32, 33, 34, 39) umfassen, die auf den Rückstellimpuls ansprechend und die mit der CPU (20) verbunden sind, um die CPU (20) in Reaktion darauf, das der Schalter (29) von der zweiten Position in die erste Position geschaltet wird, rückzustellen.

4. Vorrichtung nach einem der Ansprüche 1 bis 3, mit einer ersten Erfassungseinrichtung (30) zum Erfassen, dass eine Energieversorgungsspannung von der Hauptbatterie (22) geringer als eine erste vorgegebene Spannung ist, und mit einer Freigabeverhinderungseinrichtung (34) zum Verhindern, dass die Freigabeeinrichtung (38, 34, 41, 42, 43) die Sperre der CPU (20) freigeben, wenn die erste Erfassungseinrichtung (30) erfaßt, dass die Energieversorgungsspannung geringer als die erste vorgegebene Spannung ist.

5. Vorrichtung nach Anspruch 4, bei der die Sperreseinrichtung weiter umfaßt: eine zweite Erfassungseinrichtung (31) zum Erfassen, dass eine Energieversorgungsspannung von der Pufferbatterie (23) geringer als eine zweite vorgegebene Spannung ist, und eine Einrichtung (43) zum Verhindern, dass die Flip-Flop-Einrichtung (44) rückgestellt wird, wenn die zweite Erfassungseinrichtung (31) erfaßt, dass die Energieversorgungsspannung geringer als die zweite vorgegebene Spannung ist.

Revendications
un moyen de commutation (29) actionnable entre une première position et une deuxième position, et prenant la première position lorsque ladite batterie principale (22) est connectée dans ledit appareil, et passant de la première position à la deuxième position avant que ladite première batterie (22) ne soit retirée dudit appareil;

un moyen (28) pour fournir un signal d'arrêt (OFF) à l'unité centrale (20) lorsque ledit moyen de commutation (29) passe dans la deuxième position, ladite unité centrale appliquant des signaux de mise à un (DATA, CLOCK) audit dispositif de protection de données stockées et mettant l'appareil en mode d'attente à la réception dudit signal d'arrêt;

un moyen (44, 48) pour empêcher ladite unité centrale (20) d'accéder à ladite mémoire volatile (21) en réponse au fait que ledit moyen de commutation (29) est dans la deuxième position, comprenant un moyen formant portillon électronique (48) connecté à ladite unité centrale (20) pour recevoir de ladite unité centrale (20) ledit signal de validation et appliquant le signal de validation à ladite mémoire volatile (21) lorsque ledit moyen de commutation (29) est dans la première position, et un moyen formant bascule (44) pour empêcher ledit moyen formant portillon (48) d'appliquer ledit signal de validation à ladite mémoire volatile (21) lorsque ledit moyen de commutation (29) est dans la deuxième position, ledit moyen formant portillon (48) étant connecté à ladite unité centrale (20) pour recevoir desdits signaux de mise à un (DATA, CLOCK) et pour être mis à un par lesdits signaux de mise à un fournis par ladite unité centrale (20) pour empêcher ledit moyen formant portillon (48) d'appliquer ledit signal de validation à ladite mémoire volatile (21), et un moyen (38, 34, 41, 42, 43) pour supprimer une interdiction d'accès de ladite unité centrale (20) à l'aide dudit moyen d'interdiction (44, 48) en réponse au passage dudit moyen de commutation (29) de la deuxième position à la première position, comprenant un moyen (38) générateur d'impulsion pour générer une impulsion de mise à deux à appliquer audit moyen formant commutateur à bascule (44) pour mettre à deux ledit moyen formant commutateur à bascule (44) et à ladite unité centrale (20) pour mettre à deux ladite unité centrale (20) en réponse au passage dudit moyen de commutation (29) de la deuxième position à la première position.

2. Dispositif selon la revendication 1, dans lequel ledit moyen de commutation (29) comporte un commutateur maintenu ouvert pendant une opération de remplacement de ladite batterie principale (22) et fermé lorsque ladite batterie principale (22) est connectée dans ledit appareil.

3. Dispositif selon la revendication 1 ou 2, dans lequel ledit moyen (38, 34, 41, 42, 43) de suppression d'interdiction comporte des moyens logiques (32, 33, 34, 39) réagissant à ladite impulsion de mise à zéro et connectés à ladite unité centrale (20) afin de mettre à zéro ladite unité centrale (20) en réponse au passage dudit commutateur (29) de la deuxième position à la première position.

4. Dispositif selon l'une quelconque des revendications 1 à 3, dans lequel ledit dispositif comprend en outre un premier moyen de détection (30) servant à détecter le fait que la tension d'alimentation électrique fournie par ladite batterie principale (22) est inférieure à une première tension prédéterminée, et un moyen d'empêchement (34) de suppression d'interdiction pour empêcher ledit moyen (38, 34, 41, 42, 43) de suppression d'interdiction de supprimer l'interdiction de ladite unité centrale (20) lors que ledit premier moyen de détection (30) détecte le fait que ladite tension d'alimentation électrique est inférieure à ladite première tension prédéterminée.

5. Dispositif selon la revendication 4, dans lequel ledit moyen d'interdiction comprend en outre un deuxième moyen de détection (31) servant à détecter le fait que la tension d'alimentation électrique fournie par ladite batterie d'appoint (23) est inférieure à une deuxième tension prédéterminée, et un moyen (31) pour empêcher la mise à zéro dudit moyen formant commutateur à bascule (44) lors que ledit deuxième moyen de détection (31) détecte le fait que ladite tension d'alimentation électrique est inférieure à ladite deuxième tension prédéterminée.
Fig. 4

POWER SUPPLY FROM MAIN BATTERY 22

OUTPUT OF SWITCH 29

Q OUTPUT OF FLIP-FLOP 44

OUTPUT OF DETECTION CIRCUIT 31

RESET SIGNAL

SWITCH 29 ON OFF-PROCESS

NORMAL OPERATION

REPLACEMENT OF MAIN BATTERY

CPU 20 RUNNING AWAY

SWITCH 29 OFF RESET-OPERATION

STORED DATA PROTECTED (FLIP-FLOP 44 LATCHED)