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(54) Method of manufacturing semiconductor devices
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Procédé de fabrication d’un dispositif semi-conducteur

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Description

[0001] The present invention relates to a method of manufacturing semiconductor devices according to the precharacterizing part of claim 1.

[0002] In a conventional semiconductor device manufacturing method, semiconductor devices having a large chip size are formed on semiconductor substrates utilizing the equal size projection technique, which is accomplished by the use of, for example, a reflection type projection exposure device. A reduction projection exposure device has not been used.

[0003] In conventional semiconductor devices, a single IC chip generally has a single major function, e.g., a microcomputer or memory function, because provision of a plurality of sufficient functions in a single IC chip increases the chip size greatly. Provision of an IC chip having a pattern containing a plurality of functions requires the reduction projection exposure technique which is capable of projecting an area larger than that which can be projected by one operation of the reduction projection exposure device. It is therefore impossible to form a circuit pattern in which a plurality of sufficient functions are formed in an area which can be projected by one exposure process step.

[0004] In recent years, the chip size has increased and the pattern size has become fine. Regarding this, the use of a reflection type projection exposure device arouses various problems. Such problems will be described in detail with reference to Fig. 1 which shows an example of a reflection type projection exposure device.

[0005] The reflection type projection exposure device has an optical system which includes a combination of concave mirror 11 and a convex mirror 12 and which employs an arcuate slit-shaped illumination 13. In this device, an image of the pattern on the mask 14 is transferred on the entire surface of the wafer 15 at a projection ratio of 1:1 by synchronously moving a mask 14 and a wafer 15 in the direction indicated by arrows A in Fig. 1. When it is desired to manufacture semiconductor devices having a large chip size, the mask pattern can be transferred onto the wafer 15 using a mask having a pattern whose size is the same as the chip size. This technique achieves resolution of about 2 μm. It is therefore very difficult to form a fine pattern having a design rule of, for example, 0.5 to 1.0 μm and thereby increase the integration density. Since alignment is conducted using alignment marks formed at the right and left sides of a wafer, alignment accuracy is limited to 3σ = 1.5 μm. With the reflection projection exposure device of the above-described type, it is therefore impossible to form fine patterns having a design rule of submicron.

[0006] In other words, the reflection type projection exposure device, which is used to form IC chips having a size which is the same as the mask size, cannot cope with the increasing demands for forming finer patterns in terms of the resolution and alignment accuracy.

[0007] Furthermore, when the above-described type of exposure device is used, distortion of the hardware deteriorates the degree of orthogonalization of a formed pattern and automatic alignment accuracy between the adjoining manufacturing processes is limited to 3σ = 1.5 μm. These preclude the exposure device from coping with formation of patterns having a design rule of submicron.

[0008] That is, when semiconductor devices having a large chip size are manufactured, the use of the reflection type projection exposure device has the following drawbacks.

1. Since the resolution achieved by the exposure device is 2.5 to 3.0 μm, it is impossible to form fine patterns having a design rule of, for example, 0.5 to 1.0 μm and thereby increase the integration density.
2. Distortion of the hardware deteriorates the degree of orthogonalization of the pattern.
3. Since automatic alignment accuracy between the processes is 3σ = 1.5 μm, it is impossible to cope with demands for forming fine patterns having a design rule of submicron.

[0009] To improve the resolution or alignment accuracy, a reduction projection exposure device may be used. As shown in Fig. 2 which illustrates an example of a reduction projection exposure device, in the reduction projection exposure device, the image of a pattern formed on a reticle is demagnified at a demagnification ratio inherent in a reduction projection lens 23 and projected onto a wafer 27. After the exposure of one shot, the wafer is moved or stepped on an XY stage 28, and the process is repeated. This step-and-repeat projection exposure technique achieves approximately 1.0 μm resolution. Since alignment is conducted after exposure of each shot, alignment accuracy of 3σ = 0.2 μm is achieved.

[0010] When semiconductor devices having a large chip size are formed using the reduction projection exposure device, it is considered to use a lens not having a demagnification ratio of 5:1 or 10:1 but a demagnification ratio of 2.5:1. In that case, the exposure area (field size) is practically 40 μm. This is because it is possible to increase the mask size but it is impossible to provide an optical system of the exposure device which is capable of projecting that mask image on a large exposure area without causing distortion or irregularities. It is therefore impossible to manufacture semiconductor devices having a chip size of 50 mm or more and having fine patterns by utilizing the conventional techniques.

[0011] According to document EP-A-0 358 567 there is disclosed a generic method of manufacturing semiconductor devices in which a plurality of unit patterns are repeatedly exposed in an adjoining arrangement. The plurality of unit patterns is obtained by dividing at least a part of a device pattern, wherein the unit patterns are connected in order to complete the part of the device
pattern on the substrate. The unit pattern lines of two adjoining unit patterns have a protrusion or protrusions extending in the extension direction of said pattern lines and the unit patterns are exposed such that the protrusions are overlapped with each other.

[0012] According to document JP-A-62 125 620, there is disclosed a method of manufacturing semiconductor devices, according to which the pattern is split to form two photo masks. The substrate is then repeatedly exposed with the first photo mask to form first exposure patterns and the second photo mask to form second exposure patterns, wherein the first and second patterns are connected on the substrate. Special measures for connecting the divided patterns are not provided.

[0013] It is the object of the present invention to provide a method of manufacturing semiconductor devices by means of which a line disconnection or separation disability in the patterns can be avoided.

[0014] An aim of the present invention is to provide a method of manufacturing semiconductor devices which is capable of manufacturing large semiconductor devices that cannot be manufactured using the aforementioned conventional techniques.

[0015] The method of manufacturing semiconductor devices according to the invention is to be capable of forming a desired pattern having an area size larger than the field size that can be obtained in one exposure process step of an exposure device by dividing the desired pattern into a plurality of portions and then by conducting exposure on the divided patterns in a joined fashion.

[0016] An aim of the present invention is to provide a method of manufacturing semiconductor devices which is capable of forming on a semiconductor substrate a desired pattern having an area size larger than the field size that can be projected in one exposure process step of a reduction projection type exposure device by repeating the process of projecting a circuit pattern on the semiconductor substrate using the reduction projection type exposure device and thereby sequentially joining the circuit patterns with each other.

[0017] Another aim of the present invention is to provide a method of manufacturing semiconductor devices which is capable of forming on a semiconductor substrate a desired pattern having an area size larger than the field size that can be projected in one exposure process step of a reduction projection exposure device by repeating the process of projecting a circuit pattern on the semiconductor substrate using the reduction projection type exposure device while sequentially connecting the projected patterns with each other. The connecting portion between the adjacent circuit patterns is double projected to form a double exposure area.

[0018] According to the present invention a method of manufacturing semiconductor devices is to be provided in which a desired pattern having an area size larger than the field size that can be projected in one exposure process step of a reduction projection type exposure device is formed on a semiconductor substrate by repeating the process of projecting a circuit pattern on the semiconductor substrate using the reduction projection type exposure device while sequentially connecting the projected patterns with each other. At least part of the connecting portion is disposed in a device separating area of the semiconductor device.

[0019] Another aim of the present invention is to provide a method of manufacturing semiconductor devices which is capable of forming on a semiconductor substrate a desired pattern having a size larger than the field size that can be projected in one exposure process step of a reduction projection type exposure device by repeating the process of projecting a circuit pattern on the semiconductor substrate using the reduction projection type exposure device while sequentially connecting the projected patterns with each other. At least part of the connecting portion is present in a device separating area of the semiconductor device.

[0020] Another aim of the present invention is to provide a method of manufacturing semiconductor devices which is capable of forming on a semiconductor substrate a desired pattern having a size larger than the field size that can be projected in one exposure process step of a reduction projection type exposure device by repeating the process of projecting a circuit pattern on the semiconductor substrate using the reduction projection type exposure device while sequentially connecting the projected patterns with each other. In a plurality of exposure operations, at least one exposure process step is conducted using a reflection projection, proximity or contact exposure device.

[0021] In the present invention, when a desired pattern is formed, an exposure process step is conducted a plurality of times using patterns obtained by dividing the desired pattern into a plurality of areas, by means of which the divided patterns are connected to form the desired pattern.

[0022] Therefore, patterns having a larger area than the effective area of the pattern can be formed, and fine patterns can be formed utilizing the reduction projection exposure technique.

[0023] Furthermore, if patterning of the divided patterns is devised, patterns having any size can be formed using less number of masks or divided patterns by repeating exposure using the same divided patterns.

[0024] Furthermore, when the connecting portion between the divided patterns corresponds to a device separating or non-forming area, offsets between the divided patterns do not affect the characteristics of the formed device. This increases yield.

[0025] Offsets between the divided patterns which would occur during exposure can be compensated for by slightly overlapping the divided patterns.

[0026] The desired pattern may be divided according to the function. In that case, changes in the specifications of the individual functions can be readily coped with. Also, division of the desired pattern according to the function readily precludes formation of a device over
the divided patterns.

[0027] Division of the pattern is conducted only when necessary. If a sufficient patterning accuracy can be obtained in a sufficiently large patterning area, it is not necessary to divide the pattern.

[0028] The object of the invention is achieved by means of the combination of the features defined in claim 1. Preferable embodiments of the invention are set forth in the subclaims. In the following the invention is further illustrated by an embodiment with reference to the attached drawings.

Fig. 1 is a schematic perspective view illustrating one example of a reflection type projection exposure device;

Fig. 2 is a schematic perspective view illustrating one example of a reflection type projection exposure device;

Figs. 3, 6, 7, 10, 11, 24, 28, 30 and 31 respectively show the pattern of a first layer on a wafer;

Figs. 4, 5, 8, 9, 23, 25, 27, 29A, 29B, 32 and 33 respectively show the pattern of a reticle (mask);

Figs. 12A and 12B respectively show a reticle described in the embodiment of the present invention; Fig. 12C shows the pattern formed using the reticles shown in Figs. 12A and 12B;

Fig. 13 is a graph showing the relationship between the amount of exposure and the line width.

[0029] Fig. 3 shows a schematic pattern of a first layer on a semiconductor substrate, showing a method of manufacturing semiconductor devices. Fig. 4 shows a schematic pattern of a first reticle 105 used in a 5 : 1 reduction projection exposure device for forming the first layer, and Fig. 5 is a schematic pattern of a second reticle 106 used to form a second layer.

[0030] The first reticle 105 contains three divided patterns A, B and C. Each of these patterns represents an IC pattern. In this example, the patterns A, B and C are joined to each other in the vertical direction to form a single chip.

[0031] The first reticle 105 shown in Fig. 4 is set in the generally used 5 : 1 demagnification projection exposure device, and then the layout of the first layer on the semiconductor substrate 101 (hereinafter referred to as a wafer 101) is programmed by the system attached to the device such that the pattern shown in Fig. 3 can be projected onto the wafer 101. The joining accuracy between the actually exposed patterns A, B and C is 0.1 μm or less in both vertical and horizontal directions. This joining accuracy can be achieved by positioning the patterns utilizing the laser interferometer of the reduction projection exposure device. During the exposure, it is desired that the patterns A and B or the patterns B and C be laid on top of the other at each jointed portion over 0.1 to 0.5 μm. This is readily achieved by changing the step size of the reduction projection exposure device.

[0032] Alignment marks 103 shown in Fig. 4 are alignment marks used for the die by die method. After the exposure, the alignment marks 103 are present on the two sides of each of the joined patterns A, B and C on the semiconductor substrate, as shown in Fig. 3, and serve as alignment marks (parent marks) 102 for the second layer. When the first layer is projected using the first reticle 105, the position of a masking blade of the reduction projection exposure device is changed for each shot (pattern A, B or C) to cover the patterns other than the projected pattern. For example, when the pattern A is projected, the other patterns B and C are covered by the blade so that no light reaches them. Patterns B and C are projected in the same manner.

[0033] After the patterns A, B and C are formed, normal semiconductor manufacturing processes are conducted using the formed pattern, such as etching, diffusion of impurities or deposition of a chemical vapor deposition film, and then the second layer is patterned.

[0034] The second layer is formed using the second reticle 106 shown in Fig. 5 by aligning the alignment marks 102 formed in the first layer as the parent marks to alignment marks 104 which serve as the child marks. That is, pattern A' is aligned to the pattern A, pattern B' is aligned to the pattern B. When the patterns A', B' and C' are projected, the position of the masking blade is changed for each shot as in case of the first layer.

[0035] The above-described patterning operation is repeated a required number of times with introduction of impurities and metal interconnection being conducted after patterning of each layer to form ICs having a chip size of 3.5 mm x 60 mm on a design rule of 0.8 μm.

[0036] Fig. 6 schematically shows the pattern of a first layer on the semiconductor substrate 101 which is used in a method of manufacturing semiconductor devices.

[0037] In this example, the pattern B located in the middle of the IC pattern formed in the first embodiment by connecting three types of patterns A, B and C is projected repeatedly as patterns B1 and B2 so as to make the length of the chip size longer than that of the chip size in the first embodiment. A desired number of intermediate patterns B1 and B2 can be joined. This enables manufacture of semiconductor devices having various lengths.

[0038] In this example, three types of patterns A, B and C are joined to form a single chip. Two or four types of them may also be used.

[0039] Furthermore, the number of reticles used in a single process is not limited to one but two or more types of reticles may be used exchangeably.

[0040] Fig. 7 schematically shows how a first layer is patterned on a semiconductor substrate in a further example of a method of manufacturing semiconductor devices, Fig. 8 shows a first reticle 105 used in a 5 : 1 reduction projection exposure device to form the first layer, and Fig. 9 shows a second reticle 106 used to form a second layer.

[0041] As in the case of the first example, the first reticle 105 shown in Fig. 8 is set in the exposure device,
and then the layout of the first layer on the wafer 101 is programmed in the exposure device using the system attached thereto such that the pattern shown in Fig. 7 can be projected onto the wafer 101 which serves as the semiconductor device. In this example, the joining accuracy between the patterns A and B or the patterns B and C is 0.1 µm or less in both vertical and horizontal directions, as in the previous examples. Alignment marks 103 shown in Fig. 8 are alignment marks used for the die by die method. The alignment marks 103 are present on the two sides of each of the patterns B in the patterns A, B and C, as shown in Fig. 7, and serve as the alignment marks (parent marks) 102 for the second layer.

[0042] When the first layer is projected using the first reticle 105, the position of the masking blade of the reduction projection exposure device is changed for each shot. In this example, four of the patterns B alone are formed separately from other patterns on the periphery of the semiconductor substrate. Also, in the first and second reticles 105 and 106 shown in Figs. 8 and 9, the position of the patterns A and C relative to the pattern B is known.

[0043] Next, the second layer is formed using the second reticle 106 shown in Fig. 9 by aligning the alignment marks 102 formed in the first layer as the parent marks to the alignment marks 104 serving as the child marks. This alignment conducted in the third example differs in the manner described below from that performed in the aforementioned first and second examples.

(1) When the alignment marks 102 are aligned to the alignment marks 104 to form the second layer, only eight patterns B shown in Fig. 7 are scanned using a laser to measure offsets between the eight patterns B which constitute eight chips.

(2) The thus-obtained measured values are operated to calculate how much the alignment marks 102 are offset from the alignment marks 104 in X, Y and 0 directions in the patterns B.

(3) The offsets in the eight patterns B are averaged.

(4) The patterns A', B' and C' are moved by the obtained averaged offset and then projected. Stage accuracy alone of the XY stage of the reduction projection exposure device is utilized to achieve projection.

[0044] Thus, the pattern A' is projected over the pattern A, and the pattern B' is projected on top of the pattern B. When the patterns A, B' and C' are exposed, the position of the masking blade is changed in the manner described in the first layer.

[0045] With the aforementioned alignment technique, the joining accuracy between the patterns A' and B' or between the patterns B' and C' can be improved as compared with that achieved in the first and second examples. Whereas joining accuracy in the first and second examples is 3σ = 0.23 µm, joining accuracy of 3σ = 0.20 µm is achieved in the third examples.

[0046] Fig. 10 shows the pattern of a first layer on a wafer used in an embodiment of the present invention.

[0047] In this embodiment, the first reticle is set, and then the layout of the first layer on the wafer 101 is programmed so that the pattern shown in Fig. 10 can be formed, as in the case of the third embodiment. However, the embodiment is different from the third example in that alignment is performed using the normally formed pattern (in this embodiment, the pattern B is used) without using the dedicated patterns exclusively used for alignment formed on the periphery of the wafer. Like the third example, this embodiment achieves joining accuracy of 3σ = 0.20 µm between the patterns A' and B' or between the patterns B' and C'.

[0048] In both third example and the embodiment of the invention, three types of patterns A, B and C are joined to form a single chip. However, the number of patterns to be joined may be two, four or above.

[0049] Furthermore, the number of reticles used in a single process is not limited one but two or more types of reticles may also be used exchangeably.

[0050] The aforementioned overlapping will be described below in detail.

[0051] Although projection of the individual patterns can be made without providing the overlapped portion between the adjacent patterns, provision of the overlapped portion according to the invention is desired to achieve an improved accuracy or yield.

[0052] Fig. 11 illustrates how the individual patterns are overlapped. In Fig. 11, the patterns A, B and C are joined to each other on the substrate with an overlapped portion 230 formed between the adjacent patterns by overlapping part of one pattern on part of the other. Figs. 12A and 12B respectively show the reticles used to form the connecting portion 230. A remaining pattern 233 located at one end of a pattern 232 made of chromium and formed on a glass plate 231 has wide portions 234. The remaining pattern 233 located at one end of the reticle A (Fig. 12A) is projected such that it overlaps a remaining pattern 233' located at one end of a reticle B (Fig. 12B), as shown in Fig. 12C.

[0053] In this example, since projection is conducted using the 5 : 1 reduction projection exposure device, the ratio between the pattern on the reticle to the pattern on the substrate is 5 : 1. Therefore, a length ℓ and a width W₀ of the remaining pattern 233 on the reticle are respectively reduced to a length ℓ and a width W₁ on the substrate. A width 5W of the wide portions 234 is expressed by 5W = 5W₁ - 5W₀ as shown in Fig. 12A, where W₀ is the width of the formed chromium pattern.

[0054] Fig. 13 shows the relationship between the amount of exposure and the line width. As shown in Fig. 13, since the connecting portion 230 is double exposed, this double exposed area is thinner than the other portion by ΔCD. To compensate for this, the remaining patterns 233 and 233' are formed wider beforehand. ℓ and w of the remaining pattern 233 or 233' are calculated in
the manner described below. That is, assuming that joining accuracy in the Y direction in the used exposure device is

$$X + 3\sigma$$

and that the difference between the line width $CD_{EX}$ at the amount of exposure $EX$ and the line width $CD_{2EX}$ at the amount of exposure $2EX$ is

$$\Delta CD = CD_{EX} - CD_{2EX}$$

$$\ell = \frac{1}{2} (|X| + 3\sigma)$$

$$w = \frac{1}{2} \Delta CD$$

It was found from the measurements that joining accuracy was

$$\bar{X} = 0.09 \mu m$$

$$3\sigma = 0.23 \mu m$$

and that, at the amount of exposure of 68 mJ/cm²,

$$\Delta CD = 0.20 \mu m.$$ 

Therefore, $\ell = 0.16 \mu m$ and $w = 0.10 \mu m$. Since the address size of the reticle is $0.25 \mu m$, $\ell$ is converted to the multiple of $0.05 \mu m$ as follows:

$$\ell = 0.20 \mu m,$$ and $w = 0.10 \mu m$

[0055] Overlapping exposure was conducted using the reticles having the aforementioned dimensions to form IC chips having dimensions of 3.1 mm x 54 mm on a design rule of $0.7 \mu m$.

[0056] The reason why the connecting portion 230 is provided is that when offsets between the patterns occur, line disconnection or separation disability may occur in the patterns. Provision of the connecting portion 230 can overcome this problem.

[0057] In this example, $\ell = 0.2 \mu m$ and $w = 0.1 \mu m$. However, $\ell$ and $w$ are not limited to these values but they may in general be set between $0.1$ and $0.5 \mu m$ and between $0.05$ and $0.2 \mu m$, respectively. Furthermore, in this example, the circuit patterns are one-dimensionally joined. The patterns may also be joined two-dimensionally or in any other manner as long as it does not change the scope of the present invention.

[0058] As will be understood from the foregoing description, in the present invention, circuit patterns are projected on the same semiconductor substrate in a joined fashion using the reduction projection exposure device. Therefore, the present invention has the following advantages:

1. It is possible to manufacture IC chips having a chip size larger than the field size of the reduction projection exposure device.

2. It is possible to form the patterns in an IC chip on a submicron rule. An alignment accuracy of $3\sigma = 0.2 \mu m$ or less can be achieved between the adjacent IC chip fabrication steps.

3. Manufacture of large-area and highly integrated ICs is made possible without increasing production costs.

[0059] Furthermore, since the circuit patterns are projected in a state where they are sequentially connected with each other, the area of the pattern can be increased in proportion to the number of exposure processes and is not limited to the field size of the reduction projection exposure device.

[0060] Furthermore, since the overlapping portion is provided between the patterns, even when the patterns are not connected properly, occurrence of failures, such as disconnection of the patterns or separation disability, can be reduced.

[0061] Furthermore, a combination of a plurality of separate ICs can be fabricated into a single IC. Therefore, production cost can be reduced, and reliability of the manufactured ICs can be improved.

[0062] Furthermore, the connecting portion of the patterns exists in the device separating area or non device forming area. It is therefore possible to prevent deterioration in the characteristics of the semiconductor devices or reduction in the yield.

[0063] Throughput can be improved and reduction in the production cost can be achieved by adequately selecting the exposure method.

**Claims**

1. A method of manufacturing semiconductor devices in which a desired pattern having an area size larger than the field size that can be obtained in one exposure process step of an exposure device is formed, comprising the step of exposing, wherein the exposed area is divided into plural sections so that a first pattern (A) for a first wiring section to be exposed in a first exposing process step is overlapped with a second pattern (B) for an adjacent second wiring section to be exposed in a second exposing process step, thus forming an overlapping portion (230) connecting said first and second patterns (A, B)
characterized in that said patterns (A, B) are exposed, so that the width \(5W_w\) of one end (233, 234; 233', 234') of a reticle pattern for forming the overlapping portion (230) is made broader than a width \(5W_d\) of the reticle pattern portions (232; 232') continuous therewith.

2. The semiconductor device manufacturing method according to claim 1, wherein the overlapping portion (230) corresponds to a device separating area of the semiconductor device.

3. The semiconductor device manufacturing method according to claim 1, wherein the first and second patterns (A, B) are the same.

4. The semiconductor device manufacturing method according to claim 1, wherein the first and second patterns (A, B) are different.

5. The semiconductor device manufacturing method according to claim 1, wherein the first and second patterns (A, B) are formed in the same mask.

6. A semiconductor device manufacturing method according to claim 1, wherein at least a part of the exposure process step is performed by an exposing apparatus selected from a reflection type projecting exposure apparatus, a short range exposing apparatus and a contact exposing apparatus.

**Revidendations**

1. Procédé pour fabriquer des dispositifs à semi-conducteurs, dans lequel un motif désiré ayant une taille de surface supérieure à la taille de champ qui peut être obtenue dans une étape de processus d'exposition d'un dispositif d'exposition est formé, comprenant l'étape d'exposition, à l'intérieur de laquelle la surface exposée est divisée en plusieurs sections de telle sorte qu'un premier motif (A) pour une première section de câblage devant être exposé au cours d'une première étape de processus d'exposition soit chevauché par un deuxième motif (B) pour une deuxième section de câblage adjacente devant être exposée au cours d'une deuxième étape de processus d'exposition, de façon à former par conséquent une partie de chevauchement (230) connectant lesdits premiers et deuxièmes motifs (A, B),

caractérisé en ce que :

lesdits motifs (A, B) sont exposés, de telle sorte que la largeur \(5W_w\) d'une extrémité (233, 234 ; 233', 234') d'un motif de réticule pour former la partie de chevauchement (230) soit rendue plus large que la largeur \(5W_d\) des parties de motif de réticule (232 ; 232') qui sont continues avec celle-ci.

2. Procédé de fabrication de dispositif à semi-conducteurs selon la revendication 1, dans lequel la partie de chevauchement (230) correspond à une surface de séparation de dispositifs du dispositif à semi-conducteurs.
3. Procédé de fabrication de dispositif à semi-conducteurs selon la revendication 1, dans lequel les premier et deuxième motifs (A, B) sont identiques.

4. Procédé de fabrication de dispositif à semi-conducteurs selon la revendication 1, dans lequel les premier et deuxième motifs (A, B) sont différents.

5. Procédé de fabrication de dispositif à semi-conducteurs selon la revendication 1, dans lequel les premier et deuxième motifs (A, B) sont formés dans le même masque.

6. Procédé de fabrication de dispositif à semi-conducteurs selon la revendication 1, dans lequel au moins une partie de l'étape de processus d'exposition est effectuée à l'aide d'un dispositif d'exposition sélectionné parmi un dispositif d'exposition à projection du type à réflexion, un dispositif d'exposition à courte distance et un dispositif d'exposition à contact.