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• BRÜEL & KJERSER TECHNICAL REVIEW, no. 2, 1972, Denmark, page 16; J.Austin Hansen:
"RMS-Rectifiers"

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to signal level detecting circuits for detecting levels of analog signals, and more particularly, to a circuit for detecting the level of an analog signal, such as a variable control signal, and producing a detected output signal which can be digitally processed.

Description of Related Art

In a previously proposed circuit for detecting the level of an analog signal and for producing a detected output signal which is formed so as to be digitally processed, it is customary that the analog signal which has a level that is to be detected is subjected to an analog-to-digital (A/D) conversion so as to produce a digital signal which corresponds thereto and the level of the analog signal is indirectly detected based on the digital signal obtained by the A/D conversion. For example, in the case where the brightness of the display of a fluorescent display tube which is used in an electronic apparatus and which is driven by a digitalized driving circuit that is controlled by an analog control signal, the level of the analog control signal is indirectly detected in such a manner that the analog control signal is subjected to an A/D conversion so as to produce a digital signal which corresponds to the level of the analog control signal, and the digital signal obtained during the A/D conversion is supplied to the digitalized driving circuit so as to carry out the brightness control for the fluorescent display tube.

In such a case, it is usual that the A/D conversion is carried out by an A/D converter formed as an integrated circuit and the A/D converter employed in conventional consumer product electronic apparatus is commonly a microcomputer of, for example, the eight bit type.

In the case where the A/D converter contained in the microcomputer of the eight bit type is used for detecting the level of the analog control signal, it is possible that the number of conversion steps for digitalization are insufficient for a sufficient range of level variations in the analog control signal and therefore the level of the analog control signal will be detected with insufficient accuracy. If such insufficiency in the number of conversion steps for digitalization results in the brightness control for a fluorescent display tube, the brightness of the display on the fluorescent display tube does not change smoothly in accordance with variations in the level of the analog control signal but will have unnatural sudden changes in response to the variations in the level of the analog control signal.

For avoiding such a problem, it is considered to use an A/D converter which has more than eight bit numbers for the A/D conversion of the analog control signal. However, A/D converters with more than eight bit numbers require a large number of electronic elements and parts which results in complicated and expensive devices.

From BRÜEL & KJER TECHNICAL REVIEW. no. 2, 1972, Denmark, page 16; J. Austin Hansen; "RMS-Rectifiers", a level comparator is known, which takes different output values in dependence on whether or not a variable input exceeds a reference signal. However, this known level comparator does not generate signals indicating the time periods in which a variable input does or does not exceed the reference signal.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a signal level detecting circuit which is operative to detect the level of an analog signal and to produce a detected output signal which is applicable to a digital processing circuit, which avoids the aforementioned problems and disadvantages encountered with the prior art.

Another object of the present invention is to provide a signal level detecting circuit operative to detect the level of an analog signal and to produce a detected output signal which is applicable to a digital processing circuit, in which the level of the analog signal is accurately detected and which has a relatively simple and inexpensive configuration.

A further object of the present invention is to provide a signal level detecting circuit operative to detect the level of an analog signal and to produce a detected output signal which is applicable to a digital processing circuit, in which the level of the analog signal is accurately detected without an A/D converter which has more than eight bits for the A/D conversion of the analog signal.

Circuits in accordance with the present invention have the features shown in appended claim 1 or claim 2.

According to the present invention, there is provided a signal level detecting circuit comprising an input terminal to which an input signal with level variations is applied. A level comparator having first and second input terminals is supplied with the input signal and a reference signal, respectively, and is operative to produce a first comparison output signal which has a first level during first periods of time wherein the level of the input signal is equal to or lower than the level of the reference signal and a second level during periods of time other than the first periods of time or to produce a second comparison output signal which has a first level during second periods of time wherein the level of the input signal is equal to or higher than the level of the reference signal and the second level during periods of time other than the second periods of time. A control signal generator is operative to detect the first or second period of time and to produce a first control signal when the detected first or second period of time is shorter than a first ref-
ference period of time and a second control signal when the detected first or second period of time is longer than a second reference period of time which is selected to be longer than the reference period of time of or to produce a third control signal when the detected first or second period of time is longer than a third reference period of time and a fourth control signal when the detected first or second period of time is shorter than a fourth reference period of time which is selected to be shorter than the third reference period of time. A pulse generator is operative to produce a pulse signal having a period determined based on a predetermined clock signal and a pulse duty factor arranged to be variable during a given period of time at regular intermittent intervals, to increase or decrease the pulse duty factor of the pulse signal whenever the first or third control signal is obtained from the control signal generator and to decrease or increase the pulse duty factor of the pulse signal whenever the second or fourth control signal is obtained from the control signal generator. An integrator is operative to produce an integrated output signal based on the pulse signal obtained from the pulse generator during the given period of time and to supply the second input terminal of the level comparator with the integrated output signal as the reference signal.

In the signal level detecting circuit thus constituted in accordance with the present invention, the integrated output signal which is supplied to the second input terminal of the level comparator as the reference signal has its level varied in response to variations in the pulse duty factor of the pulse signal obtained from the pulse generator during the given period of time. The first period of time in which the first comparison output signal obtained from the level comparator has the first level or the second period of time in which the second comparison output signal obtained from the level comparator has the first level is varied in its length in response to level variations of the input signal compared with the level of the integrated output signal.

Whenever the level of the input signal applied to the input terminal increases so that the first period of time wherein the first comparison output signal has the first level or the second period of time wherein the second comparison output signal has the first level is shorter than the reference period of time and thereby the first control signal is obtained from the control signal generator, the pulse duty factor of the pulse signal obtained from the pulse generator is increased or decreased and thereby the level of the integrated output signal which is supplied to the second input terminal of the level comparator is increased, so that the first period of time or the second period of time is varied to be longer than the reference period of time of, and whenever the level of the input signal applied to the input terminal decreases so that the first period of time wherein the first comparison output signal has the first level or the second period of time wherein the second comparison output signal has the first level is longer than the second reference period of time which is selected to be longer than the first reference period of time and thereby the second control signal is obtained from the control signal generator, the pulse duty factor of the pulse signal obtained from the pulse generator is decreased or increased and thereby the level of the integrated output signal supplied to the second input terminal of the level comparator is decreased, so that the first period of time or the second period of time is varied so as to be shorter than the second reference period of time.

Otherwise, whenever the level of the input signal applied to the input terminal increases so that the first period of time wherein the first comparison output signal has the first level or the second period of time wherein the second comparison output signal has the first level is longer than the third reference period of time and thereby the third control signal is obtained from the control signal generator, the pulse duty factor of the pulse signal obtained from the pulse generator is increased or decreased and thereby the level of the integrated output signal supplied to the second input terminal of the level comparator is increased, so that the first period of time or the second period of time is varied so as to be shorter than the third reference period of time, and whenever the level of the input signal applied to the input terminal decreases so that the first period of time wherein the first comparison output signal has the first level or the second period of time wherein the second comparison output signal has the first level is shorter than the fourth reference period of time which is selected to be shorter than the third reference period of time and thereby the fourth control signal is obtained from the control signal generator, the pulse duty factor of the pulse signal obtained from the pulse generator is increased or decreased and thereby the level of the integrated output signal supplied to the second input terminal of the level comparator is decreased, so that the first period of time or the second period of time is varied so as to be longer than the fourth reference period of time.

With the operation as described above, the first or third control signal is obtained from the control signal generator in response to an increase of the level of the input signal and the second or fourth control signal is obtained from the control signal generator in response to a decrease of the level of the input signal. These first and second control signals or third and fourth control signals are produced by detecting the level of the input signal at a large number of level steps as the detected output signals which are applicable to the digital processing circuit.

In such a manner as aforementioned, the level of the input signal applied to the input terminal is accurately detected to produce the detected output signal which is applicable to the digital processing circuit with relatively simple and inexpensive configurations without using an A/D converter which has more than eight bits for carrying out the A/D conversion of an analog signal.

The above, and other objects, features and advan-
tages of the present invention will become apparent from the following detailed description which is to be read in conjunction with the accompanying drawings.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a schematic block diagram showing an embodiment of the signal level detecting circuit according to the present invention, together with a display device to which the embodiment is applied; and FIGS. 2, 3, 4A, 4B, 4C and 5 are waveform diagrams used for explaining the operation of the embodiment shown in FIG. 1.

**DESCRIPTION OF THE PREFERRED EMBODIMENTS**

FIG. 1 shows an embodiment of signal level detecting circuit according to the present invention and a display device to which the embodiment is applied.

Referring to FIG. 1, the display device comprises a fluorescent display tube 1 and a control unit 3 which includes a driving signal generator 2 operative to supply the fluorescent display tube 1 with a driving signal 5d to control the brightness of the display of a plurality of fluorescent elements provided in the fluorescent display tube 1.

The control unit 3 also includes a control signal generator 11 and a pulse generator 13 which constitute a part of the embodiment of the signal level detecting circuit according to the present invention, and further a clock generator 15 which supplies the control signal generator 11 with a clock signal 5c1 and also supplies both the driving signal generator 2 and the pulse generator 13 which are in the control unit 3 with a clock signal 5c2. The control signal generator 11 comprises a counter 17 to which the clock signal 5c1 is supplied and a counted result detector 19 to which a count output Co from the counter 17 is supplied. The counted result detector 19 is operative to detect a counted result represented by the count output Co from the counter 17. The counter 17 supplies both the driving signal generator 2 and the pulse generator 13 with a first control signal 5xu or a second control signal 5xd as the output signal from the control signal generator 11.

A buffer amplifier 23 comprising a transistor 21 connected to a voltage source +B, an integrator 29 comprising a resistor 25 with one end connected to the transistor 21 and a capacitor 27 connected between the other end of the resistor and a reference potential point, and a level comparator 31, which constitute a part of the embodiment of the signal level detecting circuit according to the present invention, are connected to the control unit 3. An input terminal of the buffer amplifier 23 is coupled through a terminal 5 to an output terminal of the pulse generator 13. An output terminal of the buffer amplifier 23 is coupled to an input terminal of the integrator 29. An output terminal of the integrator 29 is coupled to a reference input terminal of the level comparator 31. An output terminal of the level comparator 31 is coupled through a terminal 4 to the counter 17 in the control signal generator 11. Further, a comparing input terminal of the level comparator 31 is coupled to an input terminal 33 to which an external control signal Sc which has level variations is applied as the input signal.

The pulse generator 13 in the control unit 3 supplies the buffer amplifier 23 with a pulse signal 5w through the terminal 5. As shown in FIGS. 2 and 3, the pulse signal 5w has a given period tp based on the clock signal 5c2 from the clock generator 15 and a variable pulse duty factor defined by td/tp x 100(%) and is produced during a given period of time Tw at regular intermittent intervals corresponding to a given period Tt. The pulse signal 5w supplied to the buffer amplifier 23 is inverted in polarity to become a pulse signal 5w' which is supplied to the integrator 29 from the output terminal of the buffer amplifier 23.

In the integrator 29, the pulse signal 5w' obtained in each period of time Tw is integrated to produce an integrated output signal Sw which is supplied to the reference input terminal of the level comparator 31. As shown in FIG. 4A, the integrated output signal sw has a level which increases exponentially during the period Tw and then decreases exponentially after the period Tw. The level of the integrated output signal Sw increases as the pulse duty factor of the pulse signal 5w increases.

The external control signal Sc is supplied to the comparing input terminal of the level comparator 31. In the level comparator 31, the level of the external control signal Sc is compared with the level of the integrated output signal Sw and a comparison output signal Po which has a high level when the level of the external control signal Sc is equal to or lower than the level of the integration output signal Sw and a low level when the level of the external control signal Sc is higher than the level of the integration output signal Sw, is obtained at the output terminal of the level comparator 31. This is supplied through terminal 4 to the counter 17 in the control signal generator 11 in the control unit 3.

The counter 17 counts pulses which form the clock signal 5c1 as shown in FIG. 4B which are supplied to a clock terminal CX during each counting period in which the comparison output signal Po has a high level and produces the count output Co which represents the counted result. In such a case, as shown in FIGS. 4A, 4B and 4C, the comparison output signal Po is formed into a signal Poh having a high level during a relatively short period of time when the external control signal Sc constitutes a signal Sch having a relatively high level in relation to the level of the integrated output signal Sw, and into a signal Pon having a high level during a medium period of time when the external control signal Sc constitutes a signal Sch which has a medium level in relation to the level of the integrated output signal Sw, and into a signal Pof having a high level during a relatively long period of time when the external control signal...
Sc constitutes a signal Sc of having a relatively low level in relation to the level of the integrated output signal Sw. When the comparison output signal Po is formed into the signal Poh, one pulse of the clock signal Pc1 is counted in the counter 17 and the count output Co representing "1" is obtained from the counter 17. When the comparison output signal Po is formed into the signal Poh, three pulses of the clock signal Pc1 are counted in the counter 17 and the count output Co representing "3" is obtained from the counter 17, and when the comparison output signal Po is formed into the signal Pof, five pulses of the clock signal Pc1 are counted in the counter 17 and the count output Co representing "5" is obtained from the counter 17. The count output Co is reset after each period of time Tw.

Further, when the external control signal Sc has its level higher than the level of the signal Sch and therefore the comparison output signal Po has a high level during a considerably short period of time compared with the signal Poh or does not have a high level, the count output Co representing "0" is obtained from the counter 17. On the other hand, when the external control signal Sc has its level lower than the level of the signal Sc of and therefore the comparison output signal po has a high level during a considerably long period of time compared with the signal Pof, the count output Co representing a number more than "6" is obtained from the counter 17.

Accordingly, the counter 17 is operative to produce the count output Co which represents the count result corresponding to each counting period in which the comparison output signal Po has a high level, so as to detect the length of the counting period.

The count output Co is supplied to the counted result detector 19 which detects the counted result represented by the count output Co. The counted result detector 19 produces the first control signal Pxx when the counted result detected by the counted result detector 19 is "1" or "0", that is, the counting period of time is shorter than a first predetermined reference period of time. The second control signal Pxx is produced when the counted result detected by the counted result detector 19 is equal to or more than "5", that is, the counting period of time is longer than a second predetermined reference period of time which is selected to be longer than the first predetermined reference period. Further, the counted result detector 19 does not produce any control signal when the counted result detected by the counted result detector 19 is "2", "3" or "4".

Consequently, the first control signal Pxx is obtained from the counted result detector 19 when the external control signal Sc has its level equal to or higher than the level of the signal Sch during each period of time Tw, and the second control signal Pxx is obtained from the counted result detector 19 when the external control signal Sc has its level equal to or lower than the level of the signal Sc during each period of time Tw. This means that the first control signal Pxx is obtained from the counted result detector 19 in response to an increase in the level of the external control signal Sc and the second control signal Pxx is obtained from the counted result detector 19 in response to a decrease in the level of the external control signal Sc, so both first and second control signals Pxx and Pxx act as the level detected output signal in respect of the external control signal Sc.

Each of the first and second control signals Pxx and Pxx is supplied to the pulse generator 13 and the pulse generator 13 is operative to increase the pulse duty factor of the pulse signal Pw in response to the first control signal Pxx and to decrease the pulse duty factor of the pulse signal Pw in response to the second control signal Pxx. Accordingly, the pulse duty factor of the pulse signal Pw is increased so that the integrated output signal sw obtained from the integrator is increased in level in a manner such as to change to a signal Sw shown in FIG. 5 from a signal Sw shown in FIG. 5 when the external control signal Sc has its level equal to or higher than the level of the signal Sch, and it is decreased so that the integrated output signal Sw obtained from the integrator 29 is decreased in level in such a manner as to change to a signal Sw shown in FIG. 5 from the signal Sw shown in FIG. 5, when the external control signal Sc has its level equal to or lower than the level of the signal Sc. As a result, a condition such that the level of the external control signal Sc which has a medium level in relation to the level of the integrated output signal Sw is compared with the level of the integrated output signal Sw in the level comparator 31 is obtained and thereafter the above described operation is repeatedly carried out.

Each of the first and second control signals Pxx and Pxx is also supplied to the driving signal generator 2 as the output signal from the control signal generator 11. The driving signals Sd supplied from the driving signal generator 2 to the fluorescent display tube 1 is composed of a group of pulse signal components which drive the fluorescent elements provided in the fluorescent display tube 1, respectively. The brightness of the display of the fluorescent elements in the fluorescent display tube 1 is changed in accordance with variations in the pulse duty factor of each of the pulse signal components which form the driving signal Sd.

The driving signal generator 2 is operative to increase the pulse duty factor of each of the pulse signal components which form the driving signal Sd in response to the first control signal Pxx which is supplied from the control signal generator 11 and to decrease the pulse duty factor of each of the pulse signal components which form the driving signal Sd in response to the second control signal Pxx which is supplied from the control signal generator 11. Accordingly, the pulse duty factor of each of the pulse signal components which form the driving signal Sd is increased so that the brightness of the display of the fluorescent elements in the fluorescent display tube 1 is increased when the external control sig-
nal Sc has its level equal to or higher than the level of the signal Sch, and is decreased so that the brightness of the display of the fluorescent elements in the fluorescent display tube 1 is decreased when the external control signal Sc has its level equal to or lower than the level of the signal Sc. As a result, the brightness of the display of the fluorescent display tube 1 is controlled in response to the level variations of the external control signal Sc.

Although, in the embodiment described above, the integrated output signal Sw supplied to the reference input terminal of the level comparator 31 is formed so as to have a level which increases exponentially during each period of time Tw and which decreases exponentially after each period of time Tw, it is possible for the integrated output signal Sw to have a level which decreases exponentially during each period of time Tw and which increases exponentially after each period of time Tw. In such a case, the comparison output signal po is formed so as to have a high level during a relatively long period of time when the external control signal Sc has a relatively high level in relation to the level of the integrated output signal Sw, and to have a high level during a medium period of time when the external control signal Sc has a medium level in relation to the level of the integrated output signal Sw, and to have the high level during a relatively short period of time when the external control signal Sc has a relatively low level in relation to the level of the integrated output signal Sw, and the counted result detector 19 produces the first control signal Pxu when the counting period of time during which the comparison output signal Po has the high level is longer than a third predetermined reference period of time and the second control signal Pxd when the counting period of time is shorter than a fourth predetermined reference period of time which is selected to be shorter than the third predetermined reference period.

Although the invention has been described with respect to preferred embodiments, it is not to be so limited as changes and modifications can be made which are within the full intended scope of the invention as defined by the appended claims.

Claims

1. A signal level detecting circuit comprising:

- an input terminal (33) to which an input signal (Sc) which has level variations is applied,
- a level comparing means (31) which has first and second input terminals supplied with the input signal (Sc) and a reference signal (Sw), respectively, and operative to produce a comparison output signal, said comparison output signal having a first level during first periods of time wherein the level of the input signal is not higher than the level of the reference signal and

a second level during periods of time other than said first periods of time, characterized by a control signal generating means (11) operative to detect said first periods of time and to produce a pair of first and second control signals, said first control signal (Pxu) being produced when the detected first period of time is shorter than a first reference time, said second control signal (Pxd) being produced when the detected first period of time is longer than a second reference time which is selected to be longer than said first reference time,

a pulse generating means (13) operative to produce a pulse signal (Pw), which has a period which is based on a predetermined clock signal (Pc2) and a pulse duty factor which is variable during a given time, at regular intermittent intervals, so as to vary the pulse duty factor of the pulse signal in a first manner whenever said first control signal is obtained from said control signal generating means (11), and to vary the pulse duty factor of the pulse signal in a second manner which is different from said first manner whenever said second control signals is obtained from said control signal generating means (11), and

an integrating means (29) operative to produce an integrated output signal based on the pulse signal obtained from said pulse generating means (13) during said given time and to supply the second input terminal of said level comparing means (31) with the integrated output signal as said reference signal.

2. A signal level detecting circuit comprising:

- an input terminal (33) to which an input signal (Sc) which has level variations is applied,
- a level comparing means (31) which has first and second input terminals supplied with the input signal (Sc) and a reference signal (Sw), respectively, and operative to produce a comparison output signal, said comparison output signal having a first level during first periods of time when the level of the input signal is not lower than the level of the reference signal and a second level during periods of time other than said first periods of time, characterized by a control signal generating means (11) operative to detect said first periods of time and to produce a pair of first and second control signals, said first control signal (Pxu) being produced when the detected first period of time is longer than a first reference time, said second control signal (Pxd) being produced when the detected first period of time is shorter than a second reference time which is selected to be shorter than said first reference time,
a pulse generating means (13) operative to produce a pulse signal (Pw), which has a period which is based on a predetermined clock signal (Pc2) and a pulse duty factor which is variable during a given time, at regular intermittent intervals, so as to vary the pulse duty factor of the pulse signal in a first manner whenever said first control signal is obtained from said control signal generating means (11), and to vary the pulse duty factor of the pulse signal in a second manner which is different from said first manner whenever said second signal is obtained from said control signal generating means (11), and an integrating means (29) operative to produce an integrated output signal based on the pulse signal obtained from said pulse generating means (13) during said given time and to supply the second input terminal of said level comparing means (31) with the integrated output signal as said reference signal.

3. A signal level detecting circuit according to claim 1, wherein said control signal generating means (11) comprises a counter (17) which is supplied with said comparison output signal from said level comparing means (31) and which is operative to count the pulses forming another clock signal (Pc1) during each time during which said comparison output signal has the first level and to produce a count output (Co) representing a counted result, and a counted result detector (19) supplied with the count output (Co) from said counter (17) and operative to detect the counted result represented by the count output (Co) and to produce said pair of first (Pxx) and second (Pxd) control signals based on the counted result detected.

4. A signal level detecting circuit according to any one of the preceding claims, wherein said integrating means (29) comprises a capacitor (27) connected between the reference input terminal of said level comparing means (31) and a reference potential terminal, and a resistor (25) with one end to which said pulse signal is supplied and the other end connected to the reference input terminal of said level comparing means (31).

5. A signal level detecting circuit according to anyone of claims 1 to 4, further comprising a buffer amplifier means (23) which is connected between said pulse generating means (13) and said integrating means (29).

6. A signal level detecting circuit according to anyone of claims 3 to 5, further comprising a clock generating means (15) for supplying said pulse generating means (13) and said counter (17) with said predetermined clock signal (Pc2) and said another clock signal (Pc1), respectively.

**Patentansprüche**

1. Signalpegel-Erfassungsschaltung mit einem Eingang (33), zu dem ein Eingangssignal (Sc) mit Pegelanänderungen gegeben wird; einer Pegel-Vergleichseinrichtung (31), die einen ersten und einen zweiten Eingang aufweist, zu dem das Eingangssignal (Sc) bzw. ein Referenzsignal (Sw) gegeben werden, und die ein Vergleichs-Ausgangssignal erzeugt, wobei das Vergleichs-Ausgangssignal einen ersten Pegel während erster Zeitdauern, während der der Pegel des Eingangssignales nicht größer als der Pegel des Referenzsignales ist, und einen zweiten Pegel während anderer als der ersten Zeitdauern aufweist, gekennzeichnet durch

eine Steuersignal-Erzeugungseinrichtung (11) zur Erfassung der ersten Zeitdauer und zur Erzeugung eines Paares eines ersten und eines zweiten Steuersignales, wobei das erste Steuersignal (Pxx) erzeugt wird, wenn die erfasste erste Zeitdauer kürzer als eine erste Referenzzeitdauer ist, und wobei das zweite Steuersignal (Pxd) erzeugt wird, wenn die erfasste erste Zeitdauer länger als eine zweite Referenzzeitdauer ist, die länger als die erste Referenzzeitdauer gewählt ist;
eine Impuls-Erzeugungseinrichtung (13) zur Erzeugung eines Impulsseignales (Pw) aufweist, das eine Periode, die auf einem vorbestimmten Taktsignal (Pc2) beruht, und ein Impuls-Tastverhältnis in regelmäßig bestandenen Intervallen, das während einer gegebenen Zeit variabel ist, um das Impuls-Tastverhältnis des Impulsseignales in einer ersten Weise zu ändern, wenn das erste Steuersignal von der Steuersignal-Erzeugungseinrichtung (11) erhalten wird, und das Impuls-Tastverhältnis des Impulsseignales in einer zweiten Weise unterschiedlich von der ersten Weise zu verändern, wenn das zweite Steuersignal von der Steuersignal-Erzeugungseinrichtung (11) erhalten wird, und

2. Signalpegel-Erfassungsschaltung mit einem Eingang (33), zu dem ein Eingangssignal (Sc) mit Pegelvariationen gegeben wird;
einer Pegel-Vergleichseinrichtung (31), die einen ersten und einen zweiten Eingang aufweist, zu denen das Eingangssignal (Sc) bzw. ein Referenzsignal (Sw) gegeben wird, und die ein Vergleichs-Ausgangssignal erzeugt, wobei das Vergleichs-Ausgangssignal einen ersten Pegel während erster Zeitdauer aufweist, wenn der Pegel des Eingangssignales niedriger als der Pegel des Referenzsignals ist, und einen zweiten Pegel während anderer als der ersten Zeitdauer, gekennzeichnet durch

- eine Steuersignal-Erzeugungseinrichtung (11) zur Erfassung der ersten Zeitdauer und zur Erzeugung eines Paares eines ersten und eines zweiten Steuersignales, wobei das erste Steuersignal (Pxx) erzeugt wird, wenn die erfaßte erste Zeitdauer länger als eine erste Referenzzeit ist, und das zweite Steuersignal (Pxd) erzeugt wird, wenn die erfaßte erste Zeitdauer kürzer als eine zweite Referenzzeit ist, die kürzer als die erste Referenzzeit gewählt ist;
- eine Impuls-Erzeugungseinrichtung (13) zur Erzeugung eines ImpulsSignals (Pw) in regelmäßig beobachteten Intervallen, das eine Zeitdauer aufweist, die auf einem vorbestimmten Taktsignal (Pc2) beruht, und ein Impuls-Tastverhältnis, das während einer gegebenen Zeit variabel ist, um das Impuls-Tastverhältnis des ImpulsSignals in einer ersten Weise zu verändern, wenn das erste Steuersignal von der Steuersignal-Erzeugungseinrichtung (11) erhalten wird, und das Impuls-Tastverhältnis des ImpulsSignals in einer zweiten Weise zu verändern, die unterschiedlich von der ersten Weise ist, wenn das zweite Steuersignal von der Steuersignal-Erzeugungseinrichtung (11) erhalten wird, und
- eine Integrations-Einrichtung (29) zur Erzeugung eines integrierten Ausgangssignales auf Grundlage des ImpulsSignals, das von der Impuls-Erzeugungseinrichtung (13) während der gegebenen Zeit erhalten wird, und um das integrierte Ausgangssignal als das Referenzsignal zu dem zweiten Eingang der Pegel-Vergleichsschaltung (31) zu geben.

3. Signalpegel-Erfassungsschaltung nach Anspruch 1,

bei der die Steuersignal-Erzeugungseinrichtung (11) einen Zähler (17), zu dem das Vergleichs-Ausgangssignal von der Pegel-Vergleichseinrichtung (31) gegeben wird, und der die Impulse zählt, die ein weiteres Taktsignal (Pc1) während jeder Zeitdauer bilden, während der das Vergleichs-Ausgangssignal den ersten Pegel einnimmt, und der ein Zähl-Ausgangssignal (Co) erzeugt, das das Erfassungsergebnis wiedergibt, und einen Zählergegen-De君ktor (19) aufweist, zu dem das Zähler-Ausgangssignal (Cc) von dem Zähler (17) gegeben wird, und der das Erfassungsergebnis, das durch das Zähler-Ausgangssignal (Cc) wiedergegeben wird, erfaßt und das Paar des ersten (Pxx) und zweiten (Pxd) Steuersignales auf Grundlage des erfaßten Zählergebnisses erzeugt.


5. Signalpegel-Erfassungsschaltung nach einem der Ansprüche 1 bis 4, weiterhin aufweisend eine Puffer-Verstärkereinrichtung (23), die zwischen der Impuls-Erzeugungseinrichtung (13) und der Integrations-Einrichtung (29) geschaltet ist.

6. Signalpegel-Erfassungsschaltung nach einem der Ansprüche 3 bis 5, weiterhin aufweisend eine Takt-Erzeugungseinrichtung (15) zur Versorgung der Impuls-Erzeugungseinrichtung (13) und des Zählers (17) mit dem vorbestimmten Taktsignal (Pc2) bzw. mit einem weiteren Taktsignal (Pc1).

Revisions

1. Circuit de détection de niveau de signal comprenant :

- une borne d'entrée (33) à laquelle un signal d'entrée (Sc) qui a des variations de niveau est appliqué,
- un moyen de comparaison de niveau (31) qui a des premières et secondes bornes d'entrée reconnu respectivement, un signal d'entrée (Sc) et un signal de référence (Sw), et opérant pour produire un signal de sortie de comparaison, le dit signal de sortie de comparaison ayant un premier niveau pendant des premières périodes de temps où le niveau du signal d'entrée n'est pas plus élevé que le niveau du signal de référence et un second niveau pendant des périodes de temps autres que lesdites premières périodes de temps.

- caractérisé par
un moyen de génération de signal de commande (11) opérant pour détecter lesdites premières périodes de temps et pour produire une paire de premier et second signaux de commande, ledit premier signal de commande (Pxu) étant produit lorsque la première période de temps détectée est plus courte qu'un premier temps de référence, ledit second signal de commande (Pxdl) étant produit lorsque la première période de temps détectée est plus longue qu'un second temps de référence qui est sélectionné pour être plus long que ledit premier temps de référence.

un moyen de génération d'impulsions (13) opérant pour produire un signal d'impulsions (Pw), qui a une période qui est basée sur un signal d'horloge prédéterminé (Pc2) et un rapport cyclique d'impulsions qui est variable pendant un temps donné, à des intervalles intermittents réguliers, afin de faire varier le rapport cyclique d'impulsions du signal d'impulsions d'une première manière chaque fois que ledit premier signal de commande est obtenu dudit moyen de génération de signal de commande (11), et pour faire varier le rapport cyclique d'impulsions du signal d'impulsions d'une seconde manière qui est différente de ladite première manière chaque fois que ledit second signal de commande est obtenu dudit moyen de génération de signal de commande (11), et un moyen d'intégration (29) opérant pour produire un signal de sortie intégré basé sur le signal d'impulsions obtenu dudit moyen de génération d'impulsions (13) pendant ledit temps donné et pour fournir à la seconde borne d'entrée dudit moyen de comparaison de niveau (31) le signal de sortie intégré comme ledit signal de référence.

2. Circuit de détection de niveau de signal comprenant :

une borne d'entrée (33) à laquelle un signal d'entrée (Sc) qui a des variations de niveau est appliqué,
un moyen de comparaison de niveau (31) qui a des première et seconde bornes d'entrée recevant, respectivement, un signal d'entrée (Sc) et un signal de référence (Sw), et opérant pour produire un signal de sortie de comparaison, ledit signal de sortie de comparaison ayant un premier niveau pendant des premières périodes de temps lorsque le niveau du signal d'entrée n'est pas plus bas que le niveau du signal de référence et un second niveau pendant des périodes de temps autres que lesdites premières périodes de temps,

caractérisé par

un moyen de génération de signal de commande (11) opérant pour détecter lesdites premières périodes de temps et pour produire une paire de premier et second signaux de commande, ledit premier signal de commande (Pxu) étant produit lorsque la première période de temps détectée est plus longue qu'un premier temps de référence, ledit second signal de commande (Pxdl) étant produit lorsque la première période de temps détectée est plus courte qu'un second temps de référence qui est sélectionné pour être plus court que ledit premier temps de référence,

un moyen de génération d'impulsions (13) opérant pour produire un signal d'impulsions (Pw), qui a une période qui est basée sur un signal d'horloge prédéterminé (Pc2) et un rapport cyclique d'impulsions qui est variable pendant un temps donné, à des intervalles intermittents réguliers, afin de faire varier le rapport cyclique d'impulsions du signal d'impulsions d'une première manière chaque fois que ledit premier signal de commande est obtenu dudit moyen de génération de signal de commande (11), et pour faire varier le rapport cyclique d'impulsions du signal d'impulsions d'une seconde manière qui est différente de ladite première manière chaque fois que ledit second signal de commande est obtenu dudit moyen de génération de signal de commande (11), et un moyen d'intégration (29) opérant pour produire un signal de sortie intégré basé sur le signal d'impulsions obtenu dudit moyen de génération d'impulsions (13) pendant ledit temps donné et pour fournir à la seconde borne d'entrée dudit moyen de comparaison de niveau (31) le signal de sortie intégré comme ledit signal de référence.

3. Circuit de détection de niveau de signal selon la révendication 1, dans lequel ledit moyen de génération de signal de commande (11) comprend un compteur (17) qui reçoit ledit signal de sortie de comparaison dudit moyen de comparaison de niveau (31) et qui est opérant pour compter les impulsions formant un autre signal d'horloge (Pc1) pendant chaque période pendant laquelle ledit signal de sortie de comparaison a le premier niveau et pour produire une sortie de comptage (Co) représentant un résultat compté, et un détecteur de résultat compté (19) recevant la sortie de comptage (Co) dudit compteur (17) et opérant pour détecter le résultat compté représenté par la sortie de comptage (Co) et pour produire ladite paire de premier (Pxu) et second (Pxdl) signaux de commande sur la base du résultat compté détecté.
4. Circuit de détection de niveau de signal selon l'une quelconque des revendications précédentes, dans lequel ledit moyen d'intégration (29) comprend un condensateur (27) raccordé entre la borne d'entrée de référence dudit moyen de comparaison de niveau (31) et une borne de potentiel de référence, et une résistance (25) avec une extrémité à laquelle ledit signal d'impulsions est appliqué et l'autre extrémité raccordée à la borne d'entrée de référence dudit moyen de comparaison de niveau (31).

5. Circuit de détection de niveau de signal selon l'une quelconque des revendications 1 à 4, comprenant en outre un moyen amplificateur tampon (23) qui est raccordé entre ledit moyen de génération d'impulsions (13) et ledit moyen d'intégration (29).

6. Circuit de détection de niveau de signal selon l'une quelconque des revendications 3 à 5, comprenant en outre un moyen de génération d'horloge (15) pour fournir audit moyen de génération d'impulsions (13) et audit compteur (17) respectivement ledit signal d'horloge prédéterminé (Pc2) et ledit autre signal d'horloge (Pc1).
FIG. 2

FIG. 3