EUROPEAN PATENT SPECIFICATION

Method of producing a semiconductor device having thin film resistor

Verfahren zur Herstellung einer Halbleiteranordnung mit Dünnfilm-Widerstand

Méthode de fabrication d'un dispositif semi-conducteur ayant une résistance en couche mince

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References cited:
EP-A- 0 101 632
WO-A-83/00256
JP-B- 50 038 200
US-A- 4 569 742

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[0001] This invention relates to a semiconductor device having a thin film resistor integrated therein and a method of producing the same as a molded resin package.

[0002] Conventionally, a thin film resistor is formed and integrated with an insulating component of an IC, LSI or the like, to be used as a resistor.

[0003] This thin film resistor is usually composed of chromium (Cr) and silicon (Si) because the temperature coefficient of the resistance (TCR) thereof is low, and therefore any variations of the resistance due to changes in the temperature thereof are small.

[0004] Also, the TCR of this kind of thin film resistor composed of Cr and Si can be further lowered by varying the ratio of the content of Cr and Si.

[0005] Nevertheless, this kind of thin film resistor has a disadvantage in that it is difficult to make the TCR zero, and in general, preferably the value of $\Delta R/R_{25}$, as shown in Figure 7, is always zero even when the temperature is varied.

[0006] Figure 7 shows the temperature dependency of the resistor value, and for the above purpose, a condition of $\alpha = 0$ and $\beta = 0$ is required in the following equation obtained by the method of least squares.

$$\Delta R/R_{25} = \alpha(T - 25) + \beta(T - 25)^2$$

[0007] Wherein $R_{25}$ represents a resistance value at a temperature of 25°C, $\Delta R$ represents a variation of the value ($R_1 - R_{25}$) of the resistance measured at the temperature $T$ and $R_{25}$, $\alpha$ represents a primary coefficient, and $\beta$ represents a secondary coefficient.

[0008] As shown in Figure 8, a problem arises in that the condition of $\alpha = 0$ can be realized but another condition, i.e., $\beta = 0$ cannot be simultaneously realized.

[0009] It is considered that the reason for the non-linearity of the graph shown in Figure 7 is that, when the mobility $\mu$ becomes greater due to the existence of the microcrystal of the CrSi$_2$ in the thin film resistor composed of a Cr-Si compound, the effect of the lattice vibration caused by the change in temperature becomes remarkable, and thus the resistance represented by the following equation will be varied because variation of the $\mu$ becomes large as the temperature is raised.

$$\text{Resistance} = \frac{1}{q \times \mu \times n}$$

[0010] The present invention is intended to overcome the above problems and the object of this invention is to provide a method of producing a semiconductor device having a thin film resistor, wherein little change of the value of the resistance occurs despite variations of the temperature thereof.

[0011] Therefore, according to the present invention there is provided a method according to claim 1. The produced device is characterized in that the thin film resistor is amorphous and has the same energy band structure as that of metal.

Figure 1, and Figures 3 to 6 are cross sectional views illustrating a process of manufacturing one embodiment of the present invention;

Figure 2 is a schematic view of a sputtering device used for the embodiment shown in Figure 1, and Figures 3 to 6;

Figure 7 is a graph of a temperature dependency of a variation of the resistor value when using a conventional thin film resistor composed of chromium (Cr) and silicon (Si);

Figure 8 is a graph of a relationship between the primary coefficient $\alpha$ and the secondary coefficient $\beta$ when the ratio of Cr and Si is varied when using a conventional thin film resistor composed of Cr and Si;

Figure 9 is a graph of a temperature dependence characteristic of a variation of the resistor value where a value of the nitrogen $N_2$ is varied while the sputtering operation is carried out when using a thin film resistor composed of Cr, Si and N at a ratio of Si/(Si + Cr) of 47.5 wt%;

Figure 10(a) is a graph of a relationship between a value of the $N_2$ where the sputtering operation is carried out and a primary coefficient $\alpha$ when using a Cr-Si-N thin film resistor utilizing a CrSi target having a composition ratio of Si/(Si + Cr) of 47.5 wt%;

Figure 10(b) is a graph of a relationship between a volume of the $N_2$ where the sputtering operation is carried out and a secondary coefficient $\beta$ when using a Cr-Si-N thin film resistor formed from the CrSi target, the weight percentage of Si/(Si + Cr) being 47.5 wt%;

Figure 11 is a graph of a degree of crystallization and a generation of an optical band gap where a volume of the nitrogen $N_2$ is varied when the sputtering operation is carried out when using a Cr-Si-N thin film resistor utilizing the CrSi target, the weight percentage of Si/(Si + Cr) being 47.5 wt%;

Figure 12 shows a resistance-temperature characteristic when the composition of the target and the added volume of $N_2$ are varied;

Figure 13 shows a resistance-temperature characteristic when the annealing temperature is varied;

Figures 14(a) and 14(b) show a relationship between the film thickness of the Cr-Si-N thin film resistor 80 and the value of the primary coefficient $\alpha$ or the secondary coefficient $\beta$, respectively;

Figures 15(a), 15(b) and 15(c) show a graph obtained by plotting the results of X-ray diffraction;

Figure 16 shows an energy band gap of the Cr-Si-N thin film resistor;
Figure 17 shows a relationship between the composition ratio and the volume of N₂;
Figure 18 shows a practical cross sectional view of the resin molded IC package of one embodiment of this invention;
Figure 19 shows an electrical circuit used in the resin molded IC package of one embodiment of this invention;
Figure 20 shows a graph indicating a relationship between a strain and a variation of the resistance value;
Figure 21 shows a layout of a thin film resistor arranged on a chip for a stress test;
Figure 22 shows a graph of a distribution of a shearing force; and
Figure 23 shows a graph of a distribution of a compressive stress.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] The preferred embodiments of this invention will be explained with reference to the accompanying drawings.

[0013] Figures 1 to 6 illustrate the first embodiment of this invention.

[0014] As shown in Figure 1, a P-type channel stopper 20, a LOCOS oxide layer 30, a gate oxide layer 40, a polycrystalline silicon gate layer 50, an N-type diffusion source layer 60, an N type diffusion drain layer 65, and a BPSG layer 70 are formed, in this order, on a P-type silicon semiconductor substrate 10 by a usual MOS process, and then the thus fabricated material is fixed to an electrode 3 of a substrate of the N₂ reactive sputtering device, as shown in Figure 2.

[0015] Subsequently, a target 5 composed of Cr and Si, in which the weight percentage % of silicon to the total weight of chromium and silicon (Si/Si + Cr) is 49 wt%, is fixed to a target electrode 6 and they are both arranged in a sputtering device 7 and a reactive sputtering operation is carried out under the conditions of a reactive sputtering, forming a predetermined pattern by photo-etching the plasma nitride film. As shown in Figure 3, when the additional volume of N₂ during the sputtering operation is from 1 - 2 %, the variation of the value of the resistor is small despite variations of the temperature, and when Cr-Si-N thin film resistor (the N₂ value during the sputtering is (N₂/Ar) = 1.5%) is used, the variation of the resistor value due to temperature variations is substantially

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As shown in Figure 9, the variation of the value of the resistor due to temperature variations during the sputtering when the N₂ volume is 3% is larger than when the N₂ volume during the sputtering operation is from 1 - 2%.

This is because a higher volume of N₂ caused the generation of an as shown in Figure 11, which gives the resistor the same characteristics as a semiconductor, thereby a variation of carrier density n due to a temperature variation will be generated and therefore, when the value n in the above equation;

\[
\text{Resistance} = \frac{1}{q \times \mu \times n}
\]

is varied due to variations of the temperature, the value of the resistance is also varied.

Therefore, the upper limit to the amount of additional N₂ is a value such that the optical band gap is not generated in the thin film resistor i.e., a value at which the thin film resistor has the same characteristics as a metal.

As shown in Figure 11, when the N₂ volume is varied from 0 to 1%, the intensity of X ray diffraction of the microcrystal of CrSi₂ in the Cr-Si-N thin film resistor, is reduced as the N₂ volume is increased.

Further, when the value of N₂ is 1 - 2%, the diffraction peak measured by X ray diffraction is not generated.

Figure 15 shows the results of the X ray diffraction, wherein Figure 15(a) shows the case in which N₂ is not added, Figure 15(b) show the case in which 1% of N₂ is added, and Figure 15(c) shows the case in which 2% of N₂ is added.

As shown in these Figures, when N₂ is not added the peaks indicating the existence of the microcrystal of CrSi₂ therein, appear at the three respective points A, B and C, but when N₂ is added, no peak appears.

This means that, when the N₂ volume is increased, the degree of microcristallization of CrSi₂ in the Cr-Si-N thin film resistor is reduced, and thus the Cr-Si-N thin film resistor becomes amorphous.

But, when the N₂ volume is excessive, an undesirable optical band gap is generated as explained above.

Figure 16 shows the results obtained when the energy band construction of the Cr-Si-N thin film resistor was analysed by a tunnel spectroscopy utilizing a tunnel current measurement method.

As shown in Figure 16, when the N₂ volume is 0%, a densities of states N(E) is not reduced at an energy E = 0 eV and when the N₂ volume is 3%, a densities of states N(E) is reduced and indicates that an energy band gap has been formed.

These results are the same as the results obtained by the optical band gap measuring method.

It is considered that characteristics of the energy band of the Cr-Si-N thin film resistor will change from those of a metal to those of a semiconductor as the N₂ volume is increased.

Namely, as understood from the results obtained by the optical band gap measuring method and the densities of states N(E) measuring method, the N₂ volume should be such that an energy band gap of the Cr-Si-N thin film resistor is not generated.

When the N₂ volume is within the above range, the Cr-Si-N thin film resistor has the characteristics of a semiconductor in which the carrier density thereof is not change by variations of the temperature.

As apparent from Figures 10(a) and 10(b), when the N₂ volume during the sputtering is varied, the primary coefficient α and a secondary coefficient β can be made zero, and in this embodiment, when the N₂ volume is 1.5%, the coefficients α and β can be made approximately zero, and therefore, the resistance value of the Cr-Si-N thin film resistor undergoes little change even when the temperature is varied as shown in Figure 9.

Figure 12 shows a resistance-temperature characteristic when the composition of the target and the additional N₂ volume are varied.

As shown in Figure 12, the values of the primary coefficient α and the secondary coefficient β are close to zero when the silicon weight percentage is 41 - 57 wt% and the additional N₂ volume is 1 - 2%, and thus the temperature coefficient of the resistance (TCR) is close the zero.

Figure 13 shows a resistance-temperature characteristic depending upon variations of the annealing temperature applied to the thin film resistor after the forming, thereof.

As shown in Fig. 13, the values of the primary coefficient α and the secondary coefficient β are close to zero when the annealing temperature is lower than 500°C, and when the annealing temperature is higher than 500°C, the value of the primary coefficient α is gradually raised and the value of the secondary coefficient β is gradually lowered.

The reason why the values of the primary coefficient α and secondary coefficient β are changed is considered to be that, when the annealing temperature is higher than 500°C, crystallization of the CrSi₂ in the thin film resistor occurs and thus the thin film resistor is no longer amorphous.

According to this embodiment, as explained above, since the thermal history applied to the thin film resistor from when the thin film resistor is formed to when the final process is carried out is lower than 500°C, the values of the primary coefficient α and the secondary coefficient β are not changed.

Figures 14(a) shows relationship between the film thickness of the Cr-Si-N thin film resistor 80 and the value of the primary coefficient α with respect to the
N₂ value as a parameter, and Figure 14(b) shows a relationship between the film thickness of the Cr-Si-N thin film resistor 80 and the secondary coefficient β when the N₂ value is constant.

[0052] In these Figures, the curve having a circle symbol shows the characteristic when 1.5% of N₂ is added and the curve having a triangle shows the characteristic when N₂ is not added.

[0053] As shown in these Figures, when N₂ is added according to the present invention, the TCR does not depend upon the thickness of the film, and thus a desired resistance value can be easily obtained by adjusting the thickness of the film.

[0054] Further, since the TCR does not change even when variations of the thickness of the film occur during the manufacturing process, the thin film resistor of the present invention is easily produced.

[0055] Figure 17 shows the results of a component analysis of the Cr-Si-N thin film resistor of this embodiment, utilizing an XPS analyzer, wherein the component ratio is indicated as the ratio of the atomic number when the atomic number of Cr is assumed to be 1. In Figure 17, the thin film to be analyzed was produced in such a way that Cr-Si-N film having a thickness of 1000 Å is formed on a substrate and then it was heat treated in a gas stream of H₂/N₂ at a temperature of 450°C for 30 minutes. Thereafter the thickness of the film was reduced to 200 Å by etching operation with a sputtering method utilizing a device such as ESCALAB-5 produced by VG Co.. Then the surface of it is provided to the analysis.

[0056] As shown in Figure 17, when the N₂ volume is increased during the N₂ reactive sputtering, the composition ratio of nitrogen N in the thin film is also increased, and further, as the volume of nitrogen is increased, the volumes of oxygen and carbon are also increased.

[0057] Oxygen is naturally taken into the film during the sputtering to form a network of Si-N-O, and therefore, the volume of oxygen will be increased as the volume of nitrogen is increased.

[0058] Accordingly, as a component of the Cr-Si-N thin film resistor, the volume of chromium, silicon, nitrogen, and oxygen must be controlled.

[0059] When the atomic number of Cr is represented as 1 and the composition ratio of Cr, Si, N and O are controlled, for example, Cr = 1, Si = 2 - 2.5, N = 0.3 - 1.5 and O = 0.5 - 1.5, a thin film resistor in which the resistance characteristic has a low temperature dependency is obtained.

[0060] Note, when the atomic number of Cr is represented as 1, carbon may be included therein at a composition ratio of C = 0 - 1.

[0061] Also, in this embodiment, an N₂ reactive sputtering method is used for producing the Cr-Si-N thin film resistor, but other methods may be used as long as they are within the scope of the claims.

[0062] Further, when the atomic number of Cr is represented as 1, the composition ratio of the thus-formed thin film resistor may be, for example, Cr = 1, Si = 2 - 2.5, N = 0.3 - 1.5 and O = 0.5 - 1.5.

[0063] In this embodiment, the film thickness of the Cr-Si-N thin film resistor is set at 160 Å but this thickness is not restricted and may be 30 - 1000 Å as mentioned above, and further although the weight percentage of Si in the CrSi target is set at 47.5 wt%, it may be set at 41 - 57 wt% as shown in Figure 2.

[0064] This embodiment of the present invention is applied to an NMOS process, but can be applied to any other process as long as Cr-Si-N thin film resistor can be used and it can be applied to a CMOS process, bi-MOS process, bi-polar IC process or the like.

[0065] Further, in this embodiment the Cr-Si-N thin film resistor is formed on the surface of a BPSG film, but this resistor may be formed on a surface of an insulating portion such as an SiO₂ film, PSG film, Si₃N₄ film or the like. Also, the thin film resistor of the present invention can be used alone as a resistor device chip for a resistor array.

[0066] A semiconductor device in which a linear integrated circuit includes resistors on a chip is known, and a method in which a linear IC chip is packaged by a resin molding process is now in use.

[0067] In this type of device, however, a problem has been arisen in that the resistance is easily changed by a variation of a stress occurring during the resin molding operation, and thus it is considered difficult to obtain a high accuracy of an analog characteristic thereof in one chip.

[0068] Namely, when packaging process is carried out, a resistance value of a polycrystalline silicon or diffusion resistance (P⁺) is varied due to the effect of the stress of the resin molding, and at the same time, is varied by variations of the stress applied to the IC chip due to a variation of a temperature caused by variations of an atmospheric temperature thereof or a heat generation thereof.

[0069] Therefore, when a linear IC, which requires a high accuracy since it is used as a 5 V power source IC in automobiles without adjustment, is produced, the resistors are usually mounted thereon by arranging them outside the package, whereby the number of terminals of the IC, the electric devices mounted externally of the package, the steps for assembling those devices on the package, and the area of the substrate occupied by those devices are increased, which greatly increases production costs.

[0070] Therefore, there is a need for a method of providing a semiconductor in which a variation of the resistance caused by a variation of a stress applied to the IC chip due to a variation of the temperature, can be effectively suppressed.

[0071] An embodiment of a semiconductor device which is used as a 5 V power source IC in an automobile, without adjustment, will be explained with reference to the drawings.
In this IC, an output voltage is adjusted by a thin film trimmed on a chip, i.e., a thin film resistor as mentioned above.

As shown in Fig. 19, a battery voltage $V_{\text{BATT}}$ is applied to an emitter terminal of a PNP transistor $T_{r1}$, and a constant output voltage is output from a collector terminal of the PNP transistor $T_{r1}$.

An output of a differential amplifier 100 is connected to a base terminal of the PNP transistor $T_{r1}$, and the non-inverting input terminal thereof is connected to a terminal $102a$ of a band gap reference voltage generating portion 102.

A terminal $102b$ of the band gap reference voltage generating portion 102 is connected to the earth, and another terminal $102c$ is also connected to the earth through a thin film resistor 103, for example, a Cr-Si thin film resistor, to change the value thereof, the band gap reference voltage $V_{\text{ref}}$ output from the terminal $102a$ of the band gap reference voltage generating portion 102 can be adjusted.

The collector terminal of the PNP transistor $T_{r1}$ is connected to the earth through resistors $R4$ and $R5$ connected in series, and a node portion formed between the resistors $R4$ and $R5$ is connected to an inverting input terminal of the differential amplifier 100.

These resistors $R4$ and $R5$ are used for amplifying the band gap reference voltage generating $V_{\text{ref}}$.

The constant output voltage $V_{\text{out}}$ is represented by the following equation:

$$V_{\text{out}} = (V_{\text{ref}} + V_{\text{IO}}) \times \frac{r1 + r2}{r1}$$

Wherein $V_{\text{ref}}$ denotes a band gap reference voltage, $V_{\text{IO}}$ denotes an offset voltage of the differential amplifier 100, $r1$ denotes a value of the resistor 105, and $r2$ denotes a value of the resistor 104.

Accordingly, when a constant output voltage $V_{\text{out}} = 5$ V is required, the following conditions, for example, $V_{\text{ref}} + V_{\text{IO}} = 1.25$ V and $(r1 + r2)/r1 = 4$, should be satisfied.

Before the molded resin packaging process, the band gap reference voltage $V_{\text{ref}}$ is adjusted by trimming the thin film resistor 103 (trim resistor) by a laser trimming method, to provide an output voltage $V_{\text{out}}$ of 5 V.

Namely, in this embodiment, even when the initial values of $V_{\text{ref}}, V_{\text{IO}}, r1$, and $r2$ are varied respectively, the output voltage $V_{\text{out}}$ can be set precisely at 5 V.

In this embodiment, a Cr-Si-N thin film resistor or a Cr-Si-N-O thin film resistor, as explained above, is used for the resistors 104 and 105.

Figure 18 shows an arrangement of the resistor 104 and 105 in an IC chip, wherein an insulation film (SiO$_2$) 107 is deposited on a surface of a silicon substrate 106 and Cr-Si thin film resistors or Cr-Si-N thin film resistors 108 and 109 are provided on the surface of the insulation film 107 by a sputtering method.

The thin film resistors 108 and 109 are electrically connected to an aluminum wiring 110.

Further, there is provided a surface protection film 111 covering the surface of the thin film resistors 108 and 109 and the aluminum wiring 110 and the surface of the protection film 111 is covered with a molding resin, and after the resistor (trim resistor) is trimmed, a packaging process for packaging the IC chip with a molding resin is carried out.

More precisely, after the IC chip is adhered to a chip mounting portion of a lead frame with a suitable adhesive (die bonding), a bonding pad provided on the chip is connected to the lead frame and then the packaging process is carried out.

In the packaging process utilizing a resin molding method, when a polysiloxane or a diffusion resistor is used in accordance with a conventional method, the value of the resistance of the IC package after the packaging operation is completed is remarkably different from the initial value thereof before the packaging process is carried out, due to the influence of the stress generated by an adhesive, fixing the lead frame and the IC chip, curing, or the stress generated by the molding resin. Therefore, the output voltage $V_{\text{out}}$ is entirely different.

When the output voltage $V_{\text{out}}$ is measured in such a way that a diffusion resistor (P$^+$) is used as the resistors 104 and 105 and the output voltage of the IC is adjusted to $5 \pm 0.001$ V, then the IC chip is packaged by a resin molding method, and thereafter, the molded chip is measured the output voltage thereof remarkably varied in the range of $5 \pm 0.035$ V (0.7%).

In comparison, in the present invention, when Cr-Si-N thin film resistors 108 and 109 are used as the resistors 104 and 105, a film thickness of 30 - 1000 Å can be obtained, and the output voltage after the molded resin packaging is completed can be set to $5 \pm 0.0075$ V (0.15%).

Figure 20 shows a variation of the resistance value $(\Delta R/R)$ of the resistors 104 and 105 with respect to the strain of a chip after the packaging is completed, wherein the characteristic curves L1 and L2 represent the cases in which the Cr-Si thin film resistors 108 and 109 are used as the resistors 104 and 105, respectively, and the characteristic curves L3 and L4 represent the...
cases in which polycrystalline silicon is used as the resistors 104 and 105, respectively.

[0093] As shown in Fig. 20, the two pairs of different characteristic curves (L1 and L2, L3 and L4) represent the results of measurements in which the resistors L and T are respectively mounted on a chip 113 fixed on a supporting vase 112 in such a way that one thereof is arranged so that the longitudinal axis thereof is parallel to the X axis and the other is arranged with the longitudinal axis thereof parallel to the Y axis, and then the resistance is measured by applying a strain to the chip with an external force indicated by an arrow in Figure 21. Further, the stress of the molding resin varies with the temperature, the lower the temperature, the larger the stress.)

[0094] It was confirmed that the variations of the resistance ΔR/R of the polycrystalline silicon resistor and the P’ diffusion resistor with respect to the strain are substantially the same.

[0095] When the value of the resistors 104 and 105, after the packaging operation was completed, is assumed to be Δr1 + Δr1, r2 + Δr2, respectively, (wherein Δr1 and Δr2 denote the variation of the value of the resistance after the molded packaging operation is completed), the output voltage Vout is represented by the following equation:

\[
V_{out} = (V_{ref} + V_{IO}) \times \frac{r1 + r2 + \Delta r1 + \Delta r2}{r1 + \Delta r1}
\]

[0096] Since the respective pattern arrangements of the resistors 104 and 105 on the chip are not located at exactly the same place on the chip, they must be separate from each other, and therefore the extent of the effect of the stress thereon will be different depending upon the distance from the center of the chip or the difference of the arrangement of the resistors 104 and 105 with respect to the X axis and Y axis which cross each other at a right angle.

[0097] Accordingly, when the polycrystalline silicon resistor or the diffusion resistor is used as the resistors 104 and 105, the variation value Δr1 and Δr2 will be varied in every IC package, since the ratios of Δr1 and Δr2 are not constant and the resistors 104 and 105 can not be formed on the same position on the chip in every IC package.

[0098] Further, the stress of the molding resin varies in accordance with the variation of the temperature (the lower the temperature, the larger the stress) whereby the value of the resistance is varied.

[0099] Conversely, when the Cr-Si-N thin film resistors 108 and 109 are used as the resistors 104 and 105, the variation of the resistance ΔR/R of this film after the resin molded packaging can be reduced to a point where it can be ignored, compared with that of the polycrystalline silicon resistor and the P’ diffusion resistor. Therefore, the output voltage Vout of the IC after the resin molded packaging can be controlled within the range of 5 ± 0.0075 V (0.15%).

[0100] Thus, in this embodiment, a constant voltage IC used for an automobile which is required to maintain the voltage at a high accuracy at 5 ± 0.025 V (0.5%), is produced by forming the resistors 104 and 105 with the Cr-Si-N thin film resistor and by packaging by resin molding method to thereby eliminate variations of the value of the resistance caused by variations of an atmospheric temperature after the packaging or before and after the resin molding process, in completed, and further, caused by the influence of stress variations of the molded resin due to temperature variations caused by heat generation can be suppressed.

[0101] Further, when a Cr-Si-N thin film resistor is used as the resistors 104 and 105 instead of the Cr-Si thin film resistor, this semiconductor can be used as an NiCo magnetic resistive device.

[0102] The semiconductor device using the thin film resistor of the present invention also can be used as a resistor provided on a portion of a 5 V power source IC used for automobile, without adjustment, other than the portion indicated in Figure 18.

[0103] Moreover, the value of the resistance can be externally adjusted to control variations of the resistance characteristics caused by stress of the molded resin due to temperature variations.

[0104] Further, although the semiconductor device using the thin film resistor of the present invention can be used for another type of resin molded package IC having a resistor, for example, an amplifying resistor in a differential amplifier or a resistor for setting a reference voltage in a voltage comparator or the like, variations of the characteristics thereof due to variations of the temperature will cause some problems.

[0105] Namely, the semiconductor device using the thin film resistor of the present invention can be used for resin molded package IC in which the resistance of each resistor used therein is kept at a constant value.

EFFECT OF THE INVENTION

[0106] According to the present invention, the following advantages can be obtained.

[0107] In the semiconductor device as shown above, a thin film resistor has a characteristic by which variations of the resistance value due to the temperature variations can be effectively suppressed.

[0108] Further, in the method of producing the semiconductor device having a thin film resistor as mentioned above, a thin film resistor having a characteristic in which variations of the resistance value due to the temperature variations are eliminated can be effectively produced.

[0109] Moreover, variations of the resistance value of the resistor provided in resin molded package IC chip caused by temperature variations and variations of the stress of the molded resin can be effectively suppressed.
Claims

1. A method of producing a semiconductor device having an amorphous thin film resistor which is formed on a substrate, has the same energy band construction as that of metal and comprises chromium, silicon and nitrogen, the amorphous thin film resistor forming process consisting essentially of the steps of preparing a target containing chromium and silicon, wherein the weight percentage of the silicon to the total weight of the chromium and silicon is 41 to 57 weight %, and reactive sputtering said substrate, utilizing said target in an atmosphere of an inert gas containing 1-2% nitrogen gas, wherein a thermal history of said amorphous thin film resistor applied after said thin film resistor forming process up to the final processing step is at temperatures less than 500 °C, to thereby maintain the amorphous condition of said thin film resistor.

2. A method of producing a semiconductor device according to claim 1, comprising a patterning step in which a Cr-Si-N thin film formed on said substrate during the reactive sputtering is etched to remove said film from the surface of said substrate except for the place on which said thin film resistor is finally provided, a wiring step in which, first, a conductive film is formed over the entire surface of said substrate utilizing a sputtering method and, subsequent, wirings are formed by etching said conductive film, wherein the thermal history includes a sintering step in which said wirings are sintered.

Patentansprüche


2. Verfahren zur Herstellung einer Halbleiteranordnung nach Anspruch 1, gekennzeichnet durch einen Strukturierungsschritt, bei welchem eine auf dem Substrat während des reaktiven Sputterns gebildete Cr-Si-N-Dünnschicht geätzt wird, um die Schicht von der Oberfläche des Substrats außer der Stelle zu entfernen, auf welcher der Dünnschichtwiderstand endgültig vorgesehen ist, einen Verdrahtungsschritt, bei welchem zuerst eine leitende Schicht über der gesamten Oberfläche des Substrats unter Verwendung eines Sputterverfahrens gebildet wird und darauffolgend Verdrahtungen durch Ätzen der leitenden Schicht gebildet werden, wobei die thermische Entwicklung einen Sinterschritt beinhaltet, bei welchem die Verdrahtungen gesintert werden.

Revendications

1. Procédé de fabrication d’un dispositif à semiconducteurs comportant une résistance à couche mince amorphe qui est formée sur un substrat, présente la même configuration de bande d’énergie que celle du métal, et comprend du chrome, du silicium et de l’azote, le procédé de fabrication de résistance à couche mince amorphe étant constitué essentiellement des étapes de préparation d’une cible contenant du chrome et du silicium, dans lequel le pourcentage en poids du silicium par rapport au poids total du chrome et du silicium est de 41 à 57 % en poids, et de pulvérisation réactive dudit substrat, en utilisant ladite cible dans une atmosphère de gaz inerte contenant de 1 à 2% de gaz azote, dans lequel un historique thermique de ladite résistance à couche mince amorphe appliqué après ladit procédé de fabrication de résistance à couche mince jusqu’à l’étape de traitement finale représente des températures inférieures à 500 °C, afin de maintenir ainsi l’état amorphe de ladite résistance à couche mince.

2. Procédé de fabrication d’un dispositif à semiconducteurs selon la revendication 1, comprenant une étape de formation de motif dans laquelle un film mince de Cr-Si-N formé sur le substrat durant la pulvérisation réactive est gravé pour éliminer le dit film de la surface du substrat à l’exception de l’emplacement sur lequel ladite résistance à couche mince est finalement prévue, une étape de câblage dans laquelle, tout d’abord, un film conducteur est formé sur la surface entière du dit substrat en utilisant un procédé de pulvérisation et, ensuite, des liaisons sont formées par la gravure dit film conducteur, dans lequel le dit historique thermique comprend une étape de frittage dans laquelle lesdites liaisons sont frittées.
Fig. 3

Fig. 4
**Fig. 10(a)**

![Graph showing the relationship between primary coefficient (ppm/°C) and nitrogen volume (%)](image)

**Fig. 10(b)**

![Graph showing the relationship between secondary coefficient (ppm/°C²) and nitrogen volume (%)](image)
Fig. 14(a)

- N₂ VOLUME 0%
- N₂ VOLUME 1.5%

FILM THICKNESS [Å]

PRIMARY COEFFICIENT [ppm/°C]
Fig. 15(a) $N_2 = 0$

Fig. 15(b) $N_2 = 1\%$

Fig. 15(c) $N_2 = 2\%$
Fig. 17
Fig. 19
**Fig. 20**

- **Cr-Si-N Thin Film**
- **Polly Crystalline Silicon**

Symbols:
- L_3 (K_L = 18.8)
- L_1 (K_L = 1.33)
- L_2 (K_T = -1.35)
- L_4 (K_T = -5.3)

Axes:
- \( \Delta R/R \) (Y-axis)
- STRAIN \( \varepsilon \) (X-axis)

Scale:
- \( x10^{-3} \) to 10 on the Y-axis
- \( x10^{-4} \) on the X-axis
Fig. 22

Shearing stress generated on the surface of an IC chip (kg/mm²)

Distance from the center of IC chip (mm) →
Fig. 23

Compressed Stress Generated on the Surface of a Chip (kg/mm²) vs Distance from the Center of IC Chip (mm)