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High-speed data latch with zero data hold time
Datenflip-flop mit einer Datenhaltezeit gleich Null
Bascule de donnée à haute vitesse avec un temps de maintien de donnée nul

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Proprietor: TEXAS INSTRUMENTS INCORPORATED
Dallas Texas 75265 (US)

Inventors:
• Krenik, William R.
  Dallas Texas (US)
• Hsu, Wei-Chan
  Plano Texas 75075 (US)

Representative: Abbott, David John et al
Abel & Imray
Northumberland House
303-306 High Holborn
London, WC1V 7LH (GB)

References cited:
EP-A- 0 293 923
US-A- 4 146 802


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Description

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to digital circuits, and more particularly to high-speed data latching circuits for temporarily storing digital information.

BACKGROUND OF THE INVENTION

Digital processing circuits often require latches for temporarily storing digital signals when transferring such signals between circuits. Such applications include high-speed A/D and D/A converters, high-speed memories, such as RAMs, ROMs, EPROMs, etc., high-speed pipelined logic circuits, and other applications.

Data latches are generally clocked to assure that the data being transferred is reliably stored, and that a coordinated transfer is accomplished without loss of data. In order to ensure that a data latch reliably stores digital signals presented at its input, such digital signal must be held at the latch input for a specified period of time during the input clocking cycle. The state of the digital signal appearing at the input of the latch during the noted period of time can then be reliably latched or stored in a flip-flop circuit internal to the latch. The specified period of time is termed the "hold time". The data is clocked and stored in the latch during such hold time, and thereafter the data on the input line of the latch can be changed without affecting the data stored within the latch.

High-speed data operations are optimized by minimizing the data hold time of the latches. Thus, the faster the data can be latched and stored, the processing of other digital circuits can commence for preparing updated or new inputs to the latches. High-speed CMOS data latches are currently available which operate at speeds up to twenty MHz. Such a latch is disclosed in the article "A CMOS 8-bit High-Speed A/D Converter IC", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-20, No. 3, p. 775, June, 1985. The disadvantage of such a latch circuit, however, is its extremely long hold time, thus limiting the speed with which the latch may be used with other circuits.

It can be seen that a need exists for an improved high-speed data latch with an extremely short data hold time so that such latch does not present a limitation when used with other high-speed circuits. An additional need exists for a memory sense amplifier data latch in which the hold time is so small that a single clock transition can be utilized to sense data on the data line as well as precharge the data line, thereby reducing the complexity of the clocking schemes in memory support circuits.

United States Patent No. 4 146 802 discloses a latching circuit with a node which is precharged by a precharge signal and discharged by the latching of a particular state in the latch. The node is connected to a control electrode of a transistor that lies in series with an input terminal of the latching circuit. The voltage at the node controls the operation of the transistor. An input signal at the input terminal can be locked out when the latching circuit is in a particular latched state.

According to the present invention there is provided a data latch circuit comprising

an input data section for receiving data input signals;
an input data storage flip-flop comprising two cross-connected transistors for receiving and storing data from said input data section;
an output data storage flip-flop having output conductors prechargeable to a predetermined state;

and means for transferring data from said input data storage flip-flop to said output data storage flip-flop, characterised in that said input data section comprises two circuits each comprising two transistors connected in series, one transistor in each circuit being responsive to a respective one of the input data signal and the input data signal inverted and the other transistor or in each circuit being responsive to the state of a respective one of the output conductors, each other transistor being rendered nonconducting by the respective output conductor not being in the predetermined state,

the two circuits being connected respectively in parallel with the transistors of the input data storage flip-flop, whereby said input data storage flip-flop can only change state in response to a data input signal when one of the output conductors is not in the predetermined state.

In an embodiment, the high-speed latch of the invention can be employed as a sense amplifier in a memory of the type utilizing prechargeable complementary bit lines. With such an arrangement, a single clock signal can serve as both the latch and precharge signal, thereby simplifying the clock system and making more efficient use of high-speed memory circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages will become more apparent from the following and more particular description of the preferred embodiment of the invention, as illustrated in the accompanying drawings in which like reference characters generally refer to the same parts or elements throughout the views, and in which:

FIG. 1 is an electrical schematic drawing of the high-speed latch, constructed according to the preferred embodiment of the invention; and
FIG. 2 is an electrical schematic drawing of an alternate embodiment of the invention well adapted
for semiconductor memory applications.

**DETAILED DESCRIPTION OF THE INVENTION**

With reference to FIG. 1, there is illustrated the high-speed latch constructed in accordance with the preferred embodiment of the invention. The latch includes an input data flip-flop 10, an output data flip-flop 12 and a transfer circuit 14 for coupling signals from the input data flip-flop 10 to the output data flip-flop 12.

More specifically, the input data flip-flop 10 comprises a number of N-channel transistors, of which two transistors 16 and 18 from a cross-coupled flip-flop. Associated with the input data flip-flop 10 is a data input 20 which functions to couple external data thereto. Preferably, the high-speed latch is constructed in a balanced manner, in which complementary data is coupled to the input data flip-flop 10. Hence, data appearing on the data input 20 is coupled as such via N-channel transistors 22 and 24 to the input data flip-flop 10. The complementary signal of the data input 20 is inverted by inverter 26 and coupled via transistors 28 and 30 to the input data flip-flop 10. As can be seen from FIG. 1, transistors 22 and 24 are bridged in series across flip-flop transistor 16, while transistors 28 and 30 are bridged in series across flip-flop transistor 18. Transistor 22 is controlled by the input data, while transistor 28 is controlled by the complement of the input data. Furthermore, the gates of transistors 24 and 30 are connected in a cross-coupled manner, forming a positive feedback path, to the output data flip-flop 12. A ground forms a common return or rail for the input data flip-flop 10.

Nodes 32 and 34, which define the output nodes of the input data flip-flop 10, are connected to respective output nodes 36 and 38 of the output data flip-flop 12 via respective transfer transistors 40 and 42. Transfer transistors 40 and 42 are of the N-channel type which are controlled by a signal on a latch input 44.

In the preferred form of the invention, the output data flip-flop 12 is constructed with P-channel transistors. Transistors 46 and 48 of the output data flip-flop 12 are connected in a cross-coupled manner to function as a flip-flop. The flip-flop transistors 46 and 48 are each connected between a positive supply voltage Vdd and the respective output nodes 36 and 38. Bridged across the flip-flop transistors 46 and 48 are respective precharge transistors 50 and 52. The gates of the precharge transistors 50 and 52 are also connected to the latch input 44, and are responsive to signals thereon for precharging the output nodes 36 and 38 substantially to the voltage Vdd. The output nodes 36 and 38 of the output data flip-flop 12 define a balanced and complementary output of the high-speed latch, as identified by reference numerals 54 and 56. The complementary outputs 54 and 56 of the high-speed data latch may be connected to other circuits through buffer or driver circuits (not shown).

The arrangement of the input data flip-flop 10, the output data flip-flop 12 and the transfer transistors of the transfer circuit 14 is rather conventional, as noted in the publication identified above. However, the understanding of the principles and concepts of the invention are best understood by presenting the entire operation of the high-speed data latch. In operation, the latch undergoes an initial precharge cycle in preparation of latching data therein. According to an important technical advantage of the invention, the data hold time of the latch is reduced substantially to a zero time period, defined by the condition in which a signal transition on the latch input 44 can function both as a precharge signal as well as the signal for inputting data into the latch. In practice, the hold time is less than about fifty picoseconds, which constitutes a portion of the clock signal rise time transition. Such a hold time is far less than that of data latches heretofore known.

The high-speed latch can be controlled by a single high-speed clock signal. For purposes of example, the clock signal on the latch input 44 is shown as a waveform having a 50% duty cycle. Because of the high-speed characteristics of the latch of the invention, such signal may control the latch operation upwardly at a rate of 200 MHz. During the logic low portion of the latch signal, precharge transistors 50 and 52 are driven into conduction, while transfer transistors 40 and 42 remain in a cutoff state. The conduction of precharge transistors 50 and 52 provides a path between the Vdd supply voltage and the output nodes 36 and 38, whereby such nodes are precharged to logic high level. During the logic low period of the latch signal, flip-flop transistors 16 and 18 of the input data section discharge the output nodes 32 and 34 thereof toward the ground potential. Depending on the threshold voltage of input flip-flop transistors 16 and 18, the associated nodes 32 and 34 drop to a voltage near the ground potential. Also, during the logic low state of the latch signal, the high-speed flip-flop is nonresponsive to input data.

During the rising transition of the latch signal on the latch input 44, the precharge transistors 50 and 52 are driven into cutoff, while the transfer transistors 40 and 42 are driven into conduction. Hence, the input data flip-flop 10 is connected to the output data flip-flop 12, via respective nodes 32, 36, 34, and 38. With nodes 36 and 38 precharged to logic high states, and during the rising transition of the latch signal, the data applied to the input data flip-flop 10 is prepared for transfer to the output data flip-flop 12.

Assuming, for purposes of example, that the data applied to the input data 20 is a logic high, transistor 22 will be driven into conduction, while transistor 28 will be cutoff. Associated series feedback transistors 24 and 30, due to their connection to the respective precharged output data flip-flop nodes 38 and 36, are both capable of conducting. As a result, with transistors 22 and 24 both conducting, node 32 will be essentially grounded, which potential is transferred through transistor 40 to thereby discharge the output data flip-flop node 36. On
the other hand, since transistor 28 is rendered nonconductive by the complement of the input data signal, node 34 cannot be discharged, thus leaving output data flip-flop node 38 precharged to a logic high. Nodes 34 and 38 thus slew to a logic high state, while nodes 32 and 36 slew toward a logic low state. The output data flip-flop 12 then presents complementary signals on the outputs 54 and 56. As noted above, buffers can be connected to the outputs 54 and 56 to provide complementary logic signals, with states approaching the \( V_{dd} \) and ground potentials.

It is important to realize that on the rising edge of the latch signal when data is presented to the input flip-flop 10, the nodes 36 and 38 of the output data flip-flop 12 begin slewing to definable states. During such slew transition, the inhibit transistors 24 and 30 are driven to respective opposite logic states. The opposite states of inhibit transistors 24 and 30, together with their serial connections to respective transistors 22 and 28, prevent a data change subsequent to the latch slew interval from affecting the logic state initially set into the output flip-flop 12.

For example, if data where to change on the data input 20 during the last part of the rising transition of the latch signal, as noted by reference numeral 60, such data change would not affect the initial state set into the output data flip-flop 12 during the slewing period. This is due primarily to the fact that at such point 60 in the latch signal transition, the data output flip-flop nodes 36 and 38 have slewed sufficiently in opposite directions to drive respective inhibit transistors 30 and 24 into opposite states of conduction. This situation then prevents an input data change, i.e., a logic low data state, on the data input 20 from changing the state initially set into the output data flip-flop 12.

In other words, if data on the data input 20 were to change from the high state to the low state during period 60 of the latch signal, transistor 22 would be driven into a state of nonconduction, while transistor 28 would be driven into a state of conduction. In this condition, inhibit transistor 24 would still be on, inhibit transistor 30 would be off, while transistor 22 would be on and transistor 28 would be on. It can be seen that as to the series connected transistors 22 and 24, one such transistor is off, as is the case with series connected transistors 28 and 30. Because at least one transistor in each feedback path is off, the feedback from the output flip-flop 12 to the input flip-flop 10 is broken. Thus, the change of state on the data input 20 has no affect on the logic state appearing at nodes 32 and 34, as initially established during the slewing time of the high-speed latch.

From the foregoing, it can also be appreciated that the precharge control and the data control input to the high-speed latch can be controlled with a single signal, i.e., be synchronous in nature. This eliminates the need for separate data input clock, as is necessary in many conventional latch circuits. This feature of the invention is highly advantageous in high-speed circuits such that a single high-speed clock can control all the latch operations. It can be appreciated that with the features and advantages of the present invention, high-speed signals do not need to be segmented or divided into other signals to provide delay periods to satisfy hold time requirements of the latches.

Other technical advantage of the invention include the option to construct input data flip-flop transistors 22 and 28 as large channel devices, without affecting the overall high-speed operation of the latch. In addition, transistors 46 and 48 can be constructed as narrow channel devices to reduce nodal capacitance, thereby optimizing the speed of the latch. Such changes in the structural features of the latch disclosed in the noted publication would adversely affect the speed and operation of such latch.

The features and advantages of the latch 61 of the invention can also be realized when used in connection with a semiconductor memory. The latch 61 shown in FIG. 2 is substantially identical to that illustrated in FIG. 1. FIG. 2 illustrates a latch application utilized in connection with a memory having complementary bit lines, such as shown by numerals 62 and 64. Such bit lines carry signals from a memory cell (not shown), which signals are also complementary in nature to reduce common node noise problems. The bit lines 62 and 64 are also of the type which are precharged by respective transistors 66 and 68. The bit line precharge transistors 66 and 68 are connected to a supply voltage \( V^+ \) which may typically be about one-half the magnitude of \( V_{dd} \). As noted, the bit line precharge transistors 66 and 68 are controlled by the inverse of the clock signal 70. Inverters 72 and 74 function to provide the inverse of the clock signal 70.

As the sense amplifier output nodes 36 and 38 are being precharged, one memory cell associated with the bit lines 62 and 64 is being read to output data on the bit lines 62 and 64 which were previously precharged. During the rising transition of the clock signal 70, and as described above, the precharged transistor 66 is driven into conduction to precharge the bit line 62. The same action also occurs with respect to the complementary bit line 64, wherein the precharge transistor 68 is driven into conduction. On the rising edge of the clock signal, the sense amplifier 61 slewstoward a stable state defined by the bit line memory signals, while at the same time the bit lines 62 and 64 undergo another precharge cycle. This synchronous operation is possible due to the exceedingly low hold time of the sense amplifier 61. Hence, data sensing and bit line precharging can begin substantially simultaneously, with precharging continuing for a full half clock cycle. It is apparent that the data on the bit lines is valid for only a few nanoseconds before being destroyed by the bit line precharging. As noted above, the advantage of this feature is that a single clock signal can control sense amplifier operation as well as bit line precharging. The technical advantage of this feature is that the memory can be run at a high-speed clock
rate, without further clock dividing to generate timing signals for assuring that specified data hold time requirements are met. By utilizing the latch of the invention, a memory read operation can be fully executed in a single clock cycle.

From the foregoing, disclosed is a high-speed data latch which provides a lockout of data changes input thereto, as soon as the latch begins slewing toward a definable stable state. A cross-coupled feedback path is provided between an input and output section of the latch during such slewing time period to sustain latchup of a final logic state. However, should the input data change subsequent to the slewing of the definable logic state, the positive feedback path is broken to prevent final latchup of a different logic state. In addition to the technical advantages noted above, the provision of the inhibit circuit of the invention can be easily and efficiently integrated with current semiconductor processing techniques. Indeed, the latch circuit can be constructed by fabricating the additional transistors in the same semiconductor well as the input data section of the latch. Notwithstanding, those skilled in the art may prefer to employ the features and advantages of the invention without resorting to the particular latch construction noted above.

Therefore, while the preferred embodiment of the invention has been disclosed with reference to several specific constructions, it is to be understood that many changes in detail may be made as a matter of engineering choices without departing from the scope of the invention, as defined by the appended claims.

Claims

1. A data latch circuit comprising

an input data section (20, 22, 24, 26, 29, 30) for receiving data input signals;
an input data storage flip-flop (10, 16, 18) comprising two cross-connected transistors (16, 18) for receiving and storing data from said input data section;
an output data storage flip-flop (12, 46, 48) having output conductors (54, 56) prechargeable to a predetermined state; and

means (40, 42) for transferring data from said input data storage flip-flop to said output data storage flip-flop, characterised in that said input data section comprises two circuits (22, 24, 28, 30) each comprising two transistors connected in series, one transistor (22 or 28) in each circuit being responsive to a respective one of the input data signal and the input data signal inverted and the other transistor (24 or 30) in each circuit being responsive to the state of a respective one of the output conductors (56 or 54), each other transistor (24, 30) being rendered non-conducting by the respective output conductor not being in the predetermined state,

the two circuits (22, 24, 28, 30) being connected respectively in parallel with the transistors (16, 18) of the input data storage flip-flop, whereby said input data storage flip-flop cannot change state in response to a data input signal when one of the output conductors (54, 56) is not in the predetermined state.

2. A data latch circuit according to claim 1 in which the output data storage flip-flop comprises two cross-connected transistors (46, 48) with two other transistors (50, 52) respectively connected from the output conductor (54, 56) to a reference voltage supply (Vdd) and responsive to a latch signal to precharge the output conductors to the predetermined state.

3. A data latch circuit according to claim 1 or claim 2 in which the transferring means comprises two transistors (40, 42) respectively connected from the output conductors (54, 56) to the cross-connected transistors (16, 18) of the input storage flip-flop and rendered conducting after the output conductors have been precharged.

4. A data latch circuit according to claim 2 with the features of claim 3 wherein the transistors (40, 42) of the transferring means are rendered conducting by the latch signal when the other transistors (50, 52) of the output data storage flip-flop are not conducting.

5. A data latch circuit according to any one of the preceding claims wherein the input data storage flip-flop transistors (16, 18) and the transistors (22, 24, 28, 30) of the input data section are N-channel transistors, and transistors (46, 48) of the output data storage flip-flop are P-channel transistors.

6. A memory including a data latch circuit according to any one of the preceding claims.

7. A memory according to claim 6 wherein the data latch circuit provides a sense amplifier.

Patentansprüche

1. Datenzwischenspeicherschaltung, mit

einem Eingangsdatenabschnitt (20, 22, 24, 26, 28, 30) für den Empfang von Dateneingangssignalen;
einem Eingangsdaten-Speicherflipflop (10, 16, 18), das zwei kreuzeckkoppelte Transistoren (16, 18) zum Empfangen und Speichern von vom Eingangsdatenabschnitt eingegebenen
Daten enthält; einem Ausgangsdaten-Speicherflipflop (12, 46, 48) mit Ausgangsleitern (54, 56), die im voraus auf einen vorgegebenen Zustand geladen werden können; und einer Einrichtung (40, 42) zum Übertragen von Daten vom Eingangsdaten-Speicherflipflop an das Ausgangsdaten-Speicherflipflop, dadurch gekennzeichnet, daß der Eingangsdatenabschnitt zwei Schaltungen (22, 24, 28, 30) enthält, wovon jede zwei in Serie geschaltete Transistoren umfaßt, wobei ein Transistor (22 oder 28) in jeder Schaltung entweder auf das Eingangsdatensignal oder auf das invertierte Eingangsdatensignal anspricht und der andere Transistor (24 oder 30) in jeder Schaltung auf den Zustand eines entsprechenden der Ausgangsleiter (56 oder 54) anspricht, wobei jeder andere Transistor (24, 30) durch den entsprechenden Ausgangsleiter, der sich nicht im vorgegebenen Zustand befindet, nichtleitend gemacht wird, wobei die zwei Schaltungen (22, 24, 28, 30) jeweils mit den Transistoren (16, 18) des Eingangsdaten-Speicherflipflops parallelgeschaltet sind, wobei das Eingangsdaten-Speicherflipflop seinen Zustand als Antwort auf ein Dateneingangsdiagnose nicht ändern kann, wenn sich einer der Ausgangsleiter (54, 56) nicht in dem vorgegebenen Zustand befindet.

2. Datenzwischenspeicherschaltung nach Anspruch 1, in der das Ausgangsdaten-Speicherflipflop zwei kreuzgekoppelte Transistoren (46, 48) enthält, wobei zwischen einen entsprechenden der Ausgangsleitung (54, 56) und eine Referenzspannungsversorgung (Vdd) zwei andere Transistoren (50, 52) geschaltet sind, die auf ein Zwischenspeichersignal ansprechen, um die Ausgangsleitung im voraus auf den vorgegebenen Zustand zu laden.

3. Datenzwischenspeicherschaltung nach Anspruch 1 oder Anspruch 2, in der die Übertragungseinzugabe zwischen Transistoren (40, 42) enthält, die zwischen einen entsprechenden der Ausgangsleitung (54, 56) und die kreuzgekoppelten Transistoren (16, 18) des Eingangs-Speicherflipflops geschaltet sind und leitend gemacht werden, nachdem die Ausgangsleitung vorgeladen worden sind.

4. Datenzwischenspeicherschaltung nach Anspruch 2 mit den Merkmalen des Anspruches 3, in der die Transistoren (40, 42) der Übertragungseinzugabe durch das Zwischenspeichersignal leitend gemacht werden, wenn die anderen Transistoren (50, 52) des Ausgangsdaten-Speicherflipflops nichtleitend sind.

5. Datenzwischenspeicherschaltung nach irgendeinem der vorangegangenen Ansprüche, in der die Eingangsdaten-Speicherflipflop-Transistoren (16, 18) und die Transistoren (22, 24, 28, 30) des Eingangsdatenabschnitts N-Kanal-Transistoren sind und die Transistoren (46, 48) des Ausgangsdaten-Speicherflipflops P-Kanal-Transistoren sind.


7. Speicher nach Anspruch 6, in dem die Datenzwischenspeicherschaltung einen Leseverstärker schafft.

Revalidations

1. Circuit de verrouillage de données comprenant

   une section de données d'entrée (20, 22, 24, 28, 30) pour recevoir des signaux d'entrée de données;
   une bascule bistable (10, 16, 18) de mémorisation de données d'entrée comprenant deux transistors (16, 18) connectés selon un couplage croisé et servant à recevoir et mémoriser des données provenant de ladite section de données d'entrée;
   une bascule bistable (12, 46, 48) de mémorisation de données de sortie, comportant des conducteurs de sortie (54, 56) pouvant être préchargés à un état prédéterminé, et des moyens (40, 42) pour transférer des données depuis ladite bascule bistable de mémorisation de données d'entrée à ladite bascule bistable de mémorisation de données de sortie,
   caractérisé en ce que ladite section de données d'entrée comprend deux circuits (22, 24, 28, 30) comprenant chacun deux transistors branchés en série, un transistor (22 ou 28) dans chaque circuit étant sensible à l'un respectif du signal de données d'entrée et du signal de données d'entrée inversé, et l'autre transistor (24 ou 30) dans chaque circuit étant sensible à l'état de l'un respectif des conducteurs de sortie (54 ou 56), chaque autre transistor (24, 30) étant rendu non conducteur par le conducteur de sortie respectif qui n'est pas dans l'état prédéterminé, les deux circuits (22, 24, 28, 30) étant connectés respectivement en parallèle aux transistors (16, 18) de la bascule bistable de mémorisation de données d'entrée, ladite bascule bistable de mémorisation de données d'entrée ne pouvant
pas changer d'état en réponse à un signal d'entrée de données lorsque l'un des conducteurs de sortie (54,56) n'est pas dans l'état prédéterminé.

2. Circuit de verrouillage de données selon la revendication 1, dans lequel la bascule bistable de mémorisation de données de sortie comprend deux transistors (46,48) connectés selon un couplage croisé et deux autres transistors (50,52) connectés respectivement entre le conducteur de sortie (54,56) et une source de tension de référence (Vdd), et apte à répondre à un signal de verrouillage pour précharger les conducteurs de sortie dans l'état prédéterminé.

3. Circuit de verrouillage de données selon la revendication 1 ou 2, dans lequel les moyens de transfert comprennent deux transistors (40,42) connectés respectivement entre les conducteurs de sortie (54,56) et les transistors (16,18), connectés selon un couplage croisé, de la bascule bistable de mémorisation d'entrée, et rendus conducteurs après que les conducteurs de sortie ont été préchargés.

4. Circuit de verrouillage de données selon la revendication 2, comportant les caractéristiques de la revendication 3, dans lequel les transistors (40,42) des moyens de transfert sont rendus conducteurs par le signal de verrouillage lorsque les autres transistors (50,51) de la bascule bistable de mémorisation des données de sortie ne sont pas conducteurs.

5. Circuit de verrouillage de données selon l'une quelconque des revendications précédentes, dans lequel les transistors (16,18) de la bascule bistable de mémorisation de données d'entrée et les transistors (22,24,28,30) de la section de données d'entrée sont des transistors à canal N, et les transistors (46,48) de la bascule bistable de mémorisation de données de sortie sont des transistors à canal P.


7. Mémoire selon la revendication 6, dans laquelle le circuit de verrouillage de données forme un amplificateur de détection.
FIG. 1

FIG. 2