A programmable logic array.

Priority: 13.08.86 US 896050

Date of publication of application: 24.02.88 Bulletin 88/08

Publication of the grant of the patent: 09.10.91 Bulletin 91/41

Designated Contracting States: DE FR GB IT

References cited:
EP-A-0 093 947
EP-A-0 178 437
DE-A-3 413 139
US-A-4 202 695

IBM TECHNICAL DISCLOSURE BULLETIN, vol. 26, no. 9, February 1986 "High Performance Cmos Logic Gate" pages 3994-3995

IBM TECHNICAL DISCLOSURE BULLETIN, vol. 26, no. 12, May 1984 J.P.STRECK "Charge-Conserving Bit Line Boost Circuit" pages 6318-6321

Proprietor: International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504(US)

Inventor: Masleid, Robert Paul
1400 Doonesbury Drive
Austin Texas 78758(US)
Inventor: Schmookler, Martin Stanley
7504 Rockpoint Drive
Austin Texas 78731(US)

Representative: Burt, Roger James, Dr.
IBM United Kingdom Limited Intellectual
Property Department Hursley Park
Winchester Hampshire SO21 2JN(GB)

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid (Art. 89(1) European patent convention).
Description

This invention relates to a programmable logic array.

Programmable logic arrays are used in digital computers to provide pre-programmed output data. Common types of programmed logic arrays include read-only memories (ROM) and programmed array logic (PAL). Furthermore, the programmed logic arrays are common in microprocessors, microcomputers and micro-controllers for storing data. These programmable logic arrays include a series of parallel word lines that are addressed by an input decoder circuit. An example is the address decode circuit of a ROM that decodes an input address to activate one of a series of word lines of the array. The input lines, word lines, are positioned orthogonally to, but not electrically connecting, a series of parallel bit lines. The bit lines actually provide the output signal from the array. Existing read-only memories provide either pull-up or pull-down resistors tied to these bit lines. These pull-up or pull-down resistors are connected to a potential source resulting in a potential present on the bit lines. The array itself includes programmable devices that are positioned in selected locations to pull-down or pull-up the potential on the bit line when a selected word line is activated. In this manner, the programmed elements in the array control the output signals present on the bit lines. The absence of a programmable element at an array intersection also provides an output since the absence of the device will result in the intersection bit line being unaffected by a specific word line being selected.

The disadvantage of using pull-up or pull-down resistors is that (1) a significant transition time is present because each bit line must be discharged (if the bit line is to be discharged) before the output of the bit lines can be read, and (2) the array uses DC power whenever the bit lines are active.

It is presently common to implement the programmed logic arrays as an array including field effect transistors such as CMOS type transistors. The pull-up (or pull down) resistors and the programmable devices are both field effect transistors. The pull-up device is configured to function as a resistor. The resistance of the pull-up device together with the switching transistor devices in the programmed logic array result in a ratio voltage divider circuit where the pull-up resistor has a minimum resistance necessary to enable the programmable devices to pull down the voltage level. The higher the voltage level, the longer the transition time required to change a bit line from one output state to another. Of course, a low output voltage level may be difficult to detect for state transition determination. Therefore, this voltage ratio structure always presents the designer with this trade off dilemma.

The present invention seeks to provide a programmable logic array with fast access times and low direct current power requirements.

Application of the present invention provides a means of designing a programmable logic array wherein the output bit lines are actively pulled up or down by the programmable elements as required by the data. In other words, no resistive pull-up or pull-down devices are used. Therefore, the output signals change state faster and the programmed logic array dissipates power only during output state transition. While this arrangement may require more area on the surface of a semiconductor device compared with an equivalent programmed logic array with resistive pull-ups or pull-downs, this disadvantage is offset when faster access time or lower direct current power usage is required and wherein the use of clock load devices or output differential amplifier circuits are not desirable.

According to one aspect the invention provides a programmable logic array comprising: a plurality of electrically isolated input lines; input means for addressing said plurality of input lines and directing a selection signal to an addressed one thereof; a plurality of electrically isolated output lines positioned to form a plurality of nonconductive intersections with said input lines; and an individual transistor disposed at each intersection, the control electrode of the transistor being connected to one of the input lines and one current flow electrode of the transistor being connected to the output line at the said intersection and the other current flow electrode of the transistor being connected to a selected one of two voltage levels, the selection being made in the course of programming the array, whereby a programmed logic output signal is obtained on the output line to which said one current flow electrode is connected when a selection signal is directed to an addressed input line.

Other aspects of the invention are defined in the claims appended hereto.

How the invention can be carried out will now be described by way of example, with reference to the accompanying drawings, wherein:

Fig. 1 is a schematic diagram of a prior art logic array implemented with pull-up devices;
Fig. 2 is a schematic diagram of one embodiment of the invention providing field effect transistors connected to true and complement lines of the input line;
Fig. 3 is a schematic diagram of a second embodiment of the invention wherein each output/input intersection includes two field effect devices;
Fig. 4 is a schematic diagram of a third embodiment having the transistors of one polarity posi-
tioned in the logic array with output signal energy provided with the array element in conjunction with a switching transistor of opposite channel polarity; and

Fig. 5 is a schematic diagram of a fourth embodiment having selected field effect transistors connected to the input line to receive the input signal and output signal energy.

This invention requires that only one input line in a logic array be active at any one time. This condition is commonly true for ROMs. It will be also shown that such conditions may be provided for programmable array logic devices (PAL). Fig. 1 represents the prior art method of providing signal output as known from EP-A-O 093 947 for example. In Fig. 1, an address decode circuit 12 is provided to receive an input address via lines 10. The address on lines 10 can be either serial or parallel. The received address is decoded by the address decode circuit 12 to activate one of word lines 14, 16, and 18. Word lines 14, 16, and 18 are positioned parallel to each other and orthogonally to a series of bit lines 20, 22, and 24 that provide the output signals for the array. Three word lines 14, 16 and 18 and three bit lines 20, 22, and 24 are shown in Fig. 1. Any number of bit lines and/or word lines may be provided. Programming the word line/bit line intersections is provided by placing field effect transistors such as transistors 32, 36, 40, 46 and 48 each connecting an individual word line to an individual bit line. Furthermore, the transistors 32, 36, 40, 46 and 48 are connected to a ground potential. There are no transistor devices at intersections 34, 38, 42, and 44. Additionally, each of the bit lines 20, 22, and 24 includes a pull-up transistor device 26, 28 and 30 respectively. As previously discussed, these transistor devices 26, 28 and 30 act as pull-up resistors. In other words, the voltage present at one terminal of the pull-up devices 26, 28 and 30 is provided to the respective bit line. Therefore, before any programming devices such as transistors 32, 36, 40, 46 and 48 are activated, the output on the bit lines 20, 22, and 24 are high or 1.

In operation, when a word line is selected and activated, the voltage on the word line switches the gates of the transistor device connected to that word line to remove the potential from its respectively connected bit line. For example, if word line 18 was activated, the gates of transistors 32 and 48 would remove the potentials from bit lines 20 and 24 respectively. Therefore, the output on line 20 would be low or a 0, the output of line 22 would be high or a 1, and the output of line 24 would be low or a 0. Note that the output of bit line 22 is high because there is not a transistor present at intersection 36. Therefore, the logic array is programmed by placing the transistors such as transistors 32, 36, 40, 46 and 48 in respective preselected intersections where the output of one state is required and omitting such transistor devices from the intersections where the output of the opposite state is required.

As previously discussed, outputting a 0 will cause a voltage drain since the pull-up resistive device and its connected voltage supply are essentially being connected to ground during the bit line read time thus generating a current drain across the pull-up resistive element and the switching element to ground. Increasing the resistance of the pull-up resistive device or the switching device will decrease the amount of current drain. However, this will also increase the amount of transition time required before the proper output states can be achieved on the bit lines resulting in slower response time of the programmable logic array.

Fig. 2 illustrates an embodiment of the present invention wherein each of the word lines 54, 56, 58 and 60 is connected to an individual driver 62, 64, 66 and 68. The output of the drivers 62, 64, 66 and 68 are true and complement lines. The true lines 70, 74, 78 and 82 are connected to the gate of a programmable device having a channel of one polarity while the complement lines 72, 76, 80 and 84 are connected to the gates of transistors having channels of the opposite polarity. Additionally, the true line devices, such as N channel transistors 86, 92, 98 and 100, are connected to ground while the complement line devices, the P channel transistors 88, 90, 102 and 104 are connected to a potential. Note that each intersection only includes one transistor. The word lines 54, 56, 58 and 60 are in turn connected to an address decoder 50 that is connected to an address input line 52. The address decoder 50 and address input line 52 function as discussed in the array of Fig. 1. In Fig. 2, the bit lines 94 and 96 are connected to each transistor of its word line intersections. Therefore, if the true side of the word line is high, the presence of a N channel transistor, such as transistor 86, will drive the bit line 94 low. On the other hand, a complement signal on line 76 will switch transistor 88 to provide a positive potential on bit line 94. Therefore, either state change for a specific word line will result in a positive potential or ground potential being actively placed on the respective bit line. Since the bit line is either totally discharged by an N channel transistor, such as transistor 86, or actively charged, such as by transistor 88, no DC power is required after the transition of the word lines.

Also, although the N channel transistors 86, 92, 98 and 100 and the P channel transistors 88, 90, 102 and 104 are shown as if they are in the same cell locations in the array, they may actually be in physically separate arrays with corresponding bit
lines connecting together which would reduce the area required for providing isolation between these devices having channels of opposite polarities. Therefore, the advantage of the circuit illustrated in Fig. 2 is that it provides a fast switching speed with only one device pulling either high or low at the time resulting in no DC power consumption. However, the disadvantage is that more devices, such as the true and complement line drivers and the additional transistors, are required.

In Fig. 3, each intersection includes a P channel transistor and a N channel transistor. Both devices are connected to either ground or a positive potential depending on the program data. Thus, both devices help pull either the bit line up or down resulting in faster operation due to this increased drive. The disadvantage is that the capacitance on the bit line is also increased. Another disadvantage may be the greater difficulty in selectively connecting the devices to either ground or the positive potential. However, as in Fig. 2, separate physical arrays may be used for the P channel and N channel devices. Referring to Fig. 3, the address decoder 122 is connected to an address input line 120. The address decoder 122 and address input line 120 function in the same manner as in the embodiment of Fig. 2. Word lines 124, 126, 128 and 130 connected to address decoder 120 are also connected to true and complement line drivers 132, 134, 136 and 138, also as in the previous embodiment. The true lines 140, 144, 148 and 152 are connected to N channel transistors 158, 178, and 180, 180 and 162, 182 and 164, 184 respectively. Likewise, the complement lines 142, 146, 150 and 154 are connected to P channel transistors 168, 188 and 170, 190 and 172, 192 and 174, 194 respectively. The programming of the intersections is provided by connecting the respective transistors to either the positive potential or ground. Therefore, if word line 124 were selected, the gates of transistors 158 and 168 would be activated pulling bit line 168 down. Likewise, the gates of transistors 178 and 188 would be activated pulling bit line 188 down. Therefore, the output when word line 124 is activated is a 0 on line 168 and a 0 on line 188. If word line 126 was activated, the gates of transistors 160 and 170 would be active placing a potential on line 168. The gates of transistors 180 and 190 would also be activated placing a ground potential on line 188. Therefore, the output on lines 168 and 188 would be 1 and 0, respectively.

The advantage of the array in Fig. 3 is that metal layers would be used to program the transistors by connecting the transistors to either ground or the positive voltage level. Also, since all transistors are always present, a faster manufacturing turnaround would result. However, the disadvantages include the fact that a higher number of transistors are required resulting in an additional capacitance.

Fig. 4 includes an array of single N channel transistor devices 212, 214, 216, 218, 230, 232, 234 and 236. Each of these devices is programmable by selectively connecting it to either ground or the positive potential. When the device is connected to the positive potential, it can only pull its output bit line to the potential minus the device threshold voltage. Therefore, some type of output buffer or output amplifier may be needed, such as a differential amplifier, such as common in RAMs, or an inverter, with device ratios chosen so that the N channel device will overpower the corresponding P channel device when switched. Further, one might use a P channel device with a greater threshold voltage than the N channel device. However, such solutions result in direct current power being dissipated when the bit lines are being read. The solution illustrated in Fig. 4 provides a pull-up P channel transistor with an inverter with the inverter output fed back to the gate of the P channel device. Thus, once the inverter output is pulled down, the P channel device turns on and pulls the inverter input up.

Referring to Fig. 4 for an example, if the gate of transistor 212 is activated by word line 204, transistor 212 will pull down bit line 220 to the ground potential. However, if word line 206 is activated, the gate of transistor 214 will be activated placing a voltage on bit line 220 that is equal to the original potential connected to transistor 214 minus the threshold voltage of transistor 214. This potential on bit line 220 is sufficient to transition transistor 224 placing a positive potential on the gate of transistor 222 resulting in a voltage present on bit line 220. Note that when transistor 212 is activated grounding bit line 220 that transistor 222 is off thus isolating the bit line 220 at ground potential from the positive potential preventing DC power dissipation during the time that the bit lines are being read. The advantage of the array in Fig. 4 is that the array is compact requiring only N channel devices. Further, no direct current power is dissipated during bit line output. However, the disadvantage is that a ratio design is required since the N channel devices in the array must dominate the P channel pull-up devices 222 and 228.

Figure 5 illustrates a further embodiment, in which the field effect transistors 262, 270, 276 and 278 are each connected to ground, a word line and a bit line, similar to their counterparts in Figure 4. However, in Figure 5, transistors 264, 268, 280 and 282 each include terminals that are connected to the word lines instead of a voltage source such as +V in Figure 4. Specifically, transistor 264 includes a source line 265 that is connected to word line
256. Additionally, transistor 284 includes a gate 283 also connected to the same word line 256. In this embodiment, the respective word line that is active provides the potential for the output signal on the respective bit line 272 or 274. In the embodiment in Figure 5, the outputs on lines 272 and 274 are of sufficient power to drive an NMOS channel device. Therefore, no further voltage stabilisation need be required if an NMOS device is to be driven. Additionally, a transistor structure such as illustrated in Figure 4 (including transistors 222, 224, and 226) may also be included to provide extra output voltage on the bit lines 272 and 274. Additionally, lines 272 and 274 may be connected to drive NMOS inverters to provide a higher signal output. The advantage of the configuration in Figure 5 is that the transistors 264, 268, 280 and 282 do not require independent connections to a voltage such as +V in Figure 5. However, the word line 254, 256, 258 and 260 must be capable of providing an adequate output signal for the respective bit lines 272 and 274.

Since programmed array logic or PALs are very similar to ROMs, the programmed array logic inventions as illustrated may be implemented with PALs. In a PAL, the address decoder is equivalent to the product term or AND array. In the PAL, the output of the AND array may activate more than one line. To implement the invention, the output of the AND array must be constrained such that the output on the product term lines are mutually exclusive, i.e., only one line at a time is active. Therefore, one would require that a PAL whose product terms are not mutually exclusive be re-defined so that the product terms are mutually exclusive. This will usually require more AND logic in the AND array. For example, if a PAL contains the output functions F1 = aeb + aebcd and F2 = ced the product terms aeb and ced are not mutually exclusive since both would produce an active output when the signal aebcd is 1. However, the functions may be implemented to provide mutually exclusive inputs. For example:

F1 = aebcd + aebcd + aebcd
F2 = aebcd + aebcd + aebcd

requiring five AND gates, namely (aebcd), (aebcd), aebcd), (aebcd), (aebcd), and (aebcd).

Concerning physical layout, it may appear that a satisfactory layout could be achieved by inter-leaving P channel device columns and N channel device columns or reversing the P channel device and N channel devices for every other bit position so that the P channel devices of one bit were adjacent to the P channel devices of the next bit while the N channel devices are adjacent to the N channel devices of the next bit in the other direction. However, this requires considerable space to provide the appropriate isolation between the N channel devices and the P channel devices (to prevent PNPN latchup). Less space would be needed if separate physical arrays are used as previously discussed having corresponding bit lines connected together with global wiring. A slight disadvantage to this is the extra capacitance due to having the separate bit lines in each array.

**Claims**

1. A programmable logic array comprising:

   a plurality of electrically isolated input lines (e.g. 204, 206, 208, 210 respectively 254, 256, 258, 260)

   input means (200 respectively 250) for addressing said plurality of input lines and directing a selection signal to an addressed one thereof;

   a plurality of electrically isolated output lines (220, 228) positioned to form a plurality of nonconductive intersections with said input lines; and

   an individual field effect transistor (212, 214, 216, 218, 230, 232, 234, 236 respectively 282, 284, 286-282) disposed at each intersection, the control electrode of the transistor being connected to one of the input lines and one current flow electrode of the transistor being connected to the output line at the said intersection (200, 228 respectively 272, 274) and the other current flow electrode of the transistor being connected to a selected one of two voltage levels (GND, +V respectively 254-260) selection being made in the course of programming the array, whereby a programmed logic output signal is obtained in the output line to which said one current flow electrode is connected when a selection signal is directed to an addressed input line.

2. An array as claimed in claim 1, in which the transistor is driven into a conducting state when the input line is selected.

3. An array as claimed in claim 1 or claim 2, in which all of the transistors disposed at the intersections are of one channel polarity, and in which each of the output lines is connected to a potential source through a transistor of opposite channel polarity to that of the transistors disposed at the intersections.
4. A programmable logic array comprising a plurality of true and complement pairs (140-154) of electrically isolated input lines;  

input means (122) for addressing said pair of input lines and directing true and complement selection signals to an addressed pair thereof;  

a plurality of electrically isolated output lines (168, 186) positioned to form a plurality of non-conductive intersections with said pairs of input lines; and  

an individual pair of CMOS transistors (e.g., 158, 168) disposed at each intersection, the control electrodes of the CMOS transistor pair being connected to a respective one of the pair of input lines and one current flow electrode of each transistor of the CMOS pair being connected to the output line at the said intersection (and the other current flow electrodes of the CMOS transistor pairs being connected to the same one of a selected one of two potential sources (GND, + V), the selection being made in the course of programming the array, whereby a programmed logic output signal is obtained on the output line to which said one current flow electrodes of the transistor pair is connected when a selection signal is directed to an addressed input line pair.

5. A programmable logic array comprising a plurality of true and complement pairs (70,72,74,78) of electrically isolated input lines;  

input means (50) for addressing said pairs of input lines and directing a selection signal to an addressed pair thereof;  

a plurality of electrically isolated output lines (94,96) positioned to form a plurality of non-conductive intersections with said pairs of input lines; and  

an individual field effect transistor (86-104) disposed at each intersection, the control electrode of the transistor being connected to one line of the pair of input lines and one current flow electrode of the transistor being connected to the output line at the said intersection and the other current flow electrode of the transistor being connected to a selected one of two potential sources (GND, + V), the selection being made in the course of programming the array, whereby a programmed logic output signal is obtained on the output line to which said one current flow electrode of the transistor is connected when a selection signal is directed to an addressed input line pair.

Revendications

1. Réseau logique programmable comprenant :  
une pluralité de lignes d’entrée électriquement isolées (par exemple 204,206,208,210 respectivement 254,256,258,260) ;  
des moyens d’entrée (200 respectivement 250) pour l’adressage de ladite pluralité de lignes d’entrée et l’envoi d’un signal de sélection à une ligne d’entrée adressée ;  
une pluralité de lignes de sortie électriquement isolées (220,228) disposées de manière à former une pluralité d’intersections non conductrices avec lesdites lignes d’entrée ; et  
un transistor à effet de champ individuel (212, 214,216,218,230,232,234,236, respectivement 262,264,268, 282) disposé à chaque intersection, l’électrode de commande du transistors étant connectée à une des lignes d’entrée, une électrode de circulation de courant du transistor étant connectée à la ligne de sortie à ladite intersection (220,228 respectivement 272,274) et l’autre électrode de circulation de courant du transistor étant connectée à un niveau choisi de deux niveaux de tension (terre, + V respectivement 254-260) ; la sélection étant effectuée au cours de la programmation du réseau de sortie qu’un signal de sortie logique programmée est obtenue sur la ligne de sortie à laquelle ladite première électrode de circulation de courant est connectée, lorsqu’un signal de sélection est appliqué à une ligne d’entrée adressée.

2. Réseau suivant la revendication 1, dans lequel le transistor est activé un état conducteur lorsque la ligne d’entrée est sélectionnée.

3. Réseau suivant la revendication 1 ou la revendication 2, dans lequel tous les transistors disposés aux intersections sont d’une même polarité de canal, et dans lequel chaque des lignes de sortie est connectée à une source de potentiel par un transistor de polarité de canal opposée à celle des transistors disposés aux intersections.

4. Réseau logique programmable comprenant une pluralité de paires de lignes d’entrée électriquement isolées vraies et de complément (140-154) ;  
des moyens d’entrée (122) pour l’adressage de ladite paire de lignes d’entrée et l’application de signaux de sélection vrais et de complément à une paire de lignes adressées ;  
une pluralité de lignes de sortie électriquement isolées (166,186) disposées de manière à former une pluralité d’intersections non conductrices avec lesdites paires de lignes.
d'entrée ; et
une paire individuelle de transistors CMOS (par exemple 158,188) disposés à chaque intersec-
5
tion, les électrodes de commande de la paire de transistors CMOS étant connectées à
une ligne respective de la paire de lignes d'entrée , une électrode de circulation de cour-
rant de chaque transistor de la paire de tran-
sistors CMOS étant connectée à la ligne de
sortie à ladite intersection et les autres électro-
des de circulation de courant des deux transis-
tors CMOS étant connectées à la même sour-
ce choisie parmi deux sources de potentiel
(terre, +V), la sélection étant effectuée en
cours de programmation du réseau, de sorte
15
qu'un signal de sortie logique programmée est
obtenu sur la ligne de sortie à laquelle les
dites premières électrodes de circulation de
courant de la paire de transistors sont connec-
tées lorsqu'un signal de sélection est envoyé à
20
une paire de lignes d'entrée adressée.

5. Réseau logique programmable comprenant
une pluralité de paires de lignes d'entrée
electriquement isolées vraies et de complé-
ment (70,72, 74,76);
25
des moyens d'entrée (50) pour l'adressage
des dites paires de lignes d'entrée et l'envoi
d'un signal de sélection à une paire de lignes
adressée ;
une pluralité de lignes de sortie électriquement
isolées (94,96) disposées de manière à
30
former une pluralité d'intersections non
conductrices avec lesdites paires de ligne
d'entrée ; et
un transistor à effet de champ individuel
(86-104) disposé à chaque intersection, l'élec-
35
trode de commande du transistor étant
connectée à une ligne de la paire de lignes
d'entrée, une première électrode de circulation de
courant du transistor étant connectée à la
ligne de sortie à ladite intersection et l'autre
electrode de circulation de courant du transis-
tor étant connectée à une source choisie de
deux sources de potentiel (terre, + V), la sélec-
tion étant effectuée dans le cours de la pro-
grammation du réseau, de sorte qu'un signal de
40
sortie logique programmée est obtenu sur la
ligne de sortie à laquelle ladite première élect-
trode de circulation de courant du transistor
est connectée lorsqu'un signal de sélection est
appliqué à une paire de lignes d'entrée adress-
ées.

Patentansprüche

1. Programmierbare logische Anordnung, die auf-
weist:
eine Mehrzahl elektrisch isolierter Eingangslei-
tungen (bspw. 204, 206, 208, 210 bzw. 254,
256, 258, 260),

Eingangsmittel (200 bzw. 250) zum Adressie-
ren der Mehrzahl von Eingangsleitungen und
tum Leiten eines Auswahlsignals zu einer adressedierten derselben.

eine Mehrzahl elektrisch isolierter Ausgangslei-
tungen (220, 228), die angebracht sind, um
eine Mehrzahl nichtleitender Kreuzungen mit
den Eingangsleitungen zu bilden und
einen einzelnen Feldeffekttransistor (212, 214,
216, 218, 230, 232, 234, 236 bzw. 262, 264,
268 - 282), der bei jeder Kreuzung angeordnet
45
ist, wobei die Steuerelektrode des Transistors
mit einer der Eingangsleitungen verbunden ist
und die eine Stromfluß-Elektrode des Transis-
tors mit der Ausgangsleitung bei der Kreu-
zung (200, 228 bzw. 272, 274) verbunden ist
und die andere Stromfluß-Elektrode des Transis-
tors an einen ausgewählten zweiter Span-
nungspegel (GND, + V bzw. 254 - 260) gelegt
49
ist, wobei eine Auswahl im Laufe des Program-
mierens der Anordnung getroffen wird, wo-
durch ein programmieretes logisches Ausgangs-
signal auf der Ausgangsleitung erhalten wird,
mit welcher die Stromfluß-Elektrode verbunden
50
ist, wenn ein Auswahlsignal zu einer adressier-
ten Eingangsleitung geleitet wird.

2. Anordnung nach Anspruch 1, bei welcher der
Transistor in den leitenden Zustand getrieben
55
wird, wenn die Eingangsleitung ausgewählt wird.

3. Anordnung nach Anspruch 1 oder Anspruch 2,
bei welcher alle an den Kreuzungen angeord-
ten Transistoren eines Kanaltypes sind und
bei welcher jede der Ausgangsleitungen an
eine Spannungsquelle durch einen Transistor
56
eines Kanaltypes gelegt ist, der mit jenem an
den Kreuzungen angeordneten Transistoren un-
gleichnamig ist.

4. Programmierbare logische Anordnung, die auf-
weist: eine Mehrzahl wahrer und komplementä-
er Paare (140 - 154) elektrisch isolierter Eingangs-
leitungen,

Eingangsmittel (122) zum Adressieren des

Paares von Eingangsleitungen und zum Leiten
wahrer und komplementärer Auswahlsignale zu
60
einem adressierten dieser Paare,
tungen (166, 186), die angebracht sind, um eine Mehrzahl nichtleitender Kreuzungen mit den Paaren von Eingangsleitungen zu bilden und

ein einzelnes Paar von CMOS-Transistoren (bspw. 158, 168), das bei jeder Kreuzung angeordnet ist, wobei die Steuerelektroden des CMOS-Transistor-Paares mit einem entsprechenden Paar von Eingangsleitungen verbunden ist und eine Stromflußelektrode jedes Transistors des CMOS-Paares mit der Ausgangsleitung bei der Kreuzung verbunden ist und die anderen Stromfluß-Elektroden der CMOS-Transistor-Paare an dieselbe eine ausgewählte zweier Spannungsquellen (GND, +V) gelegt sind, wobei die Auswahl im Laufe des Programmierens der Anordnung getroffen wird, wodurch ein programmiertes logisches Ausgangssignal auf der Ausgangsleitung erhalten wird, mit welcher die Stromfluß-Elektrode des Transistorpaares verbunden ist, wenn ein Auswahlsignal zu einem adressierten Eingangsleitungsbaar geleitet ist.

5. Programmierbare logische Anordnung, die aufweist: eine Mehrzahl wahrer und komplementärer Paare (70, 72, 74, 76) elektrisch isolierter Eingangsleitungen,

Eingangsmittel (50) zum Adressieren der Paare von Eingangsleitungen und zum Leiten eines Auswahlsignales zu einem adressierten dieser Paare,

eine Mehrzahl elektrisch isolierter Ausgangsleitungen (94, 98), die angebracht sind, um eine Mehrzahl nicht leitender Kreuzungen mit den Paaren von Eingangsleitungen zu bilden und

einen einzelnen Feldeffekttransistor (98 - 104), der bei jeder Kreuzung angeordnet ist, wobei die Steuerelektrode des Transistors mit einer Leitung des Paars von Eingangsleitungen verbunden ist und eine Stromflußelektrode des Transistors mit der Ausgangsleitung bei der Kreuzung verbunden ist und die andere Stromfluß-Elektrode des Transistors an eine ausgewählte zweier Spannungsquellen (GND, +V) gelegt ist, wobei die Auswahl im Laufe des Programmierens der Anordnung getroffen wird, wodurch ein programmiertes logisches Ausgangssignal auf der Ausgangsleitung erhalten wird, mit welcher die eine Stromfluß-Elektrode des Transistors verbunden ist, wenn ein Auswahlsignal zu einem adressierten Eingangsleitungsbaar geleitet ist.
FIG. 4

PRIOR ART
FIG. 2
FIG. 3
FIG. 5