Method and apparatus for testing electronic equipment.

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Description

The present invention relates to a digital circuit arrangement for testing electronic circuitry, comprising a microprocessor including a digital memory, control means, clock means and display means, and further comprising an address bus having a first address bus portion connected to the microprocessor, address buffer means which connect the first address bus portion to a second address bus portion and permit the transfer of voltage signals at least from the first address bus portion to the second address bus portion, a data bus having a first data bus portion connected to the microprocessor, data buffer means which connect the first data bus portion to a second data bus portion and permit the transfer of voltage signals both from the first data bus portion to the second data bus portion, and from the second data bus portion to the first data bus portion, and connection means which permit the interconnection of the electronic circuitry between the second address bus portion and the second data bus portion.

The invention further relates to a method for testing electronic circuitry.

As modern electronic equipment becomes more and more complex, so too have the methods by which its operation is tested. Testing may be done by factory personnel (for quality control purposes) at the time of manufacture, by service technicians at the time of routine maintenance and repair, and by users in the course of operating the equipment. In microprocessor based systems, there may exist means for “self-testing”. Certain diagnostic procedures may be carried out automatically upon power-up, or upon user demand.

In digital systems under microprocessor control, one may identify four types (levels) of testing that are commonly carried out: two levels of automatic testing, and two levels of manual testing. At one level of automatic testing, (the program level), there may exist, either in software or firmware, a monitor or other routine such as a debugging program including error-trapping routines which generate diagnostic messages upon finding a system error or fault condition. However, such messages often do not distinguish between program error and circuit/hardware fault.

At another level of automatic testing (the logic state level), concern is with the bit flow relative to the system clock and with specified bit patterns. Selected patterns (both stimulus and response pattern) may be either pre-stored or generated algorithmically. Examination of such bit patterns constitutes a data domain analysis, and may be carried out using either an external digital or logic state analyzer, or circuits which perform somewhat similar functions within the system itself. Like program testing, however, data domain analysis provides only limited information, insufficient to pinpoint the causes of erroneous bits that may appear in a response pattern.

One manual type of testing, (e.g., testing using a digital probe at selected circuit nodes) is used to indicate faulty logic conditions (ones and zeroes) in a circuit. Such testing is not limited to points that may have been addressed in a pre-programmed analysis (automatic testing data domain analysis), but may be extended to test specific transistors, resistors or capacitors. This testing may be done while the system (equipment) is operating, as in the case of a program or data domain analysis, or not operating (e.g., operation may have been suspended and a local “operation” simulated using a digital pulser). In either case, manual testing is usually performed following a prescribed trouble-shooting sequence, in order to identify faulty circuits and, ultimately, one or more faulty components, so that repair or replacement can be carried out.

Another manual type of testing is DC voltage testing, in which logical operations are ignored, and DC voltages are applied and examined. For example, if digital probing revealed a faulty logic condition indicative of a faulty voltage level, the above-mentioned trouble-shooting sequence may call for a testing for leaky transistors or capacitors at a predetermined site with a voltmeter.

What is needed and would be useful, therefore, is a test system/method which would automate digital probe testing and DC voltage testing.

From EP-A-135 009 of earlier priority but not published previously (Art 54(3) EPC), there is known an arrangement and method for testing a microprocessor system in which in addition to the main microprocessor to be tested a control microprocessor is provided. The control microprocessor has a memory of its own, a display unit and an interface circuitry which provides the connection of the control microprocessor to the main microprocessor. During the test procedure the control microprocessor has access to the address bus and the data bus of the main microprocessor. The control microprocessor first performs a self-test before testing the further elements of the testing arrangement formed by it and the entire circuitry associated with the main microprocessor. Thereafter the control microprocessor again transfers the control to the main microprocessor which on its part carries out a self-test. In the known arrangement, however, the address bus and the data bus cannot be tested independently of the circuitry connected thereto.

It is an object of the invention to indicate a digital circuit arrangement for testing electronic circuitry which is not only capable of testing itself but also allows testing of the data and address paths leading to the electronic circuitry to be tested.

It is a further object of the invention to indicate a method which allows testing of the address and data paths of an electronic circuitry to be tested independently of the test of the circuitry.

In accordance with the invention this object is accomplished by a digital circuit arrangement of the aforementioned kind characterized in that a
portion, but not all of the digital memory is connected to the first address bus portion and the first data bus portion, that the address buffer means and the data buffer means not only permit the transfer of voltage signals but connect the first bus portion to the second bus portion so as to isolate electrically the first bus portion from the second bus portion, that data latch means are provided which connect from the first data bus portion to the second data bus portion, and that address latch means are provided which connect from the second address bus portion to the second data bus portion, so as to isolate electrically the second address bus portion from the second data bus portion, but permitting the capture by said address latch means of voltage signals from the second address bus portion, and further permitting the reading through the data bus portion of the voltage signals so captured.

The present invention provides a digital circuit arrangement for testing the components of an electronic system automatically, obviating the need for manual digital probe testing and DC voltage testing. More particularly, the present invention provides a means for measuring, under microprocessor control, voltages at specific nodes in an electronic circuit, in order to test the operation of equipment containing that circuit, whether digital or analog. The circuit arrangement according to the invention comprises a microprocessor or a portion (subsystem) thereof, a digital memory, preferably in the form of a read-only memory (ROM), buffers and a latch, all of which define a central "kernel", including an addressing capability. The buffers provide isolation of the circuit component under test. The latch acts as a state machine in determining the state of the component so isolated. The ROM may contain either a look-up table or pre-determined stimulus and response data, or one or more algorithms for generating such stimulus and response data. In cases where the equipment ordinarily contains a microprocessor, a particular subset of its instructions may be employed for purposes of functional control of such measurements. In other cases, a microprocessor especially designed for the purpose of such control may be added to the equipment.

The method of testing employed by the invention includes the steps of first testing the kernel itself, and then any busses connected to the kernel. The method then tests in sequence those components of the circuitry for which addressing has been provided in order to determine their voltage states, and then compares the levels so obtained with the expected levels derived from the ROM, so as to test the circuit operation. In a more detailed embodiment of the invention, the addition of analog-to-digital converters (ADC's) to the kernel in order to form a voltage comparator allows the testing of specific voltage values at selected, addressable circuit nodes. In that case, the reference data derived from the ROM comprises nominal voltage values, or acceptable ranges thereof, as would be expected in properly functioning equipment.

The invention is illustrated in detail hereinafter by means of a drawing. The drawing shows

Figure 1A a block diagram showing a microprocessor controlled system of the prior art;

Figure 1B a block diagram showing a microprocessor-controlled test system of the present invention and

Figures 2-4 flow charts illustrating the method of the invention.

In Figure 1A there is shown a conventional CPU card 1 comprising a microprocessor 10 including an arithmetic-logic unit (ALU) 10a, read-only memory (ROM) 10b and registers 10c, together with address buffer 11 leading to address bus 12 and data buffer 13 leading to data bus 14.

Also shown are cards 2, 3 and 4 which will typically connect through a backplane (not shown) to address bus 12 and data bus 14. Cards 2, 3 and 4 will typically contain random-access memory (RAM), disk or CRT controllers, or similar circuitry necessary to carry out other functions in computer or other electronic equipment. Some of such circuitry may also be mounted directly on the CPU card. A control bus (not shown) interconnects the several cards. Said control bus connects through a control buffer (not shown) which provides electrical isolation thereof. Display or indicating means (not shown) must also be provided in order that the results of the testing procedures, as well as the operation of the equipment itself, may be observed.

Address buffer 11 and data buffer 13 ordinarily serve the purpose of driving digital signals onto the respective address bus 12 and data bus 14, on which there may exist a large fan-out requiring substantial power. Data buffer 13 will also be configured to transfer digital signals from the data bus 14 back through to the microprocessor 10. The ROM 10b contains the micro-encoded instructions which will carry out these several addressing and data read/write functions derived from some program source (not shown), which may be additional ROM or RAM.

In operation, or upon manufacture, it may occur that one or more of the cards 2, 3 and 4 will develop a malfunction which will prevent proper operation of the equipment. As noted earlier, there may be conveyed to the ROM 10b, and under the control of an external or internal digital clock (not shown), a set of instructions particularly designed for testing the system operation. However, a malfunction in any of microprocessor 10, address buffer 11, address bus 12, data buffer 13 or data bus 14 could prevent such a testing routine from being carried out. Furthermore, in the prior art configuration of Fig. 1A, without disconnecting components there would be no way of determining in which of said components the malfunction had occurred. It is principally this difficulty that the present invention solves.
Figure 1B then shows a modified card 1' and associated components which embody the invention. Corresponding component numbers in Figures 1A and 1B have the same meaning. However, the unidirectional address buffer 11 of Fig. 1A may be modified in the invention to form the bidirectional address buffer 11' of Fig. 1B. Address buffer 11' and data buffer 13 will then be of the same bidirectional type. By such change, the devices on cards 2, 3 or 4 are enabled to address the ROM 15, as in the case of a DMA controller seeking control information.

The embodiment of the invention shown in Fig. 1B also adds an additional ROM 15 and the latches 16 and 17. Use of the additional ROM 15 allows for the storage or generation of extensive test data, as will be described further below, without overtaxing the microprocessor ROM 10b. The additional ROM 15 also allows for greater design flexibility in that it may be field programmable, or alternate versions thereof may be provided, either by switching between such alternate versions all mounted on the CPU card 1', or by interchanging various ROM chips 15 in a single mount. The further addition of data latch 16 and address latch 17, which comprise essentially D latches having an additional, three-level output enable circuit, then allows the method of the invention to be carried out. As will be noted further below, address latch 17 also incorporates means for selecting individual address cycles out of the bit flow on address bus 12.

Operation of the circuit of Fig. 1B for test purposes then centers around the use of a "kernel" comprising the microprocessor 10, the additional ROM 15, and the sides of address buffer 11', data buffer 13 and data latch 16 which face said ROM 15. Such operation is made possible in part by an additional feature of address buffer 11' and data buffer 13 (as well as the control buffer, not shown). While ordinarily used simply as bus drivers because of their power capabilities, these buffers also act to isolate the devices which they interconnect. In the present case, they respectively isolate the kernel from the address bus 12 and the data bus 14 (and said control bus). The data latch 16 provides similar isolation. The kernel itself may then be tested in isolation, and so too may be the individual buses and as many of the remaining circuit components as may be individually addressed. A sequence of tests that may be conducted is shown in Fig. 2.

As noted, the "level 0" test of the kernel may amount simply to a check sum of the kernel ROM 15. That simplicity results because the kernel has been reduced to a minimum number of parts. If such a test performs correctly, the microprocessor 10 will be functioning properly, the kernel ROM 15 will have been properly programmed, and there will exist no short or open circuits within either the microprocessor 10, the kernel ROM 15, or the wiring which interconnects these devices. Similarly, there will exist at least no short circuits within the input sides of address buffer 11', data buffer 13, or data latch 16 (or of the control buffer, not shown) or the wiring leading thereto. The remaining tests can then be carried out, using the appropriate latches and buffers in each case.

In testing address bus 12 or data bus 14, the method of the invention will typically transfer a particular data pattern to the address latch 17 or the data latch 16, respectively, and then determine whether the data pattern so transferred may be recovered intact from latch into which it was placed. In testing any additional circuitry that is connected to the address bus and data bus, a data pattern may be transferred as a stimulus to one set of addressable points, and then a response data pattern so caused may be taken from a different set of addressable points, all of said points being located within the particular circuit or sub-circuit then under test.

Thus, the subsequent "level 1" test, as shown in more detail in Fig. 3, may be seen to involve the use of data latch 16 and data buffer 13 in addition to the microprocessor 10 and the kernel ROM 15. A particular table of bit patterns within the kernel ROM 15 may be designated as appropriate to this level 1 test, and the microprocessor 10 will then first select such a level 1 test pattern table within the kernel ROM 15. From that table, the microprocessor 10 will also select a particular data pattern and write it into the data latch 16. That data pattern will then be read back into the microprocessor 10 through the data buffer 13. A correct match to the original data pattern will then indicate that there exist no open or short circuits on the kernel sides of data latch 16 or data buffer 13, nor any open or short circuits within those parts of data latch 16 or data buffer 13 which lie outside of the kernel. To establish the entirety of that information, there may exist within the kernel ROM 15 a sequence of test patterns which may be employed successively as noted in Fig. 3. Such test patterns will of course be designed to pinpoint the individual bit line or lines within which a malfunction occurs.

As can be seen in Fig. 1B, the level 1 test also requires the use of data bus 14, or at least connection thereto. A successful test will indicate that there are no short circuits in data bus 14, nor indeed in any of the components or cards 2, 3 or 4 which connect directly to data bus 14. If a short does appear, it will be necessary as in the case of the prior art to begin removing cards in order to pinpoint the origin of the short, i.e., within data bus 14, the backplane (not shown), or within one of such cards. During such testing, the kernel itself will continue to function properly as before. Consequently, unlike the prior art in this case the particular bit line or lines in which the short occurs will be known. It will also be known that the address bus 12 or the components of cards 2, 3 or 4 which connect directly to address bus 12 (or indeed any of such components except those connecting to data bus 14) will not be involved.

In a very similar fashion, the address bus 12 and its associated components are tested at level 2 as shown in Fig. 4. However, since a microprocessor
such as 10 is not ordinarily configured to write out
and read in addresses as it would data, it is
necessary to use the data bus 14 and its asso-
ciated components in order to carry out the level 2
test of the address circuitry. It is for that reason,
of course, that the level 1 test of the date circuitry is
conducted first. Specifically, after a particular test
pattern has been selected by the microprocessor
10 as before, and as now shown in Fig. 4, the
address latch 17 will be used to bring data from
the address bus 12 across to the data bus 14. As in
the previous case of the level 1 test outlined in
Fig. 3, said data will then be transmitted through
the data buffer 13 to the kernel ROM 15 for
comparison to the original data pattern.
When executing the instructions of a program,
microprocessor 10 will ordinarily proceed
through a series of data and fetch cycles, the
addresses for which will appear on address bus
12. In carrying out the level 2 test, microprocessor
10 will cycle through a series of bit patterns
derived from the kernel ROM 15, and said bit
patterns will likewise be reflected on address bus
12. In the method of the level 2 test, said bit
patterns are treated as addresses, and are cap-
tured as such on selected data cycles by address
latch 17. Said treatment and capture of said bit
patterns through conceptually distinguishable
and being shown as so distinguished in steps d
and e of Fig 4, may in fact be executed by a single
set of instructions. When a particular bit pattern
has been so captured, it is then read from the
address latch 17 through the data buffer 13 and
compared to the original data pattern in the
manner of the level 1 test shown in Fig. 3.

In Table 1 below there is then set forth a series
of assembly language instructions applicable to
the particular case of the M68000 microprocessor
which will carry out the level 1 and level 2 tests,
respectively. Since the assembly language
mnemonics are quite general, the procedure is
clearly adaptable to other microprocessors. It
should also be mentioned here that in the case of
a microprocessor system which employs only a
single, multiplexed bus (other than the control
bus), said multiplexed bus would correspond to
the data bus 14 of Fig. 1B. In the same figure,
address buffer 11', address bus 12 and address
latch 17 would then be superfluous, and there
would occur no test corresponding to the level 2
test of the present case.

| TABLE 1 |
| Test level 1 (Fig. 3) |
| LEA Test_pattern, A0 | a |
| LOOP1: MOVE (A0)+, D0 | b |
| MOVE D0, DATA_LATCH | c |
| MOVE DATA_LATCH, D1 | d |
| CMP D0,D1 | e |
| BNE ERROR | f |
| CMP #ENDTEST,A0 | g |
| BNE LOOP1 | h |
| ;TO NEXT TEST LEVEL |

| Test level 2 (Fig. 4) |
| LEA Test_pattern,A0 | a |
| LOOP2: MOVE (A0)+,D0 | b |
| MOVE #0,SETUP | c |
| MOVE D0,A1 | d |
| MOVE (A1),D1 | e |
| MOVE ADRS_LATCH,D2 | f |
| CMP D0,D2 | g |
| BNE ERROR | h |
| CMP #END TEST,A0 | i |
| BNE LOOP2 | j |
| ;TO NEXT TEST LEVEL |
Successful completion of the testing at levels 0, 1 and 2 then establishes that the kernel, the associated buffers and latches, and address bus 12 and data bus 14 are all functioning properly. In addition, there are no short circuits in any of the cards 2, 3 or 4 such as would short out either address bus 12 or data bus 14. That is the necessary condition for being able to carry out the logic state or data domain analysis mentioned earlier. Testing at levels 0, 1 and 2 alone requires a minimum investment in apparatus which may be incorporated into virtually any system.

A data domain analysis may also be conducted using the apparatus of the present invention, as shown in Fig. 1B, but employing the procedures of the prior art. None of either the kernel ROM 15, the data latch 16 or the address latch 17 need be involved in such prior art testing. Also, the fact that the unidirectional address buffer 11 of Fig. 1A may be changed to the bidirectional address buffer 11' of Fig. 1B will not affect the use of the latter in a unidirectional mode for such purpose. Programs written for use in the prior art configuration of Fig. 1A may then be employed in the configuration of the present invention shown in Fig. 1B with little or no change, and will thus constitute the level 3 test shown in Fig. 2. The difference which the present invention imposes is that at the time of such prior art testing, the electrical integrity of the buses to be employed will already have been independently confirmed. Such testing may show that there are no open circuits leading to cards 2, 3 or 4, and that they display correct digital patterns.

As noted earlier, a logic state analysis is ordinarily constrained to read only HI and LO voltage levels, which may then appear as '1's and '0's (or as disassembled equivalents thereof) in a video display. A digital probe, on the other hand, will often be configured to indicate "bad" or intermediate voltage levels as well, when said probe is touched to a circuit component that exhibits such a fault. In an additional embodiment of the present invention, the circuit of Fig. 1B may be modified to accommodate not only "bad" voltage levels, but also the actual voltage values existing at each addressable circuit node. This is accomplished by incorporating analog-to-digital converters (ADC's) to feed into the data buffer 13 and the address buffer 11', or at similar convenient locations. When using an ADC with a parallel output, one may reduce the number of lines leading on to the microprocessor 10 and any intervening components by also adding a parallel-to-serial converter to the output of each such ADC.

Use of the present method to replace fully the manual procedures set forth in the typical troubleshooting routine for voltage testing would require a substantial increase in the addressing capability of the microprocessor 10 and the associated ROM. There would also be required an increase in the decoding capability at each of the cards 2, 3 or 4, and in the wiring of such cards to connect to the points of interest. At the same time, to carry out tests at levels 0, 1 and 2 requires the use of only a few instructions, of which the M68000 microprocessor, for example, includes some 56 basic types. Particularly in the case of electronic equipment that is entirely analog in nature, and would otherwise contain no digital circuitry, one may then employ a modification of the circuit of Fig. 1B in which the microprocessor 10 has been designed for testing purposes only. A very minimal need in terms of an instruction set then allows substantial expansion in terms of addressing capability.

It is then apparent that while the method and apparatus of the present invention have been described in terms of a particular embodiment, and with special reference to the M68000 microprocessor, the invention itself will be easily adaptable to other configurations, or to other microprocessors, by those having ordinary skill in the art. It will then be appreciated that the invention is not limited to the particular embodiments which have been shown and described, but may be adapted within the scope of the appended claims or equivalents thereof. In particular, the present invention incorporates no limitations on such matters as the size of the memory arrays or the types of memory devices used.

Claims

1. Digital circuit arrangement for testing electronic circuitry, comprising a microprocessor (10) including a digital memory (10c, 15), control means (10a), clock means and display means, and further comprising an address bus (12) having a first address bus portion connected to the microprocessor (10), address buffer means (11) which connect the first address bus portion to a second address bus portion and permit the transfer of voltage signals at least from the first address bus portion to the second address bus portion, a data bus (14) having a first data bus portion connected to the microprocessor (10), data buffer means (13) which connect the first data bus portion to a second data bus portion and permit the transfer of voltage signals both from the first data bus portion to the second data bus portion, and from the second data bus portion to the first data bus portion, and connection means which permit the interconnection of the electronic circuitry (2, 3, 4) between the second address bus portion and the second data bus portion characterized in that a portion (15), but not all of the digital memory (10c, 15) is connected to the first address bus portion and the first data bus portion, that the address buffer means (11') and the data buffer means (13) not only permit the transfer of voltage signals but connect the first bus portion to the second bus portion so as to isolate electrically the first bus.
portion from the second bus portion, that data latch means (16) are provided which connect from the first data bus portion to the second data bus portion, so as to isolate electrically the first data bus portion from the second data bus portion, but permitting the transfer of voltage signals at least from the first data bus portion to the second data bus portion, and that address latch means (17) are provided which connect from the second address bus portion to the second data bus portion, so as to isolate electrically the second address bus portion from the second data bus portion, but permitting the capture by said address latch means of voltage signals from the second address bus portion, and further permitting the reading through the data bus portion of the voltage signals so captured.

2. Digital circuit arrangement according to claim 1, characterized by analog-to-digital converter means connecting from said second address bus portion to said address buffer means; and analog-to-digital converter means connecting from said second data bus portion to said data buffer means.

3. Method for testing the electrical condition of an electronic circuitry (2, 3, 4) interconnected between an address bus (12) and a data bus (14), comprising the steps of conducting a verification test upon a digital memory portion (15) wherein there is stored a body of test data, transferring a portion of the test data to the electronic circuitry (2, 3, 4), receiving back from the electronic circuitry (2, 3, 4) a portion of response data and comparing the portion of response data to the portion of test data, characterized in that after the step of conducting the verification test and before the step of transferring test data to the electronic circuitry (2, 3, 4) the following steps are carried out:

transferring a first portion of the test data to the data bus (14), receiving back from the data bus (14) a first portion of response data, and comparing the first portion of response data to the first portion of test data, and transferring a second portion of said test data to the address bus (12), receiving back from the address bus (12) a second portion of response data, and comparing the second portion of response data to the second portion of test data.

4. Method according to claim 3, characterized in that the step of transferring test data to the data bus comprises the steps of

a. selecting from a first portion of a digital memory (10c, 15) an instruction sequence defining a data bus test mode;
b. selecting from a second portion of the digital memory a table of test patterns;
c. selecting from said table of test patterns a particular test pattern;
d. writing the particular test pattern into a data latch (16) through a portion of the data bus (12); e. reading from said data latch (16) a response pattern back through said portion of the data bus (14);
f. comparing the response pattern to the particular test pattern; and

g. repeating the steps c through f as necessary to test the entirety of the data bus (14).

5. Method according to claim 3 or 4, characterized in that the step of transferring test data to the address bus comprises the steps of

a. selecting from a first portion of a digital memory (10c, 15) an instruction sequence defining an address bus test mode;
b. selecting from a second portion of the digital memory (10c, 15) a table of test patterns;
c. selecting from the table of test patterns a particular test pattern;
d. transferring the particular test pattern as an address onto the address bus (12);
e. capturing the particular test pattern as an address into an address latch (17);
f. reading from the address latch (17) a response pattern;
g. comparing the response pattern to the particular test pattern; and
h. repeating said steps c through g as necessary to test the entirety of the address bus (12).

Patentansprüche

1. Digitale Schaltungsanordnung zum prüfen einer elektronischen Schaltung mit einem Mikroprozessor (10), der einen digitalen Speicher (10b,15) einschließt, Steuereinrichtungen (10a), Taktgeber-und Anzeigeinrichtungen und weiterhin mit einer Adressenleitung (12), die einen ersten Adressenleitungssteil aufweist, der mit dem Mikroprozessor (10) verbunden ist, Adressenpuffer-einrichtungen (11), die den ersten Adressenleitungssteil mit einem zweiten Adressenleitungssteil verbinden und die Übertragung von Spannungssignalen sowohl vom ersten Datenleitungssteil auf den ersten Datenleitungssteil auf den zweiten Datenleitungssteil erlauben, einer Datenleitung (14), die einen ersten Datenleitungssteil aufweist, der mit dem Mikroprozessor (10) verbunden ist, Datenpuffer-einrichtungen (13), die den ersten Datenleitungssteil mit einem zweiten Datenleitungssteil verbinden und die Übertragung von Spannungssignalen sowohl vom ersten Datenleitungssteil auf den zweiten Datenleitungssteil als auch vom zweiten Datenleitungssteil auf den ersten Datenleitungssteil erlauben, und Verbindungseinrichtungen, die es ermöglichen, die elektronische Schaltung (2,3,4) zwischen den Adressenleitungssteil und den zweiten Datenleitungssteil zu schalten, dadurch gekennzeichnet, daß ein Teil (15) des digitalen Speichers (10c,15) jedoch nicht der gesamte digitale Speicher (10c,15) mit dem ersten Adressenleitungssteil und dem ersten Datenleitungssteil verbunden ist, daß die Adressenpuffer-einrichtungen (11) und die Datenpuffer-einrichtungen (13) nicht nur die Übertragung von Spannungssignalen erlauben sondern den ersten Leitungssteil mit dem zweiten Leitungssteil so verbinden, daß der erste Leitungssteil vom zweiten Leitungssteil elektrisch isoliert ist, Datenverarbeitungseinrichtungen (16) vorgesehen sind, die den


4. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß der Schritt der Übertragung der Testdaten auf die Datenleitung die Schritte umfaßt:
   a) Wählen einer einen Datenleitungstest bestimmenden Befehlsfolge von einem ersten Teil eines digitalen Speichers (10c, 15),
   b) Wählen einer Tabelle von Testmustern von einem zweiten Teil des digitalen Speichers,
   c) Wählen eines bestimmten Testmusters von der Testmustertabelle,
   d) Schreiben des bestimmten Testmusters über einen Teil der Datenleitung (12) in ein Datenverriegelungsglied (16),
   e) Rücklesen über diesen Teil der Datenleitung (14) ein Antwortmuster vom Datenverriegelungsglied (16),
   f) Vergleichen des Antwortmusters mit dem bestimmten Testmuster, und
   g) Wiederholen der Schritte c) bis f) in der erforderlichen Weise, um die gesamte Datenleitung (14) zu prüfen.

5. Verfahren nach Anspruch 3 oder 4, dadurch gekennzeichnet, daß der Schritt der Übertragung von Testdaten auf die Adressenleitung die Schritte umfaßt:
   a) Wählen einer einen Adressenleitungstest bestimmenden Befehlsfolge von einem ersten Teil eines digitalen Speichers (10c, 15),
   b) Wählen einer Tabelle von Testmustern von einem zweiten Teil des digitalen Speichers (10c, 15),
   c) Wählen eines bestimmten Testmusters von der Testmustertabelle,
   d) Übertragen des bestimmten Testmusters als eine Adresse auf die Adressenleitung (12),
   e) Einfangen des bestimmten Testmusters als eine Adresse in ein Adressenverriegelungsglied (17),
   f) Lesen eines Antwortmusters vom Adressenverriegelungsglied (17),
   g) Vergleichen des Antwortmusters mit dem bestimmten Testmuster und
   h) Wiederholen der Schritte c) bis g) in der notwendigen Weise, um die gesamte Adressenleitung (12) zu prüfen.

Revendications

1. Schéma de circuit numérique pour tester une circuiterie électronique, comprenant un microprocesseur (10) comprenant une mémoire numérique (10b, 15), des moyens de commande (10a), des moyens formant horloge et des moyens de visualisation, et comprenant en outre un bus d'adresses (12) ayant une première région de bus d'adresses reliée au microprocesseur (10), des moyens formant mémoire tampon d'adresses (11') qui relient la première région de bus d'adresses à une seconde région de bus d'adresses et permettent le transfert de signaux de tension au moins de la première région de bus d'adresses vers la seconde région de bus d'adresses, un bus de données (14) ayant une première région de bus de données reliée au microprocesseur (10), des moyens formant mémoire tampon de données (13) qui relient la première région de bus de données à une seconde région de bus de données et permettent le transfert de signaux de tension à la fois de la première région de bus de données vers la seconde région de bus de données, et de la seconde région de bus de données vers la première région de bus de données et des moyens de connexion qui permettent l'interconnexion de la circuiterie électronique (2, 3, 4) entre la seconde région de bus d'adresses et la seconde région de bus de données, caractérisé en ce que une région
(15), mais non pas toute la mémoire numérique (10c, 15) est reliée à la première région de bus d'adresses et à la première région de bus de données, en ce que les moyens formant mémoire tampon d'adresses (11) et les moyens formant mémoire tampon de données (13) permettent non seulement le transfert de signaux de tension mais relient aussi la première région de bus à la seconde région de bus de manière à isoler électriquement la première région de bus de données de la seconde région de bus de données, de manière à isoler électriquement la première région de bus de données de la seconde région de bus de données, mais permettant le transfert de signaux de tension au moins de la première région de bus de données vers la seconde région de bus de données, en ce que des moyens formant registre de stockage de données (16) sont prévus pour relier la première région de bus de données à la seconde région de bus de données, de manière à isoler électriquement la première région de bus de données de la seconde région de bus de données et permettant en outre la lecture par la région de bus de données des signaux de tension aîné acquis.

2. Schéma de circuit numérique selon la revendication 1, caractérisé en ce que des moyens formant convertisseur analogique numérique relient la seconde région de bus d'adresses auxdits moyens formant mémoire tampon d'adresses, et en ce que des moyens formant convertisseur analogique numérique relient la seconde région de bus de données aux moyens formant mémoire tampon de données.

3. Procédé pour tester l'état électrique d'une ciruité électronique (2, 3, 4), interconnectée entre un bus d'adresses (12) et un bus de données (14), comprenant les étapes consistent à réaliser un test de vérification sur une région de mémoire numérique (15) dans laquelle on a stocké un ensemble de données de test, à transférer une partie des données de test vers la ciruité électronique (2, 3, 4), à recevoir en retour de la ciruité électronique (2, 3, 4), une partie de données de réponse, à comparer la partie de données de réponse à la partie de données de test, caractérisé en ce qu'après l'étape consistant à conduire le test de vérification et avant l'étape consistant à transférer les données de test vers la ciruité électronique (2, 3, 4), on met en œuvre les étapes suivantes consistant à transférer une première partie des données de test vers le bus de données (14), à recevoir en retour du bus de données (14) une première partie de données de réponse et à comparer la première partie de données de réponse à la première partie de données de test, et à transférer une seconde partie des données de test vers le bus d'adresses (12), à recevoir en retour du bus d'adresses (12) une seconde partie de données de réponse, et à comparer la seconde partie de données de réponse à la seconde partie des données de tests.

4. Procédé selon la revendication 3, caractérisé en ce que l'étape consistant à transférer les données d'adresses vers le bus de données comprend les étapes consistent à:
   a) sélectionner à partir d'une première partie d'une mémoire numérique (10c, 15) une séquence d'instructions définissant un mode de test de bus de données,
   b) sélectionner à partir d'une seconde région de la mémoire numérique une table de configurations d'essai,
   c) sélectionner à partir de ladite table de configurations d'essai, une configuration d'essai parti-culière,
   d) écrire la configuration d’essai particulière à l’intérieur d’un registre de stockage de données (16) au moyen d’une région du bus de données (12),
   e) lire en retour à partir dudit registre de stockage de données (16) une configuration de réponse au moyen de ladite région du bus de données (14),
   f) comparer la configuration de réponse à la configuration d’essai particulière, et
   g) répéter les étapes c à f autant de fois que cela est nécessaire, pour tester l'ensemble du bus de données (14).

5. Procédé selon l’une des revendications 3 ou 4, caractérisé en ce que l’étape consistant à transférer les données de test vers le bus d’adresses comprend les étapes consistant à:
   a) sélectionner à partir d’une première région de la mémoire numérique (10c, 15) une séquence d’instructions définissant un mode de test de bus d’adresses,
   b) sélectionner à partir d’une seconde région de la mémoire numérique (10c, 15), une table de configurations d’essai,
   c) sélectionner à partir de la table de configurations d’essai une configuration d’essai particulière,
   d) transférer la configuration d’essai particulière en tant qu’adresse sur le bus d’adresses (12),
   e) acquérir la configuration d’essai particulière en tant qu’adresse à l’intérieur d’un registre de stockage d'adresses (17),
   f) lire à partir du registre de stockage d’adresses (17) une configuration de réponse,
   g)Comparer la configuration de réponse à la configuration d’essai particulière,
   h) Répéter les étapes c à g autant de fois que cela est nécessaire pour tester l’ensemble du bus d’adresses (12).
FIG. IA.
(PRIOR ART)

FIG. IB.
FIG. 2.

FIG. 3.
LEVEL 2

SELECT A TEST PATTERN TABLE

SELECT A DATA PATTERN FROM THE TABLE

USE DATA PATTERN AS ADDRESS IN A DATA CYCLE

CAPTURE ADDRESS (FROM d) INTO ADDRESS LATCH

READ THE PATTERN IN THE ADDRESS LATCH

PATTERN ORIGINAL

YES

ERROR

NO

END OF DATA PATTERN TABLE

YES

NEXT TEST

NO

FIG. 4.