MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963 A
COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952

APPLICATION FOR A STANDARD PATENT

I/We, SONY CORPORATION

of

7-35, Kitashinagawa 6-chome,
Shinagawa-ku,
Tokyo
Japan.

hereby apply for the grant of a standard patent for an invention entitled "TIME COUNTING CLOCK GENERATOR".

which is described in the accompanying provisional/complete specification.

Details of basic application(s):

<table>
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<tr>
<th>Number of basic application</th>
<th>Name of Convention country in which basic application was filed</th>
<th>Date of basic application</th>
</tr>
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<tbody>
<tr>
<td>153406/79</td>
<td>Japan</td>
<td>November 27, 1979</td>
</tr>
</tbody>
</table>

My/our address for service is care of CLEMENT HACK & CO., Patent Attorneys, 140 William Street, Melbourne, Victoria, 3000, Australia.

DATED this 18th day of November, 1980

SONY CORPORATION

CLEMENT HACK & CO.

To: The Commissioner of Patents.

FF/App/1/80
DECLARATION IN SUPPORT OF A CONVENTION OR NON-CONVENTION APPLICATION FOR A PATENT OR PATENT OF ADDITION

In support of the application made by

Sony Corporation

for a patent for an invention entitled

TIME COUNTING CLOCK GENERATOR

I/We, Yasuo Kanai, of c/o No.7-95, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, Japan
do solemnly and sincerely declare as follows:-

1. I am/we are the applicant(s) for the patent, or am/are authorised by the abovementioned applicant to make this declaration on its behalf.

2. The basic application(s) as defined by Section 141 of the Act was/were made in the following country or countries on the following date(s) by the following applicant(s) namely:-

Country, filing date and name of Applicant(s) for the or each basic application

<table>
<thead>
<tr>
<th>Country</th>
<th>Date</th>
<th>Name(s) and address(es) of Applicant(s)</th>
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<tbody>
<tr>
<td>Japan</td>
<td>November 27, 1979</td>
<td>Sony Corporation</td>
</tr>
</tbody>
</table>

3. The said basic application(s) was/were the first application(s) made in a Convention country in respect of the invention the subject of the application.

4. The actual inventor(s) of the said invention is/are

Shosuke Tanaka, of 3016-1-2152, Nagatsuda-cho, Midori-ku, Yokohama-shi, Kanagawa-ken, Japan

Yumiyoshi Abe, of 4-13-1, Asahi-cho, Atsugi-shi, Kanagawa-ken, Japan

5. The facts upon which the applicant(s) is/are entitled to make this application are as follows:- the applicant is the assignee of the actual inventors.

DECLARED at Tokyo Japan this 10th day of November 1980

Yasuo Kanai

This form may be completed and filed after the filing of a patent application but the form must not be signed until after it has been completely filled in as indicated by the marginal notes. The
1. A time counting clock generator for a video tape recorder comprising:

   a pulse generator for generating a pulse signal in response to the movement of a video tape;
   
a direction indicating pulse generator for generating a direction indicating pulse output from said pulse signal;
   
a dividing counter for dividing said pulse signal for generating a timer counting clock, said direction indicating pulse output being supplied to an up-down control input of said dividing counter;
   
a control signal reproducing circuit for reproducing control signal recorded on said video tape; and,
   
a counter presetting means for presetting said
dividing counter to zero when said direction indicating pulse output indicates the forward movement of said video tape and to the maximum value when said direction indicating pulse output indicates the reverse movement of said video tape at each occurrence of said control signal.
Short Title: TIME COUNTING CLOCK GENERATOR

TO BE COMPLETED BY APPLICANT

Name of Applicant: SONY CORPORATION

Address of Applicant: 7-35, Kitashinagawa 6-chome,
Shinagawa-ku,
Tokyo,
Japan.

Actual Inventor: Shosuki TANAKA
Fumiyoshi ABE

Address for Service: CLEMENT HACK & CO.,
140 William Street,
Melbourne, Vic. 3000.
Australia.

Complete Specification for the invention entitled:

TIME COUNTING CLOCK GENERATOR

The following statement is a full description of this invention, including the best method of performing it known to me:

PF/CPLF/2/80
TIME COUNTING CLOCK GENERATOR

BACKGROUND OF THE INVENTION

(1) Field of the Invention:

This invention generally relates to a timer counting clock generator, and more particularly to such timer counting clock generator that is applied to a video tape recorder.

(2) Description of the Prior Art:

In the apparatus where a tape is driven such as a video tape recorder, it is usually necessary to provide a function of detecting and displaying the residual amount of the tape or prevailing position thereof. Particularly, it is necessary to accurately detect and display the prevailing tape position in case of automatically editing video tape programs with a video tape recorder.

Hitherto, it has been in practice to detect the position of the tape being driven by a tape driving device by detecting the relative position of the tape through the counting of count pulses obtained from a counter roller being rotated with the movement of the tape or by detecting the relative position of the tape through the counting of count pulses of a control signal recorded on the tape or by detecting the absolute address through reproduction of SMPTE (the Society of Motion Picture and Television - la-
Engineers) time code previously recorded on the tape.

However, by the afore-mentioned detection method using a counter roller, slip exists between the video tape and roller, so that it is difficult to obtain correct display of the tape position.

Also, by the method of counting the control signal, it is difficult to correctly detect the tape position due to the reduction of the output at the slow tape speed and signal drop out.

In particular, with the above-prior art systems mis-counting is liable to result in case when the direction of running of the tape is changed a number of times.

SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide a new tape timer circuit.

It is a secondary object of the present invention to provide a novel time counting clock generating circuit.

It is a further object of the present invention to provide newly designed tape time counting clock generating circuit applied to a video tape recorder.

According to the present invention, a tape counter roller generates counter clock pulses which have frequencies proportional to speeds of a video tape. The generated counter clock pulses are once fed to a counter circuit to which a control track pulse produced from a control track
of the video tape is fed in order to correct the generation of the tape time counting clock.

The correction of the counter operation is done such that if the video tape is running forward, the counter is preset to zero at the occurrence of the produced control track pulse, and if the video tape is running backward, the counter is preset to a maximum value at the occurrence of the reproduced control track pulse.

Thus, a revised or corrected tape time counting clock pulse is obtained at an output of the counter.

In the actual circuit arrangement, a programmable read only memory is applied to the circuit.

The above-mentioned and other objects and features of the invention will become apparent from the following detailed description taken in conjunction with the drawings which indicate embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the principal construction of an embodiment of the time counting clock generator according to the present invention;

Fig. 2 is a time chart illustrating the operation of the same embodiment;

Fig. 3 is a connection diagram showing a specific example of the circuit construction of the same embodiment;

Fig. 4 is a time chart illustrating the operation
of a first programmable read only memory used in the above embodiment; and

Fig. 5 is a time chart illustrating the operation of a second programmable read only memory.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 shows the principle construction according to the present invention. In the Figure, a video tape 1 rotates a counter roller 2. The counter roller 2 has a magnetic wheel 3, and a pair of magnetic pick-up heads 4 and 5 are provided to face the magnetic wheel. A control track head 6 reproduces control signal pulses (CTL pulses) from the video tape 1. Where NTSC (National Television System Committee) color television signal is recorded on the video tape, the CTL pulses constitute a pulse signal at 30 Hz in the normal reproducing mode in case of a helical scan video tape recorder. The magnetic pick-up heads 4 and 5 are located at such positions that their respective output pulse signals $\phi_a$ and $\phi_b$ are 90 degrees out of phase with respect to each other. The frequency of the counter clock signals $\phi_a$ and $\phi_b$ thus obtained corresponds to the tape running speed.

The counter clock signals $\phi_a$ and $\phi_b$ are shown respectively in (A) and (B) in Fig. 2, and a control signal CTL is shown in (C) in Fig. 2.

The counter clock signals $\phi_a$ and $\phi_b$ are fed to a
clock pulse generator 7 and a direction detector 8. The clock generator 7 detects the every edges of the individual counter clock signals and produces an intermediate clock signal $\phi_{CK}$ at a pulse repetition frequency equal to four times that of the counter clock signals. The direction detector 8 detects the tape running direction by comparing the phases of the counter clock signals $\phi_a$ and $\phi_b$ at all edges thereof, and provides a direction detection signal $S_D$ of logic "1" when the tape is running forward and a detection signal of logic "0" when the tape is running backward, as shown in Fig. 2. The control signal CTL from the control track head 6 is fed to an edge selector 9, which selectively produces differential pulse signals $D_{CTL}$ synchronized to the rising or falling edges of the input control signal as shown in (F) in Fig. 2, these differential pulses being coupled as load signal to a load input terminal of a 4-step reversible counter 10. The operation of the edge selector 9 is controlled by the direction detection signal $S_D$ from the direction detector 8.

The intermediate clock signal $\phi_{CK}$ from the clock generator 7 is coupled to a clock input terminal of the 4-step reversible counter 10, and the direction detection signal $S_D$ from the direction detector 8 is coupled to an operation control terminal of the counter. The direction detection signal $S_D$ is also coupled through an inverter 11
to a preset input terminal of the counter. Thus, the value of the direction detection signal $S_D$ coupled from the direction detector 8 through the inverter 11 is preset as initial data therein at every edge of the control signal $CTL$ coupled through the edge selector 9, and the counter 10 shows either up-count or down-count operations in accordance with the tape running direction. More particularly, when the tape is running forward, the 4-step reversible counter 10 counts up the clock signal $\phi_{CK}$ by the control of the direction detection signal $S_D$ of logic "1" provided from the direction detector 8. And further it is preset to zero in synchronism to the differential pulse signal $D_{CTL}$ in the presence of preset input signal of logic "00". On the other hand, when the tape is running backward, the 4-step reversible counter 10 counts down the clock signal $\phi_{CK}$ by the control of the direction detection signals $S_D$ of logic "0" provided from the direction detector 8. And therefore, it is preset to three in synchronism to the differential pulse signal $D_{CTL}$ in the presence of preset input signal of logic "11".

The 4-step reversible counter 10, in which data "0" or "3" is preset according to the direction of running of the tape, provides a counter output signal $S_{CN}$ as shown in (9) in Fig. 2. This counter output signal is fed to a two-phase clock generator 12. The two-phase clock signal generator 12 produces revised counter clock signal
\( \phi_A \) and \( \phi_B \) of different phases as shown respectively in (I) and (J) in Fig. 2.

As is shown, with this embodiment, in which data is preset in the 4-step reversible counter 10 according to the tape running direction, namely data "0" is set at every rising of the control signal CTI when the tape is running forward and data "3" is set at every falling of the control signal CTI when the tape is running backward, errors that result at the time of the reversal of the tape running direction are cancelled, and also generation of quasi-pulse signals are prevented. The revised counter clock signals \( \phi_A \) and \( \phi_B \) which represent the tape running position, are produced from respective output terminals 13 of the two-phase clock signal generator 12 in accordance with the counter output signal \( S_{CN} \) from the 4-step reversible counter 10. The revised counter clock signals \( \phi_A \) and \( \phi_B \) thus obtained, which contain tape position information based upon the control signal CTI, do not only correspond to the frame period of video signal but also correctly correspond to the tape running position even if the tape running speed is changed.

A specific example of the circuit construction of the above-embodiment of the present invention, which operates principally in the manner as described above, will be described with reference to Fig. 3.

In the example shown in Fig. 3, counter clock signal
φₐ from a signal input terminal 4a is coupled to a data input terminal of a first D-type flip-flop 16, and counter clock signal φₜ from a signal input terminal 4b is coupled to a data input terminal of a second D-type flip-flop 17. The counter clock signals φₐ and φₜ are supplied from the respective magnetic pick-up heads 14 and 15 (Fig. 1), and at the normal tape speed they have a pulse repetition frequency of 30Hz. The first D-type flip-flop 16 produces a signal DFₚ₁ at its affirmation output, which is coupled to a data input terminal of a third D-type flip-flop 18 and also to a first data input terminal A of a first programmable read only memory 20. The second D-type flip-flop 17 produces a signal DFₚ₂ as its affirmation output, which is coupled to a data input terminal of a fourth D-type flip-flop 19 and a third input terminal C of the first programmable read only memory 20. The third and fourth D-type flip-flops 18 and 19 produce respective signals DFₚ₃ and DFₚ₄ as their affirmative outputs, which are coupled to the second and fourth data input terminals B and D of the first programmable read only memory 20. Clock signal of 25KHz is supplied to clock input terminals of the first to fourth D-type flip-flops 16 to 19. These flip-flops are thus synchronized to the clock signal CLK with respect to the counter clock signals φₐ and φₜ.

The first programmable read only memory 20 receives the affirmation output signals DFₚ₃₁ and DFₚ₃₂ from
the first and second D-type flip-flops 16 and 17 and also the affirmation output signals DFQ₃ and DFQ₄ from the third and fourth D-type flip-flops 18 and 19 lagging by one clock period behind the respective affirmation output signals DFQ₁ and DFQ₂, and it effects decoding operation in a manner as shown by the time chart of Fig. 4 to produce an intermediate clock signal $\phi_{CK}$ at a frequency of fourth times that of the counter clock signals $\phi_a$ and $\phi_b$ and also direction detection signal $S_D$ corresponding to the phase difference between the counter clock signals $\phi_a$ and $\phi_b$. The memory 20 has decoding functions such that the direction detection signal $S_D$ is set when the decode decimal is 1, 7, 14, and 8 reset when the decode decimal is 15, 10, 0 and 5 and is held when the decode decimal is 15, 10, 0 and 5. The intermediate clock signal $\phi_{CK}$ and direction detection signal $S_D$ provided from the first programmable read only memory 20 are supplied to 4-step reversible counter 10. In the counter 10 of the Fig. 3, the inverter 11 of Fig. 1 is included therein. The first programmable read only memory 20 is held in a decoding operation mode according to the tape running direction, and to this end the direction detection signal $S_D$ is fed back to a fifth data input terminal E. The direction detection signal $S_D$ from the first programmable read only memory 20 is used as a control signal for a switching circuit 21 in edge selector 9. The edge selector 9 has an inverter 22, and a signal
representing the rising edges of the control signal CTL and a signal representing the falling edges thereof are selectively coupled through the switching circuit 21 to a load input terminal of the 4-step reversible counter 10.

As mentioned earlier, the 4-step reversible counter 10 effects 4-step up-counting with data "0" reset at every occurrence of the control signal CTL when the tape is running forward, while it effects 4-step down-counting with data "3" reset at every occurrence of the control signal when the tape is running backward. The counter output signal $S_{CN}$ from the 4-step reversible counter 10 is fed to a data input terminal of a fifth D-type flip-flop 25. The fifth flip-flop 25 produces a signal $D_{FQ5}$ as its affirmative output $D_{FQ6}$, which is coupled to a data input terminal of a sixth D-type flip-flop 26 and also to a fifth data input terminal $E$ of a second programmable read only memory 28. The sixth flip-flop 26 produces a signal $D_{FQ6}$ as its affirmation output, which is coupled to a sixth data input terminal $F$ of the second programmable read only memory 28. The fifth and sixth D-type flip-flops 25 and 26 are triggered by the 25-kHz clock signal $CLK$ to effect inverting action according to the logic state at the data input terminal. The affirmation output signal $D_{FQ6}$ produced from the sixth flip-flop 26 is lagging by one clock interval behind the affirmation output signal $D_{FQ5}$ produced from the fifth flip-flop 25.
The second programmable read only memory 28 receives at its first to fourth data input terminals A to D respective four-bit count output signals QA to QD from a 16-step up-counter 27, which counts the 25-kHz clock signal \( \text{CLK} \) from the signal input terminal 15 and also at its seventy data input terminal G the direction detection signal SD from the first programmable read only memory 20, and it effects decoding operation in a manner as shown by the time chart of Fig. 5. More particularly, the second programmable read only memory 28 produces a reset signal \( \text{SR} \) by selecting either the rising edges or falling edges or falling edges of the affirmation output signals DFQ5 and DFQ6 based on the logic value of the direction detection signal SD (i.e., tape running direction). The reset signal thus produced is fed back to a reset input terminal of the 16-step up-counter 27, and when 15 of 25-kHz clock signal pulses are counted by the 16-step counter 27 after the supply of the reset signal the memory 28 supplies a count stop signal \( \text{SN} \) to the 16-step up-counter 27 while also producing the revised counter clock signals \( \varphi_A \) and \( \varphi_B \) of the different phases based on the 4-bit count outputs QA to QD from the 16-step up-counter 27 and the direction detection signal SD.

As has been shown, unlike the usual method of presetting the 4-step reversible counter 10 to "0" at every reversal of the tape running direction, wherein an undesired pulse signal \( \text{SM} \) as shown by an imaginary waveform
line in (H) in the time chart of Fig. 2 is produced, there is no possibility of the generation of the aforementioned undesired pulse signal $S_M$, so that it is possible to prevent accumulation of errors and to obtain the revised counter clock signals $\phi_A$ and $\phi_B$, which accurately indicate the prevailing position of the running tape and also correspond to the frame period, from the two-phase clock generator 12.

As has been made apparent from the above-embodiment, according to the present invention two different phase counter clock signals at pulse repetition frequency corresponding to the tape running speed are processed to obtain a direction detection signal indicating the direction of running of the tape and a clock signal at a frequency of four times that of the two different phase counter clock signals, and the clock signal thus obtained is counted by a 4-step reversible counter, which is controlled for switching between up-counting and down-counting by the direction detection signal with data "0" preset when the tape is running forward and data "3" preset when the tape is running backward, for producing two revised counter clock signals of different phases according to the count output signal from the 4-step reversible counter, it is possible to provide a counting pulse generating circuit for a tape counter, which eliminates the possibility of generation of error at the reversal of
the tape running direction and is also capable of sufficiently following the changes of the tape running speed to produce revised counter pulse signals indicating the accurate tape position corresponding to the frame period of a video signal.

While in the above embodiment a 4-step reversible counter has been used, it is possible to use reversible counters on other systems, for instance a 8-step counter. In this case, data "7" is preset in the reversly running state of the tape. In general, the maximum value is to be preset in the reverse running mode of the tape at every occurance of the control pulse.
THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A time counting clock generator for a video tape recorder comprising:
   a pulse generator for generating a pulse signal in response to the movement of a video tape;
   a direction indicating pulse generator for generating a direction indicating pulse output from said pulse signal;
   a dividing counter for dividing said pulse signal for generating a timer counting clock, said direction indicating pulse output being supplied to an up-down control input of said dividing counter;
   a control signal reproducing circuit for reproducing control signal recorded on said video tape; and,
   a counter presetting means for presetting said dividing counter to zero when said direction indicating pulse output indicates the forward movement of said video tape and to the maximum value when said direction indicating pulse output indicates the reverse movement of said video tape at each occurrence of said control signal.

2. A time counting clock generator as claimed in claim 1, wherein said dividing counter is a 1/4 divider, said 1/4 divider being preset to three in decimal at the occurrence of said control signal when the direction
indicating pulse output indicates the reverse movement.

3. A time counting clock generator as claimed in claim 1, wherein said pulse generator generates a pair of pulses with the phases thereof being different by about 90° from each other.

4. A time counting clock generator as claimed in claim 1, wherein said direction indicating pulse output is supplied to a data input terminal of said dividing counter through an inverter.

5. A time counting clock generator as claimed in claim 3, said pair of pulses from said pulse generator is synthesized to produce a resultant clock signal having a frequency of four times that of the original pulse signal generated from said pulse generator, said resultant clock signal being supplied to a clock terminal of said dividing counter.

Dated this 18th day of November, 1980.

SONY CORPORATION
By its Patent Attorneys,

CLEMENT HACK & CO.


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FIG. 1
FIG. 1
FIG. 2

Diagram showing waveforms for different phases and control signals.

A. \( \phi_a \)
B. \( \phi_b \)
C. \( C_T \)
D. \( \phi_{ck} \)
E. \( S_0 \)
F. \( D_{ctrl} \)
G. \( S_{cm} \)
H. \( \phi_a \)
J. \( \phi_b \)
FIG. 4

FWD

REV

FWD

DFQ_2

DFQ_1

DFQ_4

DFQ_3

DECODE
DECIMAL

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FWD PULSE

REV PULSE

ϕ_{CK}

S_0