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PATENT REQUEST: STANDARD PATENT/PATENT OF ADDITION

We, being the persons(s) identified below as the Applicant, request the grant of a patent to the person identified below as the Nominated Person, for an invention described in the accompanying standard complete specification.
Full application details follow.

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(54) Invention Title "MULTIPLEXING METHOD FOR AN ATM SWITCHING NETWORK"

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ALCATEL N.V.

B. O'Connor (Authorized Signatory) 7 June 1996

Date
NOTICE OF ENTITLEMENT

We, ALCATEL N.V.
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being the applicant in respect of Application No. for an invention entitled "MULTIPLEXING METHOD FOR AN ATM SWITCHING NETWORK"
described in the accompanying specification, state the following:

1. The company nominated for the grant of the patent has entitlement from the actual inventor by mesne assignment.

2. The company nominated for the grant of the patent has entitlement from the applicant of the basic application listed on the patent request form by assignment.

3. The basic application listed on the request form is the first application made in a Convention country in respect of the invention.

ALCATEL N.V.

7 June 1996

B. O'Connor
A multiplexing method for asynchronous transfer mode telecommunications networks, and switching node implementing said method. The method consists in placing as the payload in a succession of cells (CL1, CL2, CL3, ...) conveying the same logical channel a succession of logical entities, referred to as “information containers” (CT1, CT2, CT3, ...) and conveying that same logical channel, each container including a payload (LD1, LD2, LD3, ...) which is a quantity of information that is greater than that of the payload (PL1, PL2, PL3, ...) of each cell.

In a preferred embodiment, the payload of each container is composite. It comprises samples of conventional synchronous digital channels and data micropackets each of which is provided with a label indicating a logical channel and the length of the packet.

Field of use: ATM telecommunications networks.

Figure to be published: Figure 1.
Invention Title:

"MULTIPLEXING METHOD FOR AN ATM SWITCHING NETWORK"

The following statement is a full description of this invention, including the best method of performing it known to us:-
This invention relates to a multiplexing method for asynchronous transfer mode telecommunications networks, and to a switching node implementing the method. Future broadband integrated services digital networks will be based on an asynchronous transfer mode, referred to as "ATM". This asynchronous transfer mode has been standardised by the CCITT: information is transported in packets called cells, comprising a header and a payload, of fixed length. The logical channel conveyed by a cell, between two nodes of the network, is identified by a virtual path identifier and a virtual circuit identifier, both contained in the header of each cell.

Consequently, a source can transmit cells at its own rate, without direct reference to the network to which it is connected. These cells can convey all types of services, while only requiring a network using a single switching type: ATM cell-switching.

Standardised cells are however not perfectly suited to all services. Narrow-band telephone services are currently conveyed by "synchronous" networks setting-up synchronous digital circuits. The samples of 30 telephone signals are transmitted together in the form of recurrent frames, each frame being divided into time intervals of which are respectively assigned to the 30 telephone circuits. At least over the development phase of asynchronous transfer mode networks, synchronous networks will remain in existence and even be used as distribution networks for synchronous mode telephone circuits which will be conveyed by cells for most of the routing. There is thus a need to organize the coexistence of these network types.

French patent application no. 93 00955 discloses a cell-forming device and a cell-disassembling device for synchronous digital channels, which devices allow a very large number of synchronous circuits to be switched in an ATM type switching network. The cell-forming device places in the same cell, which conveys a logical channel, samples respectively representing the signals of a plurality of different synchronous circuits that may be conveyed by the logical channel. The cell-forming device thus does not waste time waiting for several successive samples of the same circuit before it efficiently fills the cells. It also conforms to CCITT Recommendation Q.551 which limits the return transit delay in a synchronous network to one millisecond. These cells are referred to as "composite cells".

French patent application no. 94 11307 discloses a device for switching
samples contained in composite cells; and an access node, for accessing an asynchronous transfer mode switching network, including such devices for switching samples contained in composite cells.

A switching network is conventionally constituted by several switching matrix stages, the structure of which is optimized so as to achieve a given blocking probability, for a given traffic and a given number of inputs, and for a cell length that is fixed by the CCITT standard. Conventional calculations make it possible to select a structure from among several that are more or less optimal. An even more optimal structure could be obtained if the cell length was variable. This is however impossible since the cell length is standardised. An object of the invention is to provide a multiplexing method capable of further optimizing the use of a switching network switching standardised ATM cells.

ATM cells are in particular capable of handling a data transmission service, provided that the data to be transmitted is grouped together in packets the length of which corresponds to the length of the payload of a cell. In the case where the data source has a low data rate and thus transmits data micropackets, it is often impossible to wait for several successive micropackets coming from the same source to efficiently fill each cell. A further object of the invention is to provide a multiplexing method capable of transmitting data micropackets in standardised ATM cells, while efficiently filling the cells.

According to a first aspect of the invention, there is provided a method of performing multiplexing in an asynchronous transfer mode telecommunications network, for time-division multiplexing information in fixed-length asynchronous transfer mode cells, each cell including:

- a header containing in particular a virtual path identifier and a virtual circuit identifier that define a logical channel between two nodes of said network; and
- a payload constituted by a fixed quantity of information;

said method comprising, prior to the routing of information in the node, in placing as the payload in a succession of cells conveying the same logical channel, a succession of logical entities referred to as information containers and conveying that same logical channel, each container including a payload which is a quantity of
information that is greater than that of the payload of each cell, the quantity of information transported by each container being chosen so that the node is more efficiently used;

and wherein, in order to transmit, firstly, samples of a plurality of signals belonging to various circuits and, secondly, data having various destinations, it comprises placing, in a succession of containers conveying a given logical channel, and each having a fixed length:

- samples respectively corresponding to the circuits, each sample being locatable inside a container by its position in the container; and

- a plurality of data packets, each packet comprising a label indicating the destination and length of the packet.

The method of the present invention makes it possible to further optimize the use of each ATM switching node, by using, for each node, a container length that is optimal for the node. The length is chosen once and for all, according to statistical traffic characteristics, or can vary according to current traffic characteristics. Furthermore, it makes it possible to optimize the use of cells by enabling data micropackets (having a length that is smaller than the payload of a cell) and circuit samples to be concurrently transported in the same cell, on account of the fact that each circuit sample can be located by its position, its length being fixed and known, and that each data micropacket can be located by a label which further indicates its length.

According to a second aspect of the invention, there is provided a switching node implementing said method, and comprising:

- a first stage comprising at least one auxiliary switching matrix for grouping together in the same logical entity, referred to as a "container", information received by the node and contained in various cells, which information can be routed via the same path for at least a portion of its routing through said node; each container being transported by a plurality of cells conveying the same logical channel and transporting a quantity of information that is greater than that of the payload of each cell, the quantity of information transported by each container being chosen so that the node is more efficiently used;
- at least one conventional intermediate cell-switching stage, having inputs coupled to outputs of the first stage; and
- a last stage comprising at least one auxiliary switching matrix for placing in distinct cells respectively conveying distinct logical channels, information which has been transported in the same cell because it was grouped together in the same container; wherein

said switching node comprises at least one auxiliary switching matrix including:
- a first marking memory, dedicated to routing synchronous circuit samples;
- a first space-division switch, controlled according to routing data stored in the first marking memory so as to place synchronous circuit samples in a cell;
- a second marking memory, dedicated to routing data packets; and
- a second space-division switch, controlled according to routing data stored in the second marking memory so as to place data packets in a cell.

According to a still further aspect of the invention, there is provided a switching node implementing said method, and comprising:

- a main cell-switching network having main inputs constituting the inputs of said node, and main outputs constituting the outputs of said node; and
- at least one auxiliary cell-switching network having inputs respectively connected to auxiliary outputs of the main network and outputs respectively connected to auxiliary inputs of the main network, for:
  -- grouping together in the same logical entity, referred to as a "container" and having a capacity that is greater than the payload of a cell, information contained in various cells, which information can be routed via the same path for at least a portion of its routing through said node, and each container being transported by a plurality of cells conveying the same logical channel; and
  -- placing in distinct cells respectively conveying distinct logical channels, information which has been transported in the same cell because it was grouped together in the same container;

said switching node being characterised in that it comprises at least one auxiliary switching matrix including:
- a first marking memory, dedicated to routing synchronous circuit samples;
a first space-division switch, controlled according to routing data stored in the
first marking memory so as to place synchronous circuit samples in a cell;
a second marking memory, dedicated to routing data packets; and
a second space-division switch, controlled according to routing data stored in
the second marking memory so as to place data packets in a cell.

The invention may be better understood from the following detailed description
when read with reference to the accompanying drawings in which:

- Figure 1 schematically represents a succession of information containers,
each having a length that is not equal to an integer multiple of the length of a cell;
- Figures 2 and 3 illustrate a particular example of containers each having a
  length that is equal to twice the length of a standardised cell;
- Figure 4 shows the synoptic diagram of a first embodiment of the switching
  node according to the invention;
- Figure 5 shows the synoptic diagram of a second embodiment of the
  switching node according to the invention; and
- Figure 6 represents a switching matrix which can be used in these two
  embodiments.

Figure 1 illustrates the multiplexing method according to the invention, by
means of an example in which each container has a fixed length which is greater than
the length of a cell but smaller than twice the length of a cell. In this example, a
succession of three containers CT1, CT2, CT3 is conveyed by a succession of cells
CL1, CL2, CL3, etc. Each of the cells has a header, respectively HD1, HD2, HD3,
containing a virtual path identifier and a virtual circuit identifier. The virtual path
identifiers of the cells CL1, etc. all identify the same channel. The virtual circuit
identifiers may differ from one cell to another. Each of the cells further comprises a
payload, respectively PL1, PL2, PL3, ...

The container CT1 straddles cells CL1 and CL2. It comprises a payload LD1,
which is divided into two portions, and starts with a flag F1 constituted by a fixed
pattern. The flag F1 and a first portion of the payload LD1 occupy the entire field
provided for the payload PL1 of the cell CL1. A second portion of the payload LD1
occupies a portion of the field provided for the payload PL2 of the cell CL2. In this
example, the flag F1 immediately follows the header HD1 of the cell CL1, but this is not generally true, since the container length is not an integer multiple of the cell length.

The container CT2 comprises a flag F2 constituted by the same pattern as the flag F1, and following the second portion of the payload LD1, in the cell CL2. The flag F2 is followed by a first portion of the payload LD2, which is divided into two portions. A second portion of the payload LD2 is placed after the header HD3 in the cell CL3. The container CT3 is placed after the second portion of the payload LD2 in the cell CL3. It starts with a flag F3 which is identical to the flags F1 and F3.

In this example, the length of each container CT1, CT2, CT3, ..., is fixed. It is the same for all the inputs of a given switching node. It is determined according to the traffic that the node will statistically receive. If the containers only convey circuits, the optimal length of the containers, for a statistically known traffic and a given blocking probability, can be determined using conventional calculation methods. If the containers must convey data micropackets, or a combination of data micropackets and telephone circuits, the length of the containers can be optimized by simulation.

According to a variant of implementation, the length of the containers can vary in time for the same input of a switching node. Primitives of a container length modification protocol are transmitted in the payload of a container prior to changing the container length.

According to another variant of implementation, the containers do not comprise flags, but an error detection code word, similar to that used in the header of standardised ATM cells. The code word is calculated using a standardised algorithm, applied to the header bits. It enables the detection of header transmission errors. The code word further enables the detection of the beginning of each cell. A known method of detecting the beginning and the end of each cell in a continuous succession of standardised cells consists in:

- calculating, on the fly, a code word, according to the standardised algorithm;
- retrieving in the succession of received bits a word constituted by the same number of bits as the code word;
- comparing the calculated code word to the received bits, and concluding that
the header of a cell is detected when the calculated code word is identical to a word retrieved on the fly.

Figures 2 and 3 represent in more detail two containers CT4 and CT5 respectively, in an example where each container has a length that is exactly equal to twice the length of a cell, and transports both telephone circuit samples and data micropackets. In this example, data is stored in micropackets each having a length that is smaller than that of the payload that may be transported in a cell, which further enables circuit samples to be transported in the same cell.

In Figure 2, the container CT4 is conveyed by a cell CL4 and a cell CL5 having respective headers HD4 and HD5. The headers comprise the same virtual path identifier VP, but two different virtual circuit identifiers, VC1 and VC2 respectively. In these figures, the fields referenced U are empty fields. In this example, the cell CL4 transports: a sample of a telephone circuit CH1; a sample of a telephone circuit CH2 which is divided into two portions so as to use two available but non-adjacent fields; a sample of a telephone circuit CH3; a data micropacket PK1; a data micropacket PK2; and two control bytes CTR4 enabling the detection of errors in the payload of the cell CL4.

In this example, a flag is not needed to identify the beginning of each container as it can simply be identified by the header of alternate cells.

The cell CL5 comprises: a sample of a telephone circuit CH4; a sample of a telephone circuit CH5; a data micropacket PK3; a data micropacket PK4; and two control bytes CTR5 enabling the detection of errors in information transmitted in the payload of the cell CL5. Each micropacket includes a label, respectively L1, L2, L3, L4 constituted by a logical reference enabling the independent routing of each micropacket, and by length data enabling the precise definition of the end of the micropacket.

Figure 3 represents the container CT5 which follows the container CT4. It is conveyed by two successive cells CL6 and CL7 having respective headers HD6 and HD7. The headers comprise the same virtual path identifier VP, but two different virtual circuit identifiers, VC1 and VC2 respectively.

Figure 3 shows that the containers CT4 and CT5, respectively for each virtual
circuit, have a structure that is identical as far as the telephone circuits are concerned and so long as the circuits are set-up, and a structure that is variable as far as the data micropackets are concerned.

The cell CL6 transports samples of the telephone circuits CH1, CH2, CH3 in positions that are identical to those occupied by the samples of these circuits in the cell CL4. Similarly, the cell CL7 transports samples of the telephone circuits CH4 and CH5 in positions that are identical to those occupied by the samples of these circuits in the cell CL5. However, the cell CL6 transports a data micropacket PK5, having a label L5, but not necessarily having the same length nor the same position as the micropackets PK1 and PK2 in the cell CL4.

It further transports a control word CTR6 which depends upon the entire payload transported by the cell CL6.

Similarly, the cell CL7 transports a micropacket PK6 which does not have the same length nor the same position as the micropackets PK3 and PK4 which were transported by the cell CL5. The cell CL7 further transports a control word CTR7 which is calculated on the entire payload transported by the cell CL7.

In other examples of implementation, the position of the samples of a given circuit may vary in time so as to optimize cell filling. Primitives of a sample position modification protocol are then transported in containers.

In this example, the data packets to be transmitted are micropackets the length of which is much smaller than that of a cell, but they could just as well be data packets having a length that is greater than the payload of a cell, for instance 1.5 times the length of a cell, by distributing such a packet partly over a first cell and partly over a second cell constituting the same container.

According to a preferred embodiment, all the circuit samples are grouped together in a first portion of the container, and all the micropackets are grouped together in the second portion. The position of the border between the two portions of the container is then one of the elements of the container structure information transmitted by the signal circuits. This information also includes the position in the container of the samples of each circuit, which position may be fixed for the whole duration of the circuit or may be variable.
Figure 4 represents a first embodiment of the switching node according to the invention. This embodiment comprises:

- n input links IL1, ..., ILn respectively connected to n optical network units ONU1, ..., ONU'n, and n output links OL1, ..., OLn respectively connected to n optical network units ONU'1, ..., ONU'n, each of the optical network units being connected to one or more user terminal(s), represented by dots in the Figure;

- p input matrices IM1, ..., IMp, each having three inputs and three outputs, in this very simplified example;

- p output matrices OM1, ..., OMP, each having three inputs and three outputs, in this very simplified example; and

- a conventional ATM switching network, referenced SN, constituted by a plurality of stages not represented in the Figure, comprising n inputs and n outputs.

Each of the optical network units ONU1, ..., ONU'n has an output that is connected to an input of one of the input matrices IM1, ..., IMp. Each of the optical network units ONU'1, ..., ONU'n has an input that is connected to an output of one of the output matrices OM1, ..., OMP. Each output of each input matrix IM1, ..., IMp is connected to an input of the switching network SN. Each output of the network SN is connected to an input of one of the output matrices OM1, ..., OMP.

The implementation of the input matrices, IM1, ..., IMp and of the output matrices OM1, ..., OMP will be described hereafter with reference to Figure 6.

Figure 4 illustrates the operation of the first embodiment using an example in which:

- a user terminal T1, connected to the optical network unit ONU1, transmits a cell CL10 containing information (telephone circuit samples or data micropackets) addressed to a user terminal A;

- a user terminal T2, connected to the optical network unit ONU1, transmits a cell CL11 containing information addressed to a user terminal B; and

- a user terminal T3, connected to the optical network unit ONU3, transmits a cell CL12 containing information addressed to a user terminal C.

The user terminals A and C are both connected to the optical network unit ONU'1, while the user terminal B is connected to an optical network unit ONU'2. As
the user terminals A, B, C are connected to the same output matrix OM1, it is possible to group together in the same container information that is addressed to the three user terminals, and it is possible to handle the container as a single entity up to the output matrix OM1. The function of the matrix OM1 is to differentiate and appropriately reroute information addressed to the user terminals A and C on the one hand and to the user terminal B on the other, that is, respectively towards the output links OL1 and OL2. The function of the switching network SN is to route the containers, each constituted by two cells in this example, by individually routing each of the two cells along the same path, without knowing that the two cells constitute a container.

In this example, the optical network unit ONU1 forms a composite cell CL13 containing both information addressed to A and information addressed to B. The optical network unit ONU3 retransmits the cell CL12 without modifying its payload. The input matrix IM1 forms a container CT6, constituted by two successive cells CL14 and CL15, by placing therein all the information that is to transit through the output matrix OM1 before reaching its respective destination. Information addressed to A, B and C is thus placed in the container CT6. The network SN routes the two cells CL14 and CL15 up to any output of the network SN that is connected to an input of the matrix OM1.

The matrix OM1 breaks down the container CT6 and places the information it contains in the two cells CL16 and CL17 respectively addressed to the optical network units ONU'1 and ONU'2. The cell CL16 is a composite cell containing information addressed to A, and information addressed to C. The cell CL17 is a cell which only contains information addressed to B. The optical network unit ONU'2 retransmits the cell CL17 to the user terminal B without modifying its payload. The unit ONU'1 breaks down the composite cell CL16 into two cells CL18 and CL19 which only contain, respectively, information addressed to A and information addressed to C.

Figure 5 shows the synoptic diagram of a second embodiment of the switching node according to the invention. This second embodiment comprises:

- n input links IL1, ..., ILn respectively connected to n optical network units ONU1, ..., ONU n, and n output links OL1, ..., OLn respectively connected to n
optical network units ONU'1, ..., ONU'n;
- a conventional ATM switching network, referenced SN', having n main inputs, n main outputs, n auxiliary inputs and n auxiliary outputs; and
- another ATM switching network, referred to as an "auxiliary network", and referenced ASN, comprising n inputs respectively connected to the n auxiliary outputs of the network SN' and n outputs respectively connected to the n auxiliary inputs of the network SN'.

In this example, the auxiliary network ASN comprises:
- a conventional ATM switching matrix, referenced MO, comprising n inputs and n outputs;
- q input matrices IM'1, ..., IM'q, each having two inputs and two outputs, in this simplified example; and
- q output matrices OM'1, ..., OM'q, each having two inputs and two outputs, in this simplified example.

The inputs of the matrices IM'1, ..., IM'q constitute the n inputs of the network ASN. Their outputs are respectively connected to the n inputs of the matrix MO. The n outputs of the matrix MO are respectively connected to the inputs of the output matrices OM'1, ..., OM'q. The outputs of the output matrices respectively constitute the n outputs of the network ASN. The implementation of the input matrices IM'1, ..., IM'q and of the output matrices OM'1, ..., OM'q will be described hereafter with reference to Figure 6.

Figure 5 illustrates the operation of the second embodiment, again in the case where:
- a user terminal T1, connected to the optical network unit ONU1, transmits a cell CL21 containing information addressed to a user terminal A;
- a user terminal T2, connected to the optical network unit ONU1, transmits a cell CL22 containing information addressed to a user terminal B; and
- a user terminal T3, connected to the optical network unit ONU3, transmits a cell CL23 containing information addressed to a user terminal C.

The user terminals A and C are both connected to the same optical network unit ONU'1, while the user terminal B is connected to the optical network unit ONU'2.
It is possible, for most of the routing, to group together in the same container information that is addressed to A, B and C since the network SN' can, at the last moment, break down the container and forward the information to its respective destinations.

The optical network unit ONU1 forms a composite cell CL24 by grouping together the information addressed to the user terminals A and B. The optical network unit ONU3 retransmits the cell CL23 without modifying its payload. The network SN' is first used to route the cells CL24 and CL23 towards the two inputs of the auxiliary network ASN, the two inputs corresponding to the same input matrix IM'1, so that the matrix may form a container CT7 containing both the information due to transit through the optical network unit ONU1 and the information due to transit through the optical network unit ONU'2. The container CT7 is constituted by two consecutive cells CL25 and CL26. The cell CL25 transports information addressed to A and information addressed to B. The cell CL26 transports information addressed to C. The container CT7 is routed by the matrix M0 and an output matrix, OM'q for instance, up to an auxiliary input of the network SN'. The network SN' is used a second time to identically route the two cells CL25 and CL26 constituting the container CT7, up to an auxiliary output of the network SN', which output is connected to an input of the corresponding auxiliary network ASN, for instance, to the input matrix IM'q.

The matrix IM'q and the matrix M0 route the container towards an output matrix OM'1 the function of which is to break down the container CT7 into two cells CL28 and CL19 due to transit respectively through the optical network units ONU'1 and ONU'2 respectively. The cell CL28 is a composite cell which contains information addressed to A and information addressed to C. The cell CL29 contains information addressed to B. The network SN' is then used a third time, to route the two cells respectively towards the two links OL1 and OL2 that can forward them respectively towards the optical network unit ONU'1 and the optical network unit ONU'2. The unit ONU'1 breaks down the composite cell CL28 into two cells CL30 and CL31 which only contain respectively information addressed to A and information addressed to C. The unit ONU'2 retransmits the cell CL29 to the user terminal B without modifying its payload.
It is to be noted that, in this embodiment, information addressed to A, B and C transmits three times through the network SN' while in the embodiment represented in Figure 4 it only transits once. The second embodiment thus uses more switching resources. It has the advantage however of being more reliable since the structure of the network ASN is, somehow, parallel to the structure of the network SN', and thus makes it possible to remedy certain failures that may occur in the network ASN, while in the first embodiment it is not possible to remedy a failure occurring in one of the input matrices IM1, ..., IMp, or in one of the output matrices OM1, ..., OMp.

Figure 6 represents the synoptic diagram of a matrix AM that could constitute one of the matrices IM1, ..., IMp, OM1, ..., OMp, IM'1, ..., IM'q, OM'1, ..., OM'q used in the implementation examples represented in Figures 4 and 5.

This matrix AM comprises:
- N inputs I1, ..., IN;
- N input circuits IC1, ..., ICN; each having an input respectively connected to one of the inputs I1, ..., IN;
- a first marking memory M1, dedicated to routing synchronous telephone circuit samples;
- a first space-division switch S1, dedicated to the synchronous telephone circuit samples;
- a second marking memory M2, dedicated to routing data micropackets;
- a second space-division switch S2, dedicated to the data micropackets;
- N output circuits OC1, ..., OCN;
- N outputs O1, ..., ON each respectively connected to an output of one of the output circuits OC1, ..., OCN; and
- a control unit CU controlling each of the sub-assemblies of the matrix AM.

Each input circuit IC1, ..., ICN comprises a register provided for storing a cell received by an input terminal, respectively I1, ..., IN. The cell is received in serial form and is stored under the control of a clock signal, not represented in the Figure, supplied by the control unit CU.

The marking memory M1 comprises a write address input, coupled to an output of the control unit CU, and a read address input, coupled to an output of each
of the input circuits IC1, ..., ICN, so as to receive a cell header HD. A data input of the memory M1 is connected to an output of the control unit CU. The contents of the marking memory M1 are supplied by the control unit CU and are written under its control when the calls are set-up.

Each logical channel ending at one of the inputs IN is identified by a virtual path identifier and a virtual circuit identifier, which are contained in the header HD of each cell conveying the logical channel. For each incoming logical channel, the marking memory M1 contains on the same line:

- synchronous telephone circuit identifiers carried by the incoming logical channel, which identifiers indicate the positions of the samples in an incoming cell;
- the identifier of an outgoing logical channel, the identifier of an output O1, ..., ON, and identifiers indicating the positions assigned to the telephone circuit samples in each outgoing cell conveying the logical channel; and
- the indication of the position X beyond which the contents of an incoming cell transport data micropackets, each cell comprising a first portion containing only synchronous telephone circuit samples, and a second portion containing only data micropackets, said position varying from one cell to another.

This information is supplied to the control unit CU via signalling links not represented in the Figure.

A first data output of the memory M1 is connected to a common input of the input circuits IC1, ..., ICN so as to supply thereto the indication X of the position beyond which the payload of a cell transports data micropackets. A second data output of the memory M1 is connected to a control input of the space-division switch S1 so as to supply thereto routing information R1 constituted by the identity of one of the outputs O1, ..., ON of the matrix AM, and by identifiers indicating the positions of the synchronous telephone circuit samples in each cell of the outgoing logical channel. A third data output of the memory M1 is connected to an input of the space-division switch S1 so as to supply thereto a header HD' essentially constituted by identifiers of the outgoing logical channel.

The switch S1 comprises N registers RG1, ..., RGN for storing respectively the portion of the cell that is dedicated to the synchronous telephone circuit samples,
respectively for the N outputs O1, ..., ON; and for storing the header HD' of each cell that will transport the samples. The function of the switch S1 is to switch in space the synchronous telephone circuit samples contained in the first portion of each of the incoming cells towards one of the output circuits OC1, ..., OCN.

Each incoming cell is stored in one of the input circuits IC1, ..., ICN, for as long as it takes to switch the various elements of information contained therein. The contents of the header HD of each received cell are supplied by the input circuit to the read address input of the marking memory M1. Reading the marking memory M1 at this address supplies routing information R1 to the control input of the space-division switch S1, so that it stores, in each of the registers RG1, ..., RGN, samples respectively addressed to the output circuits OC1, ..., OCN. They are stored in the registers at positions corresponding to those they will occupy in an outgoing cell. Reading the memory M1 also supplies the header HD' of an outgoing cell. The header is also stored in one of the registers RG1, ..., RGN. The contents of each register RG1, ..., RGN are then transferred towards one of the output circuits OC1, ..., OCN which inserts them in an outgoing cell.

The marking memory M1 also supplies to the input circuit IC1, ..., ICN the indication X of the position beyond which the contents of the incoming cell transport data micropackets. Each input circuit IC1, ..., ICN therefore knows the position X from which it can start reading data micropackets.

The marking memory M2 is dedicated to routing micropackets. It comprises: a data input connected to an output of the control unit CU, a write address input connected to an output of the control unit CU, a read address input connected to a common output of the input circuits IC1, ..., ICN, and two data outputs respectively connected to two inputs of the space-division switch S2. The marking memory M2 contains routing information R2, constituted by an identity localising one of the outputs O1, ..., ON of the matrix AM, and a new label L' for each data micropacket.

An output of the input circuits IC1, ..., ICN is connected to an input of the space-division switch S2 so as to supply thereto the data D contained in each data micropacket. Another output of the input circuits IC1, ..., ICN is connected to a read address input of the marking memory M2 so as to supply thereto the label L of each
data micropacket. When a data micropacket is read in an input circuit, the marking memory M2 is read at the address L. An output of the marking memory M2 supplies to an input of the space-division switch S2 a new label L' for the data packet. The space-division switch S2 stores each data micropacket, constituted by a new label L' and data D, in a queue Q1, ..., QN respectively corresponding to one of the output circuits OC1, ..., OCN. The queues Q1, ..., QN are provided to solve the contention problems due to the asynchronous arrival of data micropackets addressed to the same output O1, ..., ON. The queues are conventionally managed.

The output of each queue Q1, ..., QN of the space-division switch S2 is respectively connected to an input of an output circuit OC1, ..., OCN so as to supply thereto data micropackets each constituted by a new label L' and data D. The output circuits OC1, ..., OCN are periodically read under the control of the control unit CU, using a link not represented in the Figure. The cell thus read in each output circuit is supplied in serial form to the output O1, ..., ON corresponding to the output circuit.
The claims defining the invention are as follows:

1. A method of performing multiplexing in an asynchronous transfer mode telecommunications network, for time-division multiplexing information in fixed-length asynchronous transfer mode cells, each cell including:

   - a header containing in particular a virtual path identifier and a virtual circuit identifier that define a logical channel between two nodes of said network; and
   - a payload constituted by a fixed quantity of information;

   said method consisting, prior to the routing of information in the node, in placing as the payload in a succession of cells conveying the same logical channel, a succession of logical entities referred to as "information containers" and conveying that same logical channel, each container including a payload which is a quantity of information that is greater than that of the payload of each cell, the quantity of information transported by each container being chosen so that the node is more efficiently used; wherein

   in order to transmit, firstly, samples of a plurality of signals belonging to various circuits and, secondly, data having various destinations, it comprises in placing, in a succession of containers conveying a given logical channel and each having a fixed length:

   - samples respectively corresponding to the circuits, each sample being locatable inside a container by its position in the container; and
   - a plurality of data packets, each packet comprising a label indicating the destination and length of the packet.

2. A method as claimed in claim 1, wherein the position of each of the samples of a given circuit is fixed for the whole duration of the circuit.

3. A method as claimed in claim 1, wherein the position of each of the samples of a given circuit is variable for the duration of the circuit; and wherein primitives of a sample position modification protocol are transported in containers.

4. A method as claimed in claim 1, wherein the beginning of each container is indicated by a predetermined flag.

5. A method as claimed in claim 1, wherein the length of each of the containers transmitted over a given link may vary; and wherein primitives of a container length
modification protocol are transmitted in the payload of a container, before the length is changed.

6. A switching node implementing the method as claimed in any one of claims 1 to 5, comprising:

- a first stage comprising at least one auxiliary switching matrix for grouping together in the same logical entity, referred to as a "container", information received by the node and contained in various cells, which information can be routed via the same path for at least a portion of its routing through said node; and each container being transported by a plurality of cells conveying the same logical channel and transporting a quantity of information that is greater than that of the payload of each cell, the quantity of information transported by each container being chosen so that the node is more efficiently used;

- at least one conventional intermediate cell-switching stage, having inputs coupled to outputs of the first stage; and

- a last stage comprising at least one "auxiliary" switching matrix for placing in distinct cells, respectively conveying distinct logical channels, information which has been transported in the same cell because it was grouped together in the same container; wherein

said switching node comprises at least one auxiliary switching matrix including:

- a first marking memory, dedicated to routing synchronous circuit samples;

- a first space-division switch, controlled according to routing data stored in the first marking memory so as to place synchronous circuit samples in a cell;

- a second marking memory, dedicated to routing data packets; and

- a second space-division switch, controlled according to routing data stored in the second marking memory so as to place data packets in a cell.

7. A switching node implementing the method as claimed in any one of claims 1 to 5, comprising:

- a main cell-switching network having main inputs constituting the inputs of said node, and main outputs constituting the outputs of said node; and

- at least one auxiliary cell-switching network having inputs respectively connected to auxiliary outputs of the main network and outputs respectively connected
to auxiliary inputs of the main network, for:

-- grouping together in the same logical entity, referred to as a "container" and having a capacity that is greater than the payload of a cell, information contained in various cells, which information can be routed via the same path for at least a portion of its routing through said node, and each container being transported by a plurality of cells conveying the same logical channel; and

-- placing in distinct cells respectively conveying distinct logical channels, information which has been transported in the same cell because it was grouped together in the same container; wherein

said switching comprises at least one auxiliary switching matrix including:

- a first marking memory, dedicated to routing synchronous circuit samples;
- a first space-division switch, controlled according to routing data stored in the first marking memory so as to place synchronous circuit samples in a cell;
- a second marking memory, dedicated to routing data packets; and
- a second space-division switch, controlled according to routing data stored in the second marking memory so as to place data packets in a cell.

8. A switching node as claimed in claim 6 or 7, wherein it further comprises:

- for optimising the resources within a container to be transmitted, means for assigning to each circuit sample a position in the container, for accordingly modifying the contents of the first marking memory, and for placing in the container primitives of a circuit sample position modification protocol, for all established circuits; and
- means for interpreting, upon reception of a container, primitives transported by the container and indicating position modifications, for determining the positions of samples transported in the container, and for accordingly updating the first marking memory.

9. A multiplexing method and a switching node substantially as hereinbefore described with reference to Figures 1-5 of the accompanying drawings.

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ABSTRACT

A multiplexing method for asynchronous transfer mode telecommunications networks, and switching node implementing said method. The method consists in placing as the payload in a succession of cells (CL1, CL2, CL3, ...) conveying the same logical channel a succession of logical entities, referred to as "information containers" (CT1, CT2, CT3, ...) and conveying that same logical channel, each container including a payload (LD1, LD2, LD3, ...) which is a quantity of information that is greater than that of the payload (PL1, PL2, PL3, ...) of each cell.

In a preferred embodiment, the payload of each container is composite. It comprises samples of conventional synchronous digital channels and data micropackets each of which is provided with a label indicating a logical channel and the length of the packet.

Field of use: ATM telecommunications networks.

Figure to be published: Figure 1.