CONVENTION APPLICATION FOR A PATENT

We, N.V. PHILIPS' GLOEILAMPENFABRIEKEN, a limited liability company, organized under the laws of the Kingdom of the Netherlands and carrying on business at 29 Emmasingel, Eindhoven, The Netherlands, hereby apply for the grant of a Patent for an invention entitled:

"SIGNAL-BOUYER CIRCUIT ARRANGEMENT"

Which is described in the accompanying complete specification. This application is made under the provisions of Part XVI of the Patents Act 1952-1969 and is based on the following application or applications for a patent or patents or similar protection made in the following country or countries on the following date or dates:

in Great Britain, appl. No. 40033-77, filed 26th September 1977
(Preliminary Spec.)
in ........................................, appl. No. ........................................, filed 25th May 1978
(Case Spec.)
in ........................................, appl. No. ........................................, filed ........................................

Our address for service is
Patent and Trade Mark Division,
Philips Industries Holdings Ltd,
The Philips Building, Blue Street,
North Sydney, New South Wales 2060, Australia.

Dated this 4th September 1978

N.V. PHILIPS' GLOEILAMPENFABRIEKEN

To: THE COMMISSIONER OF PATENTS.
COMMONWEALTH OF AUSTRALIA
Patents Act

DECLARATION FOR A PATENT APPLICATION

INSTRUCTIONS
(a) Insert "Convention" if applicable
(b) Insert FULL name(s) of applicant(s)
(c) Insert "of addition" if applicable
(d) Insert TITLE of invention
(e) Insert FULL name(s) AND address(es) of declarant(s)
(See headnote+)
(f) Insert FULL name(s) AND address(es) of actual inventor(s)
(See headnote++)
(g) Recite how applicant(s) derive(s) title from actual inventor(s)
(See headnote++)
(h) Insert country, filing date, and basic applicant(s) for the/or EACH basic application
(i) Insert PLACE of signing
(j) Insert DATE of signing
(k) Signature(s) of declarant(s)

Note: No legalization or other witness required

In support of the (a) convention application made by

(b) N.V.Philips'Gloeilampenfabrieken,

(hereinafter called "applicant(s)") for a patent for an
invention entitled (d) "Signal buffer circuit arrangement".

(c) Dirk Jan Sakkers
a Deputy Manager for Patents and Trade Marks
of N.V.Philips'Gloeilampenfabrieken
of Emmasingel, Eindhoven, the Netherlands,
do solemnly and sincerely declare as follows:

1. I am/we are the applicant(s).

2. I am/we are authorized to make this declaration on behalf of the applicant(s).

3. I am/we are the actual inventor(s) of the invention.

(See, where the applicant(s) are not the actual inventor(s))

Christopher Paul SUMMERS and
Donald George THOMPSON
both of New Road, Mitcham Junction, Mitcham, Surrey CR4 4XY, England,
is/are the actual inventor(s) of the invention and the facts upon which the applicant(s) is/are entitled to
make the application are as follows:

(g) The Applicant is the assignee from Philips Electronic and
Associated Industries Limited of Abacus House, 33 Gutter Lane,
EC2Y 8AH, England, who are in turn the assignees from the said
actual inventors by virtue of an assignment.

(Note: Paragraphs 3 and 4 apply only to Convention applications)

3. The basic application(s) for patent or similar protection on which the application is based is/are
identified by country, filing date, and basic applicant(s) as follows:

(b) in Great Britain on 26th September 1977
by Philips Electronic and Associated Industries Limited

4. The basic application(s) referred to in paragraph 3 hereof was/were the first application(s) made in
a Convention country in respect of the invention the subject of the application.

Declared at (k) Eindhoven, The Netherlands
Dated (l) 4th September 1976
(m) 

To: The commissioner of Patents

PHB 32592
Claim 1. A signal buffer circuit arrangement for providing an inter-face between the circuit of an integrated circuit and an external circuit, said arrangement having two current paths including respective unidirectional conductive devices by which conduction in one or the other only of these two current paths can be controlled, which arrangement is characterized in that it comprises internally of the integrated circuit two signal paths which form said two current paths and which are connected to the same external connecting pin of the integrated circuit, in each of which signal paths the respective unidirectional conductive device can be arranged to be reverse-biased in the presence of a signal in the other path to inhibit the passage of a signal in its own path, said signals being of opposite polarity or occupying respective different amplitude ranges of the same polarity, and said arrangement further comprising externally of the integrated circuit a load resistor which is connected at one end to said external connecting pin, together with means for connecting the other end of said load
resistor to one or the other of two bias voltage terminals to which can be applied respective biasing voltages for determining which one of the two unidirectional conductive devices is to be reverse-biased, as aforesaid.
COMPLETE SPECIFICATION FOR THE INVENTION ENTITLED:
"SIGNAL BUFFER CIRCUIT ARRANGEMENT".

The following statement is a full description of this invention, including the best method of performing it known to me:
This invention relates to signal buffer circuit arrangements and more particularly to a signal buffer circuit arrangement of a type suitable for providing an interface between the circuit of an integrated circuit and an external circuit.

A well-known problem that exists in the design of integrated circuits is to use on an integrated circuit as few pins as possible for making external connections between the internal circuitry of the integrated circuit and external circuitry. The fewer the number of pins that are used, the more cost effective is an integrated circuit package, even where additional circuitry is included in the integrated circuit in order to save using a pin.

It is desirable to provide an integrated circuit that has a particular output that can be interfaced with an input of an external circuit which may require an integrated circuit output of one polarity for one form of the external circuit but of opposite polarity for another form of the external circuit. One example of this is in television receivers some of which are designed to receive a separated synchronising signal without inversion, whereas others are designed to receive a separated synchronising signal which has been inverted. Thus, a synchronising regenerator or separator circuit which is realised as an integrated circuit package for general use as a component of a television receiver would normally require two separate external pins to provide the two versions of the separated synchronising signal.

The present invention proposes an integrated circuit of the above type which enables only a single external pin to be used to provide at that pin an output signal of one or the other of two possible different polarities or one of the other of two different amplitudes ranges of the same polarity.

According to the invention there is provided a signal buffer circuit arrangement of the type referred to having two current paths including respective unidirectional conductive devices by which conduction in one or the other only of these two current paths can be
controlled, which arrangements is characterized in that it comprises internally of the integrated circuit two signal paths which form said two current paths and which are connected to the same external connecting pin of the integrated circuit, in each of which signal paths the respective unidirectional conductive device can be arranged to be reverse-biased in the presence of a signal in the other path to inhibit the passage of a signal in its own path, said signals being of opposite polarity or occupying respective different amplitude ranges of the same polarity, and said arrangement further comprising externally of the integrated circuit a load resistor which is connected at one end to said external connecting pin, together with means for connecting the other end of said load resistor to one or the other of two bias voltage terminals to which can be applied respective biasing voltages for determining which one of the two unidirectional conductive devices is to be reverse-biased, as aforesaid.

In one particular embodiment of the invention the unidirectional conductive device in one signal path is a first transistor of one conductivity type and the unidirectional conductive device in the other signal path is a second transistor of the opposite conductivity type, which first and second transistors have their emitter-collector paths connected in series between supply lines, with their emitters connected together and to said external connecting pin, and the arrangement further comprising an input transistor having its base connected to receive an input signal, and its emitter and collector connected one each to the base of a respective one of said first and second transistors to feed thereto non-inverted and inverted versions of the input signal, one of said first and second transistors being biased for conduction and the other being cut-off, as determined by the connection of said load resistor. This embodiment gives the advantage that a single signal source can be used to provide an input signal which is transformed into non-inverted and inverted versions by the arrangement.

In order that the invention may be more
fully understood, reference will now be made by way of example to the drawing accompanying the Specification. In the drawing the single figure shows a realisation of a part of a synchronising regenerator circuit arrangement according to the invention.

The synchronising regenerator circuit arrangement comprises three transistors 11, 12 and 13 being connected between a signal voltage terminal 14 to which a signal voltage \( V_{ab} \) is applied, and the integrated circuit external connecting pin 3. A load resistor 8, a switch or strap 9 and bias voltage terminals \(+V\) and \(OV\) are provided for feeding at will a d.c. voltage \( +V \) or \( OV \) to the pin 3. The transistor 11 is an input transistor which has its emitter-collector path connected between positive and negative supply lines \(+ve\) and \(-ve\) in series with equal value emitter and collector resistors 15 and 16. A synchronising signal voltage \( V_{ab} \) is applied to the base of the transistor 11 which is responsive to produce a same polarity version of the signal voltage \( V_{ab} \) at its emitter and an inverted polarity version of the signal voltage \( V_{ab} \) at its collector. The two transistors 12 and 13 are of opposite conductivity types and have their emitter-collector paths connected in series between the positive and negative supply lines \(+ve\) and \(-ve\). The emitters of these two transistors 12 and 13 are connected together and to the external connecting pin 3.

Assuming that the voltages on the positive and negative supply lines \(+ve\) and \(-ve\) have, respectively, the same value as the bias voltages at terminals \(+V\) and \(OV\), say, \(+12v\) and ground, respectively, then when the load resistor 8 is strapped to the bias voltage terminal \(OV\), the transistor 12 is biased for conduction and the transistor 13 is cut-off. Conversely, when the load resistor 8 is strapped to the bias voltage terminal \(+V\),
the transistor 13 is biased for conduction and the
transistor 12 is cut-off. The bases of the two transistors
12 and 13 are connected to the emitter and collector,
respectively, of the transistor 11. The particular tran-
sistor 12 or 13 which is biased for conduction by the
strapping of the load resistor 8 is responsive to the
same or inverted polarity version (as the case may be)
of the signal voltage Vab applied to its base to produce
that version of the signal voltage Vab at its emitter and
thus at the external connecting pin 3.
THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS

1. A signal buffer circuit arrangement for providing an interface between the circuit of an integrated circuit and an external circuit, said arrangement having two current paths including respective unidirectional conductive devices by which conduction in one or the other only of these two current paths can be controlled, which arrangement is characterized in that it comprises internally of the integrated circuit two signal paths which form said two current paths and which are connected to the same external connecting pin of the integrated circuit, in each of which signal paths the respective unidirectional conductive device can be arranged to be reverse-biased in the presence of a signal in the other path to inhibit the passage of a signal in its own path, said signals being of opposite polarity or occupying respective different amplitude ranges of the same polarity, and said arrangement further comprising externally of the integrated circuit a load resistor which is connected at one end to said external connecting pin, together with means for connecting the other end of said load resistor to one or the other of two bias voltage terminals to which can be applied respective biasing voltages for determining which one of the two unidirectional conductive devices is to be reverse-biased, as aforesaid.

2. A signal buffer circuit arrangement as claimed in Claim 1, characterized in that the unidirectional conductive device in one signal path is a first transistor of one conductivity type and the unidirectional conductive device in the other signal path is a second transistor of the opposite conductivity type, which first and second transistors have their emitter-collector paths connected in series between supply lines, with their emitters connected together and to said external connecting pin, and the arrangement further comprising an input transistor having its base connected to receive an input signal, and its emitter and collector connected one each to the base of a respective one of said first and second transistors to feed thereto non-inverted and inverted
versions of the input signal, one of said first and second transistors being biased for conduction and the other being cut-off, as determined by the connection of said load resistor.

3. A signal buffer circuit arrangement as claimed in any preceding Claim, characterized in that it is provided in conjunction with an integrated circuit which is formed as a sync. separator circuit that can provide either non-inverted or inverted separated synchronising signals at said external connecting pin.

4. A signal buffer circuit arrangement substantially as hereinbefore described with reference to the single figure of the drawing.

Dated this first day of December, 1981.

N.V. PHILIPS GLOEILAMPENFABRIEKEN